Tran Le Anh Tuan

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Summary

- Excellent in written and spoken communication skills, critical thinking and time management.
- 7+ years of industrial experience in developing highly efficient data science tools, designing and building dashboards for data analysis and visualization.
- Solid research experience in statistical modeling, numerical analysis and machine learning, especially for nano-scale devices and semiconductor manufacturing.
- Self-motivation, goal-orientation, responsibility, team player with a professional manner.
- Korean Permanent Residency(F5 visa): Do not need visa sponsorship.

Academic Qualifications

- **Ph.D. in Computational Nanoelectronics** — **Daejeon, Korea**
  Korea Advanced Institute of Science and Technology (**KAIST**) — 2006-2011
  PhD thesis: "Modeling of silicon nanowire MOSFETs using the Multi-subband Monte Carlo Method"
- **M.Sc. in Electronics and Telecommunication** — **Hanoi, Vietnam**
  Hanoi University of Science and Technology (**HUST**) — 2003-2005
- **B.Sc. in Electronics and Telecommunication** — **Hanoi, Vietnam**
  Hanoi University of Science and Technology (**HUST**) — 1998-2003

Industry Experience

Samsung Electronics — **Suwon, Korea**
Logic Process Architecture (PA) Team, Foundry Business — Oct. 01, 2011 - Mar. 31, 2019
Staff Engineer

- **Development of MongoDB (NoSQL) Database, Node.js and Express framework for yield management and device performance improvement in foundry processes**
  - MongoDB Database of PA team has been developed using pymongo library.
  - Fab data from Samsung cloud platform has been uploaded to MongoDB.
  - By using data of PA MongoDB, integrated web-based reports of yield, device and process analysis have been generated and reported.

- **Development of Yield Analysis Spotfire Tools**
  - Low Yield Wafer Root Cause Analysis.
  - Yield expectation, analysis and enhancement.

- **Development of Device to Process Correlation and Outlier Analysis using Python**
  - Normal distribution outlier detection: Develop a simple but efficient algorithm using statistics and semiconductor domain knowledge to find outliers, test modals, and mapping them on a wafer map.
  - Multivariate outlier detection methods using data mining, including Fast MCD Mahalanobis distance-based method, for correlation analysis amongst process, electrical and chip probing parameters to find root causes of weak points in 14nm and 10nm FINFET technology.

- **Development of Advanced Process Control (APC) and Automated Report System using Spotfire**

- Development the automation trend assessment tool: A graphical representation of time series data showing a trend line that reveals a general pattern of changes such as excursion, internal process split and provides messages of change points and statistical process control (Cp/Cpk and Pp/Ppk).
- This tool is automated by Python scripts embedded into TIBCO Spotfire software and has been applying for key inline FEOL and BEOL process parameters and key electrical (device and SRAM) parameters of 14nm and 10nm FINFET technology.
- Cumulative Cp/k Fail Rate: A predictive tool to find weak points in the semiconductor process and to recommend the decisions.
- Analysis of weak points in electronics macros: Statistical Cp and k, FPI (Fail Point Index) and FIR (Fail Item Repeatability).

- **Applying Machine Learning To Semiconductor Manufacturing**
  - Variability reduction for semiconductor devices: High-dimensional data reduction methods combined with semiconductor segmentation techniques to find key process parameters for 14nm and 10nm FINFET technology.
  - Clustering algorithms and tool development for semiconductor process applications.

- **Semiconductor Modeling and Simulation**
  - [Method development] Develop a smart sampling based method, so-called "the Fast Monte Carlo" for yield estimation of a Static Random Access Memory (SRAM) cell. The code is implemented by Python script with the SRAM Spice netlist library.
  - Statistical SRAM cell design, Z-score method and soft yield analysis.
  - SRAM cell performance, stability, reliability and variability.
  - SRAM fault modeling: Creating a Spice netlist for 14nm FINFET SRAM cell and carrying out Synopsis HSPICE simulation to analyse SRAM parameters, such as Static Noise Margin (SNM) vs. Resistor and Iread vs. Resistors, which are presented based on physical defects.

- **Data Analytics and Visualization**
  - Expertise in TIBCO Spotfire software for data analysis and visualization.
  - Expertise in Matplotlib, seaborn and D3.js for data visualization.
  - Work closely with other parts to define data process and approach.

- **Project Management**
  - Lead a small part in Process Architecture Verification Engineering (PAVE) team.
  - Shares knowledge by mentoring staff and frequently making internal training.

Kramer Electronics Representative **Hanoi, Vietnam**
Technical and Sales Engineer 7.2004 – 07.2006

- **Worked as a Technical and Sales Engineer**
  - Support audio and video technical solutions to customers.
  - Work with customers to define business objective and strategy, then report to headquarters in Singapore and Israel.
  - Hand on implementing sale progress.
  - Introducing and marketing products to potential customers.

Blockchain Project Experience (personal project: my passion to develop code at home)

- **A basic blockchain implementation using Python.** https://github.com/tuantla80/Blockchain
  - Demonstrate basic concepts of blockchain to understand technical aspects internally.
    (1) Blockchain itself (2) Peer to peer network (3) Consensus mechanism
  - A new version to add more features is currently developed.

Research Experience

Korea Advanced Institute of Science and Technology (KAIST) **Daejeon, Korea**
Department of Information and Communications Engineering 8.2006 – 8.2011
Graduate Researcher

- **Semi-classical Monte Carlo Method for Semiconductor Device Simulation**
  - Deeply investigating the fundamental concepts of carrier transport in MOSFETs devices.
  - Developing an in-house semi-classical Monte Carlo code to create a strong background to develop Multi-subband Monte Carlo simulator.

- **Multi-subband Monte Carlo for the Modeling of Silicon Nanowire Transistor**
  - Theoretically deriving all relevant scattering mechanisms including acoustic, non-polar optical phonon and surface roughness form factor for k•p method.
  - Developing an in-house simulator with a Multi-subband Monte Carlo (MSMC) approach to investigate the behavior of carrier mobility in silicon nanowire MOSFETs to assess device performance. The simulation tool, which is written by C/C++ language with MPI for parallel computing, was developed from the ground-up to solve 2D Poisson equation coupled with 1D Boltzmann equation in the transport direction and 2D Schrodinger equation in the quantization plane. In particular, the 1D Boltzmann equation is solved by statistical Monte Carlo method. The simulator is very versatile to add more advanced effects and can be used to explain the experimental data.
  - Creating a strong basis for further research on many relevant aspects related to the operation of the silicon nanowire transistors.

- **Quantum Transport in MOSFET and Silicon Nanowire Transistors Using NEGF Model**
  - A ballistic quantum transport has been investigated to propose a guideline for the next generation of nanowire transistor.
  - 1D NEGF Matlab code.

- **Hole Effective Masses in Si Nanowire pMOSFETs Using the k•p Method**
  - Deeply investigating a physics insight of the validity and limitation of the parabolic effective mass model (PEM).
  - Benchmarking the parabolic effective mass model with the k•p method for the p-type nanowire devices.
  - Proved that the isotropic parabolic effective mass model (PEM) simply failed to produce important transport characteristics such as subthreshold slope, on-current and threshold voltage shift.
  - Proposed a modified PEM Hamiltonian model to overcome the limitation of PEM model.
  - Proposed an MSMC transport kernel using k•p theory to investigate the hole mobility in Si nanowire pMOSFET.

Korea Advanced Institute of Science and Technology (KAIST) **Daejeon, Korea**
Department of Information and Communications Engineering 8.2006 – 8.2011
Teaching Assistant
Lecture notes preparation, homework design and grading, Q&A session, final project grading**.**

- **Courses**
  - General Physics
  - Electromagnetic Theory
  - Applied Quantum Mechanics
  - Programming Fundamentals C/C++

Hanoi University of Science and Technology (HUST) **Hanoi, Vietnam**
Department of Electronics and Telecommunication 2003-2005
Research Assistant
- Focusing on studying novel devices including DG MOSFETs and FinFETs.

- Semiconductor process technology
- Device physics and compact model

Technical and Personal Skills

- **Programming Languages**: Python, C/C++, HTML/CSS/Javascript, Matlab, Perl, MPI Parallel Programming, VBA, Fortran, SQL.
- **Toolkit Used**: Pycharm, Anaconda, Spyder, GDB.
- **Frameworks/ Libraries Used**: [**Python**] NumPy, SciPy, Panda, Scikit-Learn, Tensorflow, Matplotlib, Seaborn, Plotly, Cufflinks, python-pptx, openpyxl, NLTK, pymongo, django. [**HTML/CSS/Javascript**] Node.js, socket.io, D3.js, C3.js, Bootstrap, jQuery. [**C/C++**] Lapack, PETSc. [**Database**] MongoDB, PostgreSQL, [**Container technology - Virtualization**] Docker, Amazon AWS (Cloud Formation, Terraform, EC2 instance) , Google Cloud. [**Automation/Build**] Ansible.
- **Platform Used**: Windows, Linux, Unix, Solaris.
- **Software**: TIBCO Spotfire, SAS JMP, MiniTab, Microsoft Office (Excel, PowerPoint, Words), Origin, GNUplot, Paramatrix, Tableau.
- **TCAD/EDA software**: Synopsis HSPICE, StarRC (Parasitic extraction).
- **Language skills**: English, Vietnamese (native), Korean (basic).

Fellowships and Awards

● Intermediate Award at Process Architecture Team	Samsung Electronics	Suwon, 2013
● Best Paper Awards	NANO KOREA 2009	KINTEX, 2009
● IITA IT Scholarship	Korean Government	KAIST, 2006-2010
● Honor Bachelor Degree	HUST University	Hanoi, 2003
● Full Scholarships for Undergraduate	Vietnam Ministry of Education	Hanoi, 1998-2003

Journal Publications

1. **Anh Tuan Tran Le** and Mincheol Shin, "Hole-effective Masses in the Transport Calculation of Si Nanowire pMOSFETs", *Journal of Nanoscience and Nanotechnology*, Vol. 11, 322–325, 2011

Conference Publications

1. **Anh Tuan Tran Le** and Mincheol Shin, "Low-Field Electron Mobility Calculation in Silicon Nanowires with a Multi-subband Monte Carlo Approach", The 18th Korean Conference on Semiconductors 2011 (KCS 2011), Jeju, Korea, Feb. 16-18, 2011.

2. **Anh Tuan Tran Le** and Mincheol Shin, "Hole Effective Masses in the Transport Calculation of Si Nanowire pMOSFETs", *NANO KOREA 2009*, The 7th International Nanotech Symposium in Korea, Aug. 26-28, 2009. **(Best Paper Awards)**

3. **Anh Tuan Tran Le** and Mincheol Shin, "Low-Temperature Behaviors and Coulomb-Blockade Effect in Nanowire Schottky-Barrier MOSFET*", The 3rd IEEE-NEMS* (Nano/Micro Engineered and Molecular Systems) Sanya, Hainan, China, Jan. 6-9, 2008

Work permit in Korea

- **Permanent Residence (F-5 visa)**