

Event-Driven Convolution-Based Processing

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<http://www.imse-cnm.csic.es/neuromorphs>

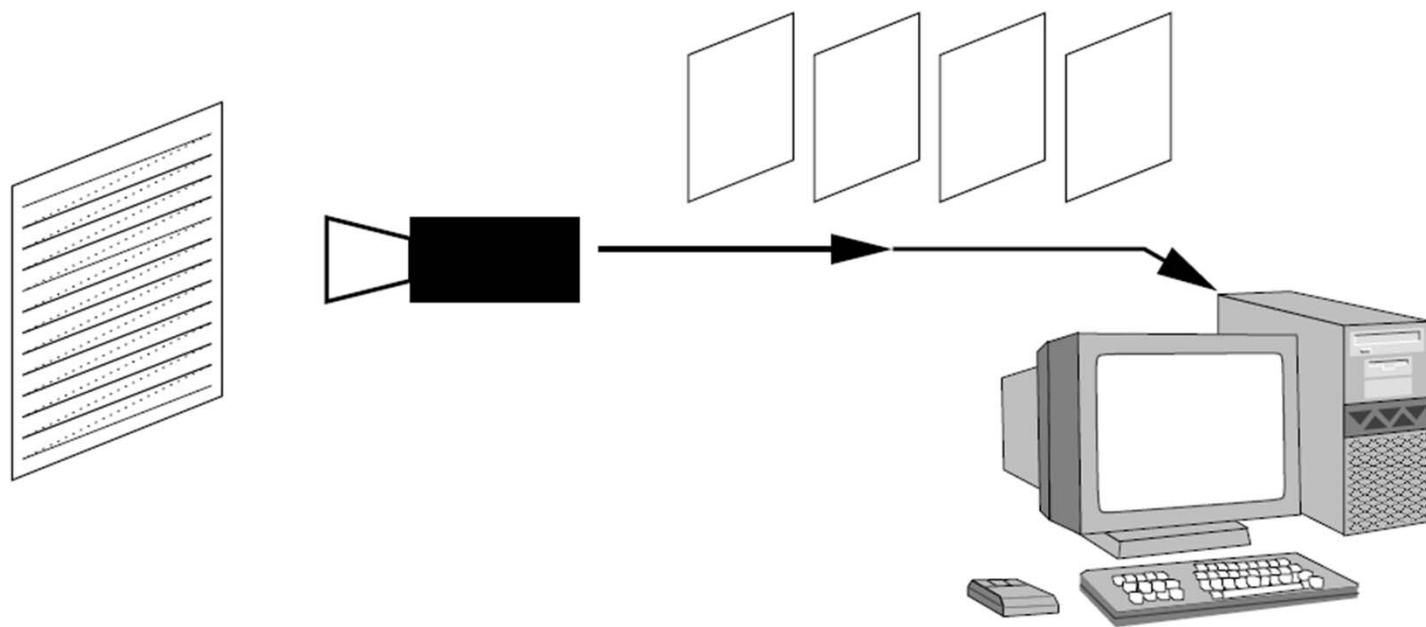


Outline:

- Efficiency of Information Encoding in the Brain
- The CAVIAR Project, the DVS, and the sensitive-DVS
- Event-Driven Convolutions on ASICs, FPGAs, and SpiNNaker
- Event-Driven Convolutions for Stereo Vision
- STBP with minimum Spike Count on SpiNNaker
- Stochastic Binary STDP reduces HW Resources and Energy

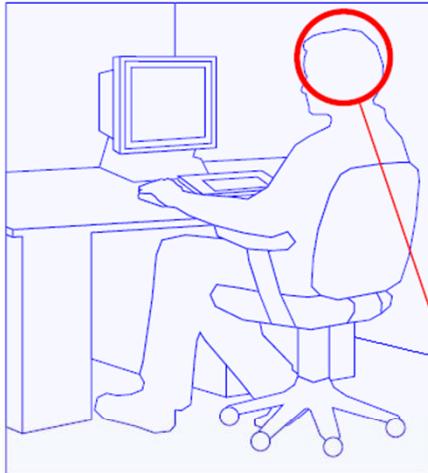
Conventional Vision Sensing/Processing/Recognition

FRAMES



- Feature Extraction Stages
- Feature Combination Stages
- Classification/Decision Stages

Biology

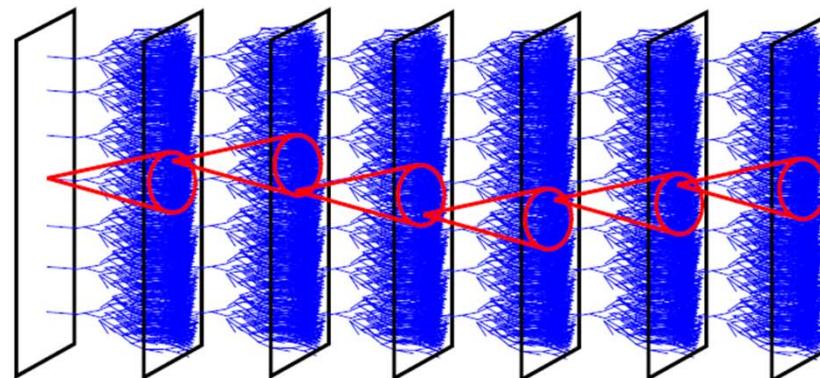


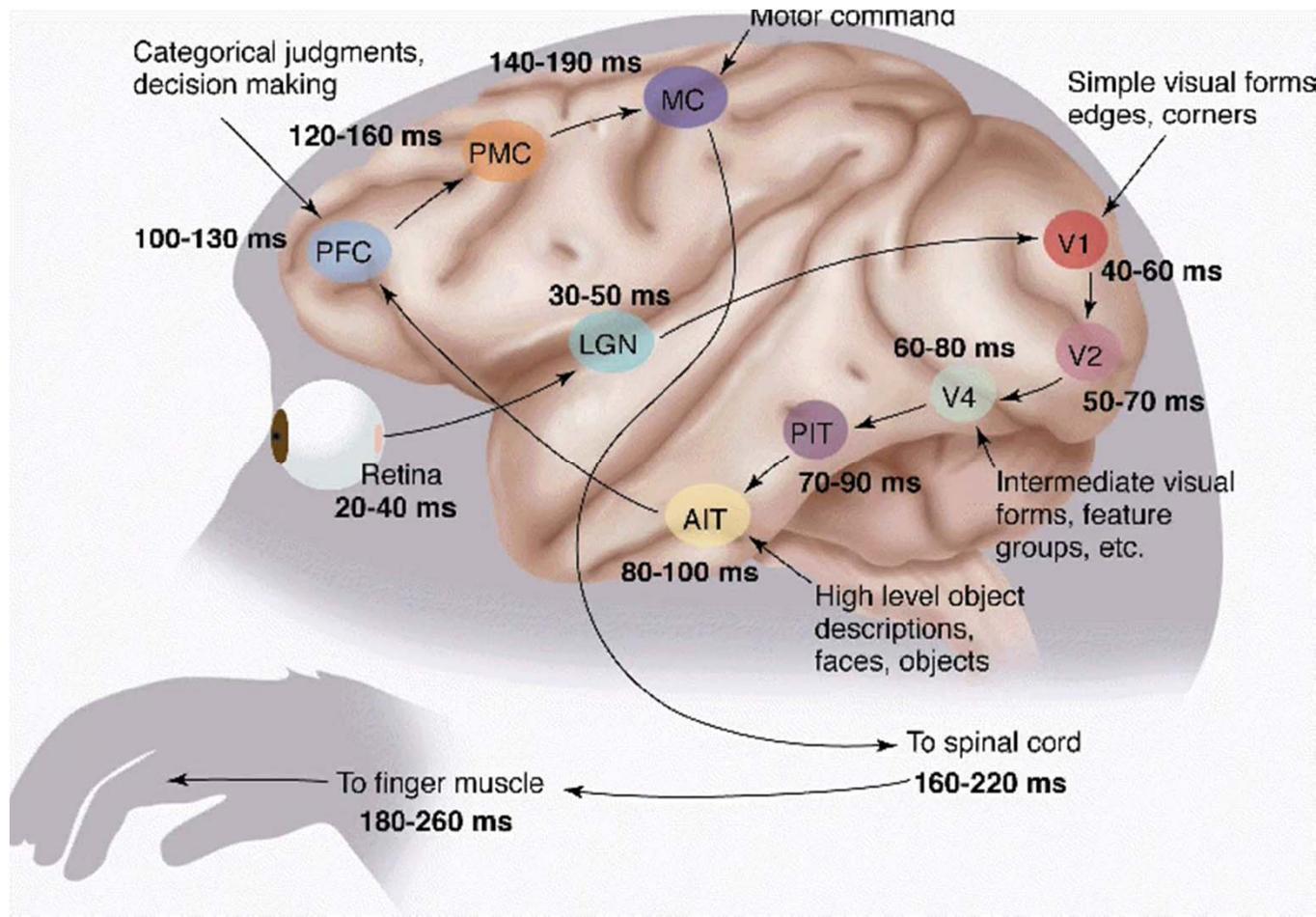
*Recognition
Delay
 $< 150ms$*

- feedforward
- 1 spike/neuron



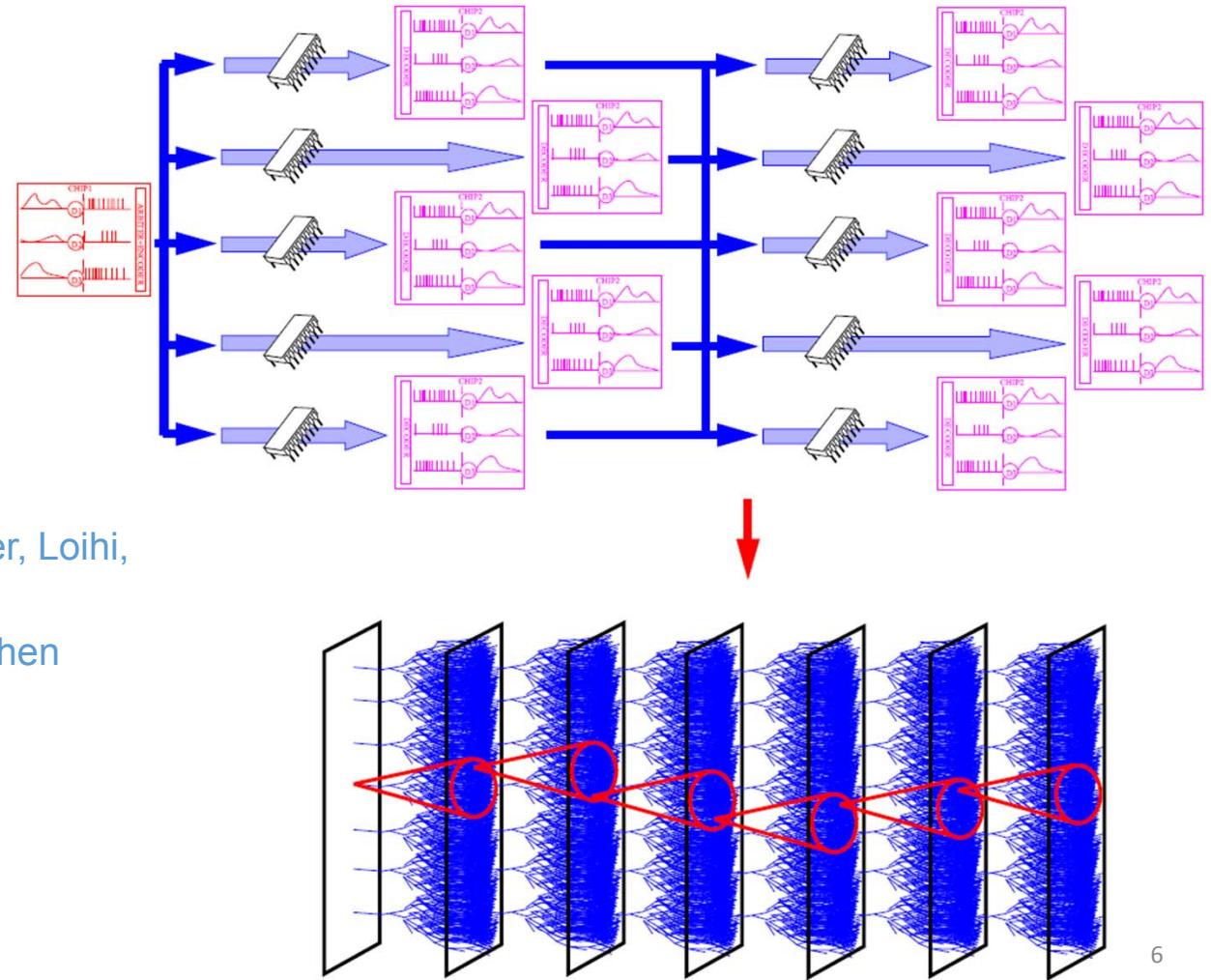
*Simon Thorpe
Nature 1996*





[Thorpe, S. J., & Fabre-Thorpe, M. (2001). Seeking categories in the brain. *Science*, 291(5502), 260-263]

Address-Event-Representation



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FP5 EU Project 2002-2006

www2.imse-cnm.csic.es/caviar/

CAVIAR Project

[Introduction](#)

[Project Main Goals](#)

[Key Issues](#)

[Technical Approach](#)

[Expected Achievements/Impact](#)

[Coordinator Contact Details](#)

[Publications](#)

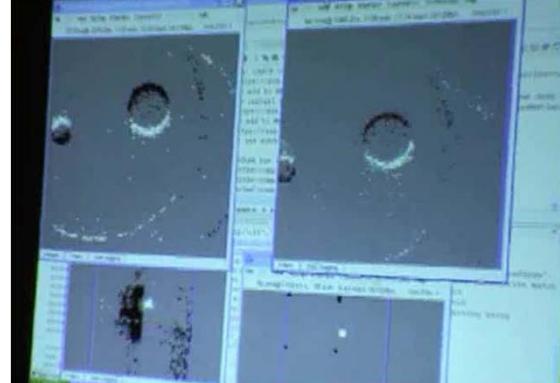
[Restricted Area](#)

[Restricted Area 2](#)

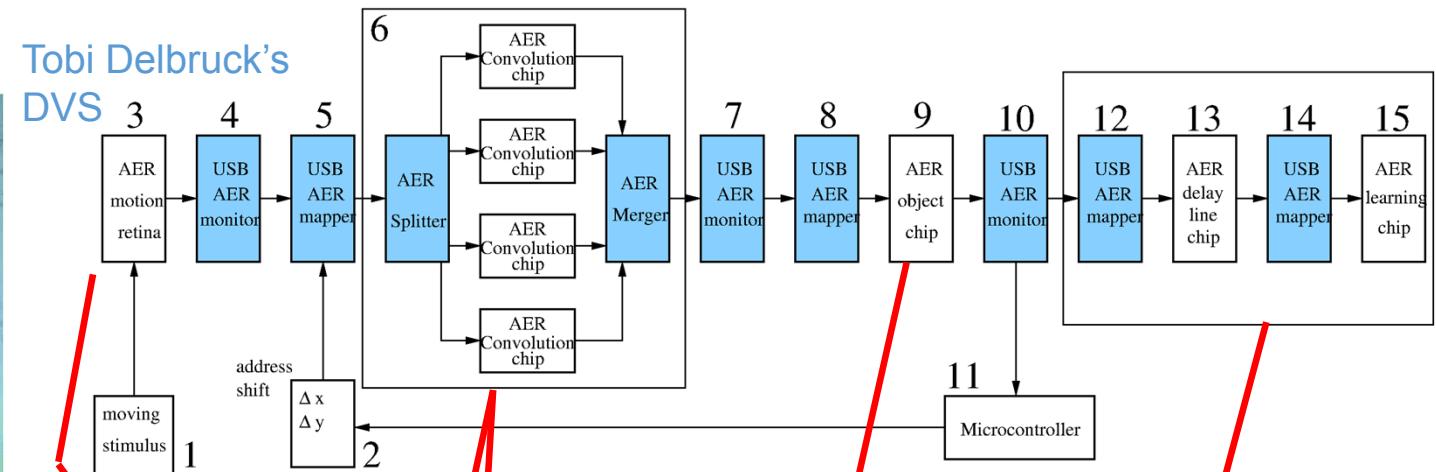
[Videos](#)

[Seeing without Frames](#)

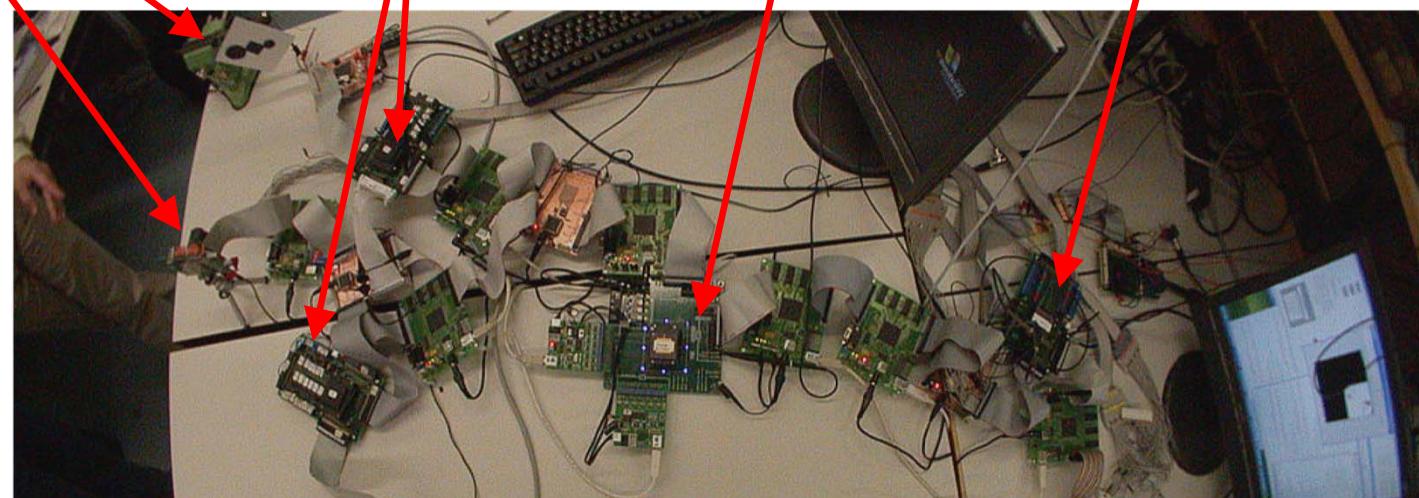
CAVIAR: Convolution AER VIsion ARchitecture



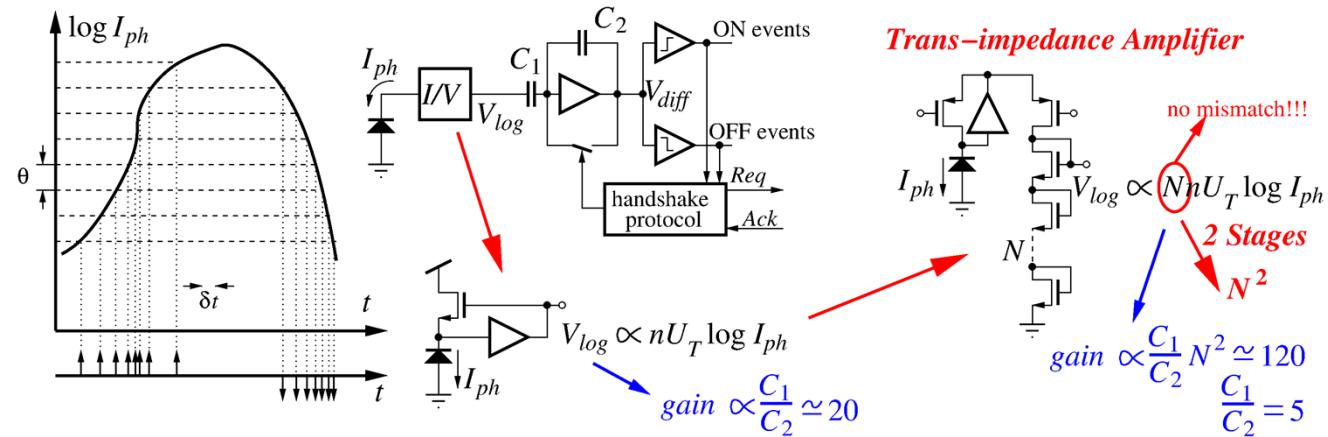
Tobi Delbrück's
DVS



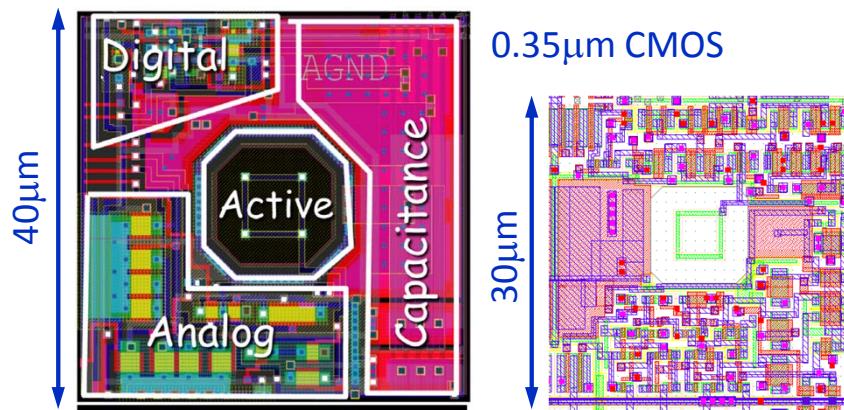
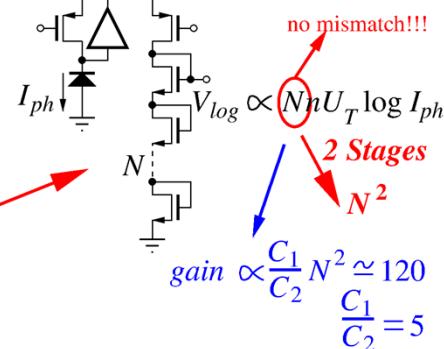
[R. Serrano-Gotarredona, et al.,
"CAVIAR: A 45k-Neuron, 5M-Synapse, 12G-connects/sec AER Hardware Sensory-Processing-Learning-Actuating System for High Speed Visual Object Recognition and Tracking," *IEEE Trans. on Neural Networks*, vol. 20, No. 9, pp. 1417-1438, Sep. 2009]



IMSE's sensitive-DVS



Trans-impedance Amplifier

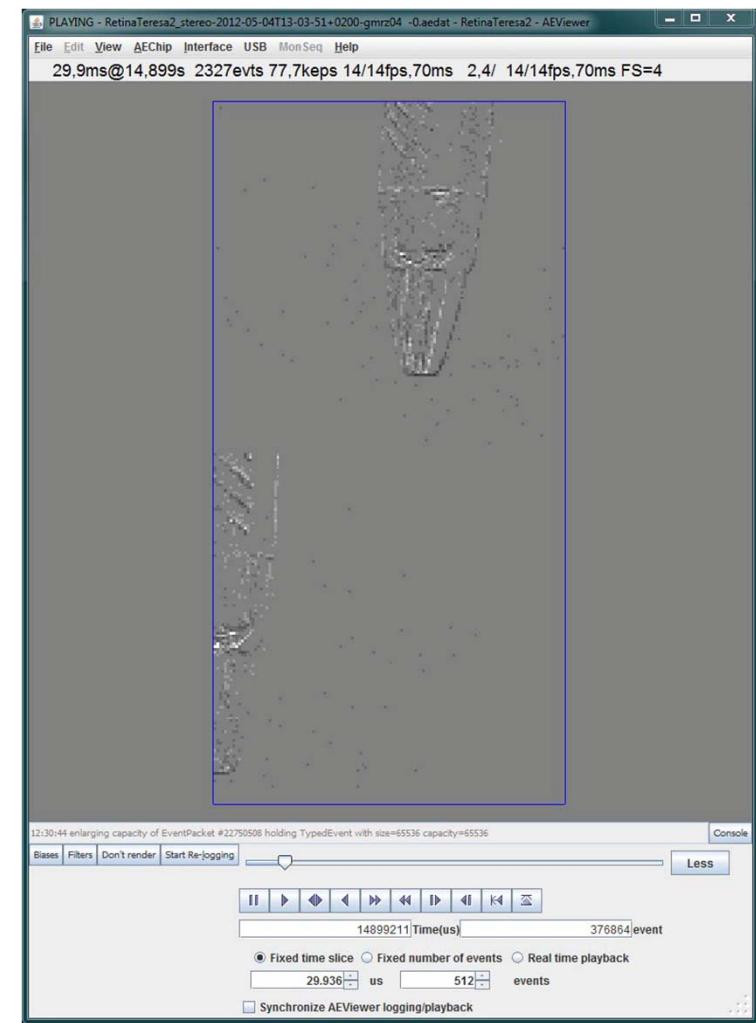


0.35 μ m CMOS

Contrast Sens. 1.5%

RMS Noise 2.1-2.6%

Patent licensed to
Prophesee

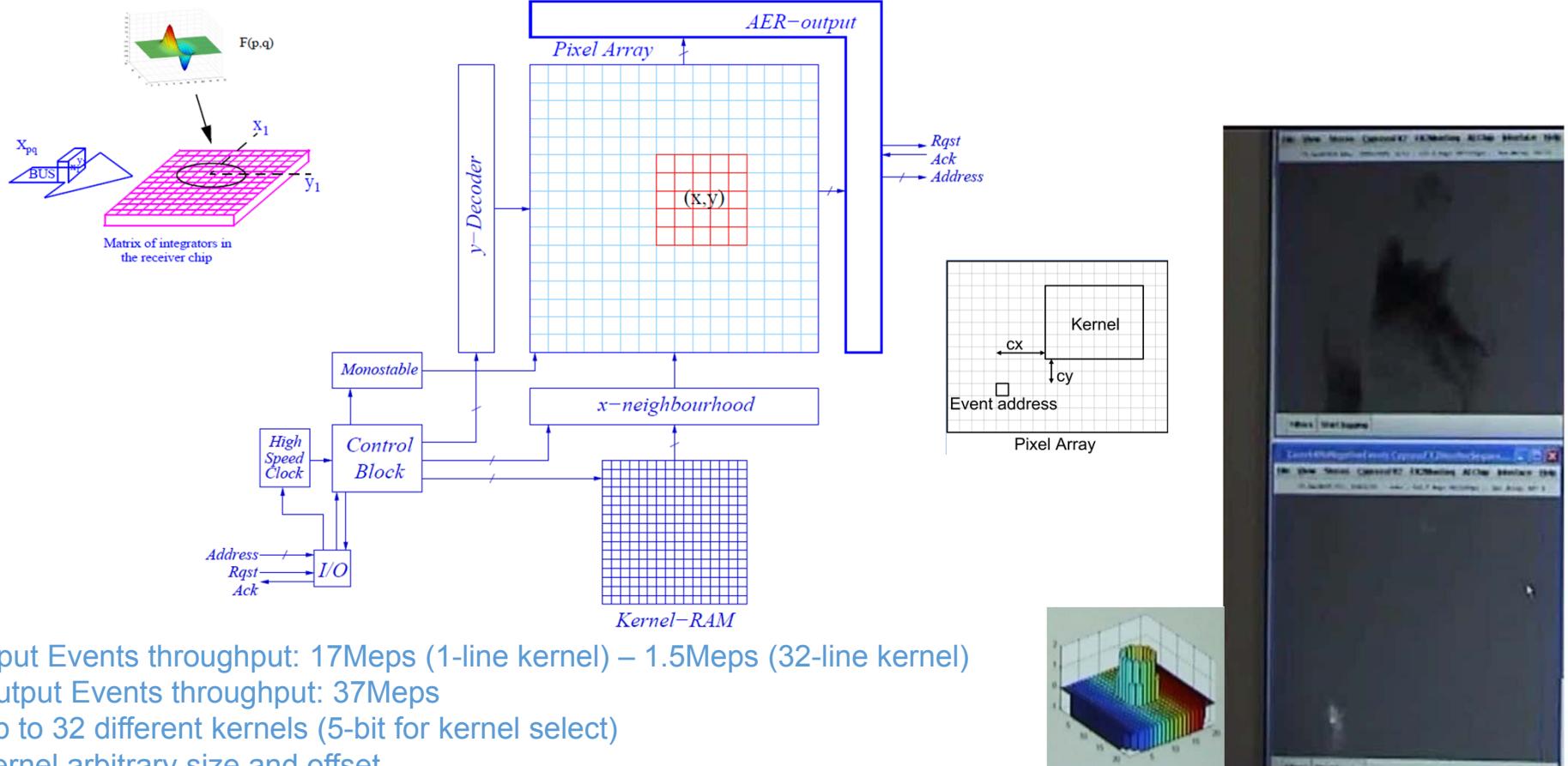


[T. Serrano-Gotarredona and B. Linares-Barranco, "A 128x128 1.5% Contrast Sensitivity 0.9% FPN 3us Latency 4mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Amplifiers," *IEEE J. Solid-State Circuits*, March 2013]

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Event-Driven Convolution ASIC

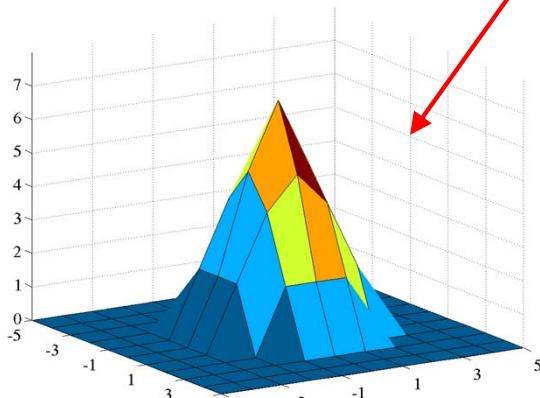
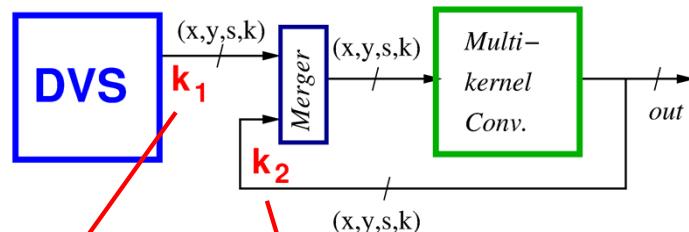


- Input Events throughput: 17Meps (1-line kernel) – 1.5Meps (32-line kernel)
- Output Events throughput: 37Meps
- Up to 32 different kernels (5-bit for kernel select)
- Kernel arbitrary size and offset

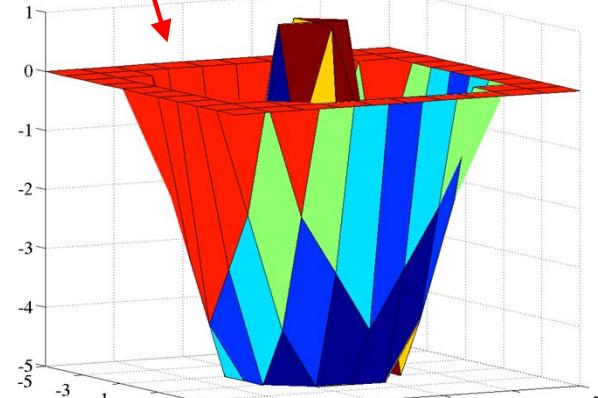
[L. Camuñas-Mesa, et al, "An Event-Driven Multi-Kernel Convolution Processor Module for Event-Driven Vision Sensors," *IEEE J. of Solid-State Circuits*, Feb. 2012.]¹²

Event/Driven Convolutions for WTA Operation

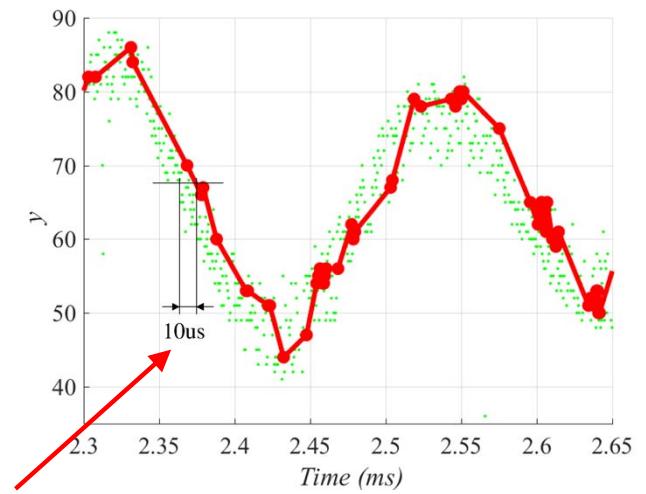
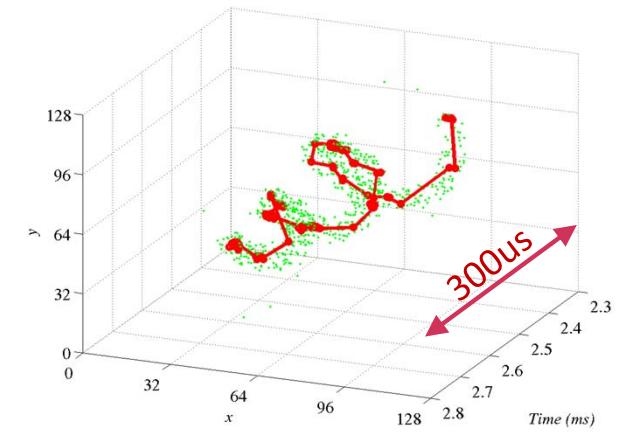
5KHz Spiral



7×7 diffusive kernel

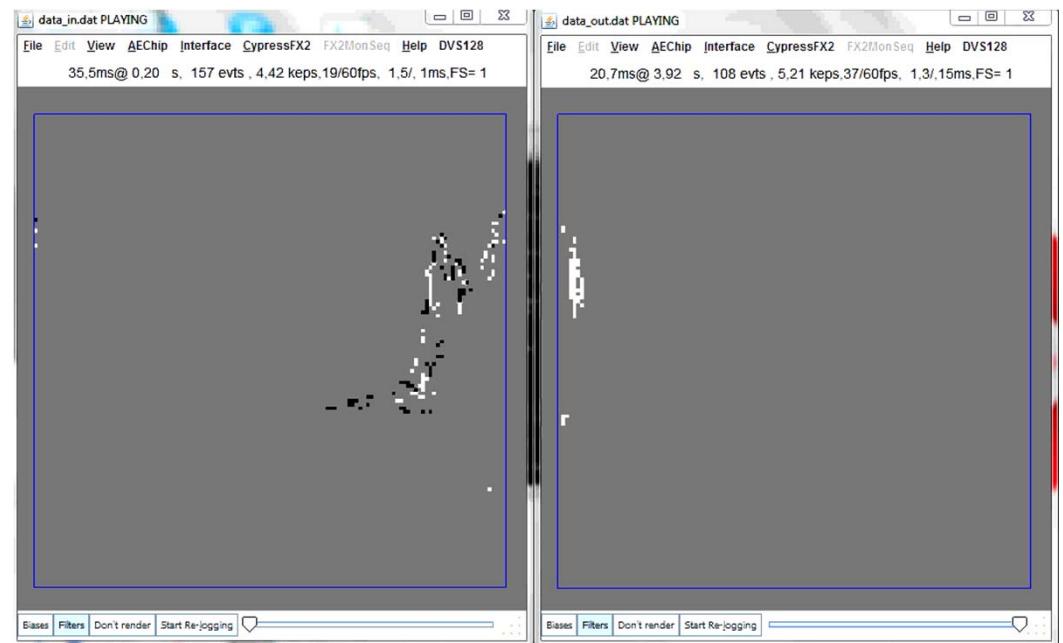
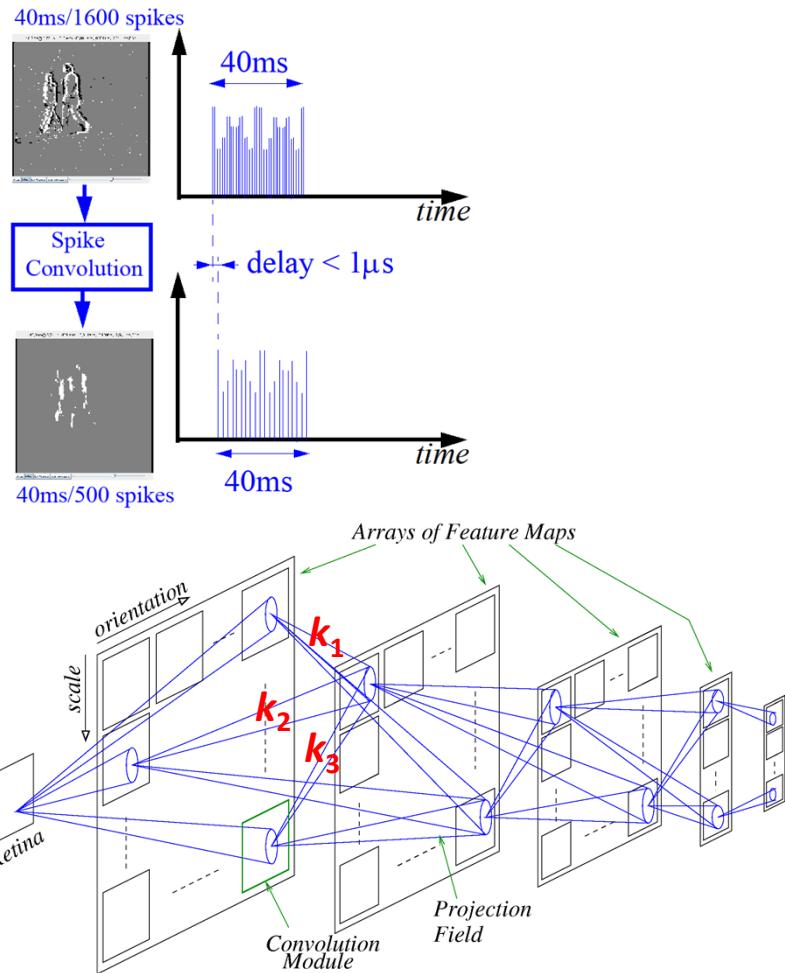


9×9 mexican hat kernel



10μs latency

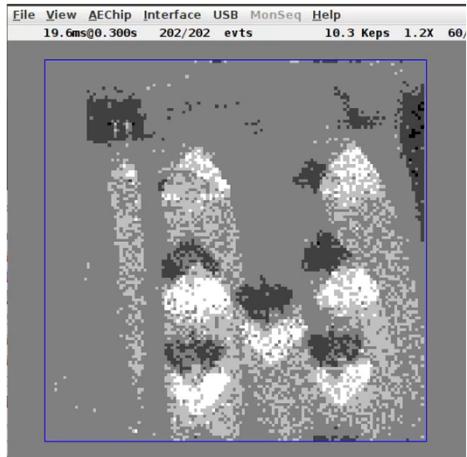
Event-Driven Convolutions Filter in space & time



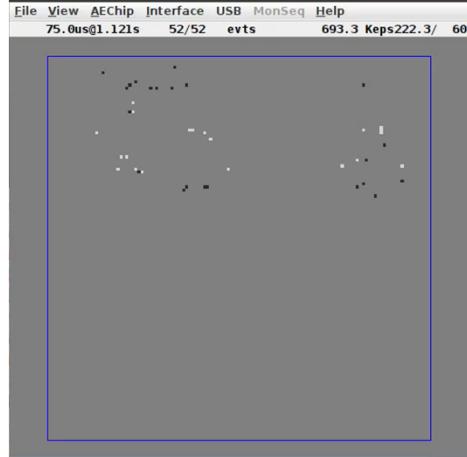
- Filter out temporal noise
- When tracking, average spatial mismatch out over time
- Forgetting rate: detect features within time-window
- Pseudo-simultaneous property

High-Speed Deep SNN

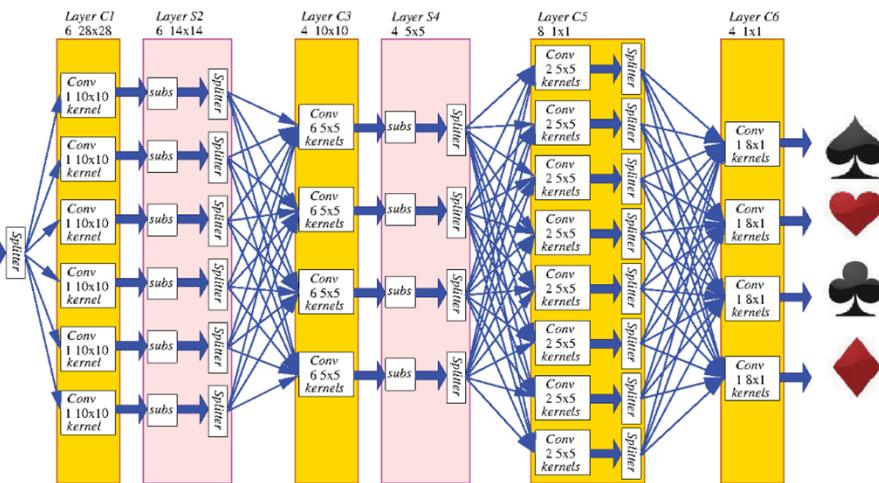
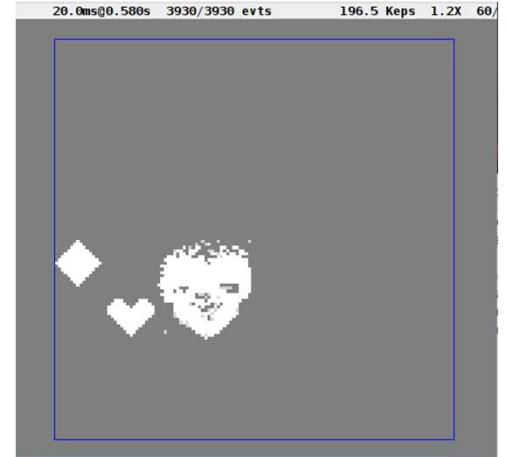
Real time (20ms computer frame time)



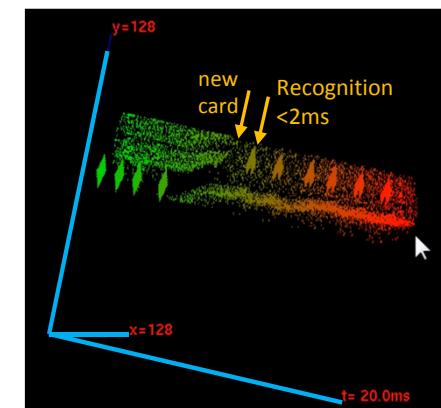
300xslower (75us computer frame time)



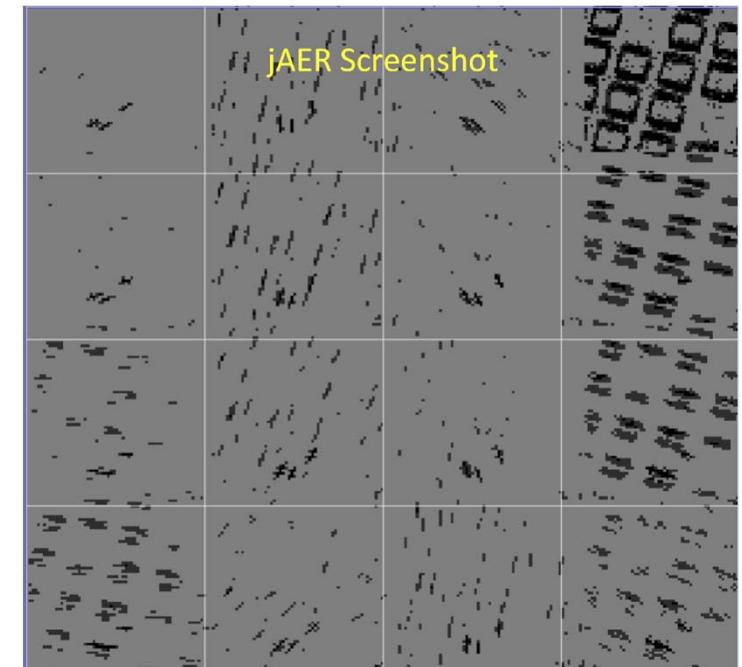
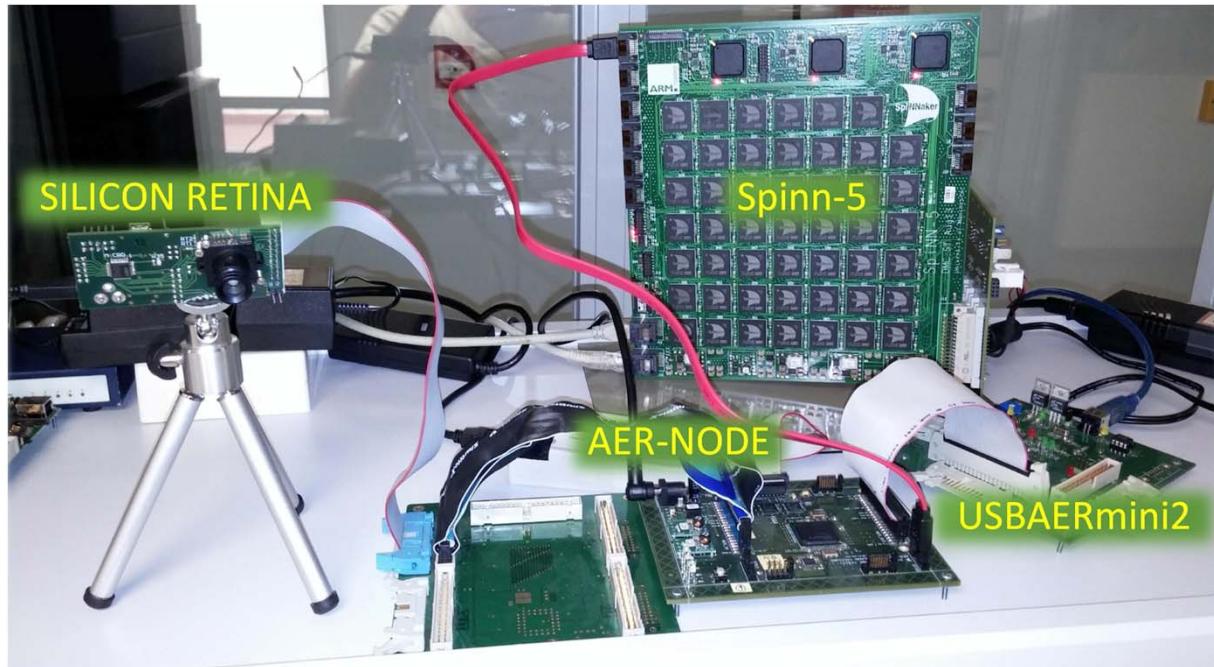
Recognition



[J. A. Pérez-Carrasco, et al., "Mapping from Frame-Driven to Frame-Free Event-Driven Vision Systems ...," IEEE TPAMI, Nov. 2013]
 [L. A. Camuñas et al. "A configurable event-driven convolutional node ...," Frontiers in Neuroscience, 2018]



Event-Driven Convolutions on SpiNNaker



[A. Yousefzadeh, et al. "Performance comparison of time-step-drive versus event-driven neural state update approaches in spinnaker," ISCAS 2018]

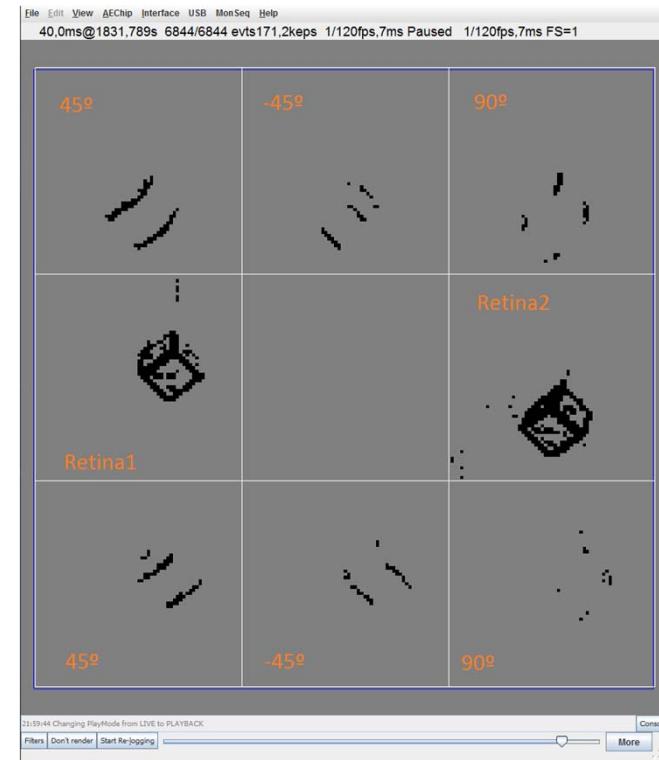
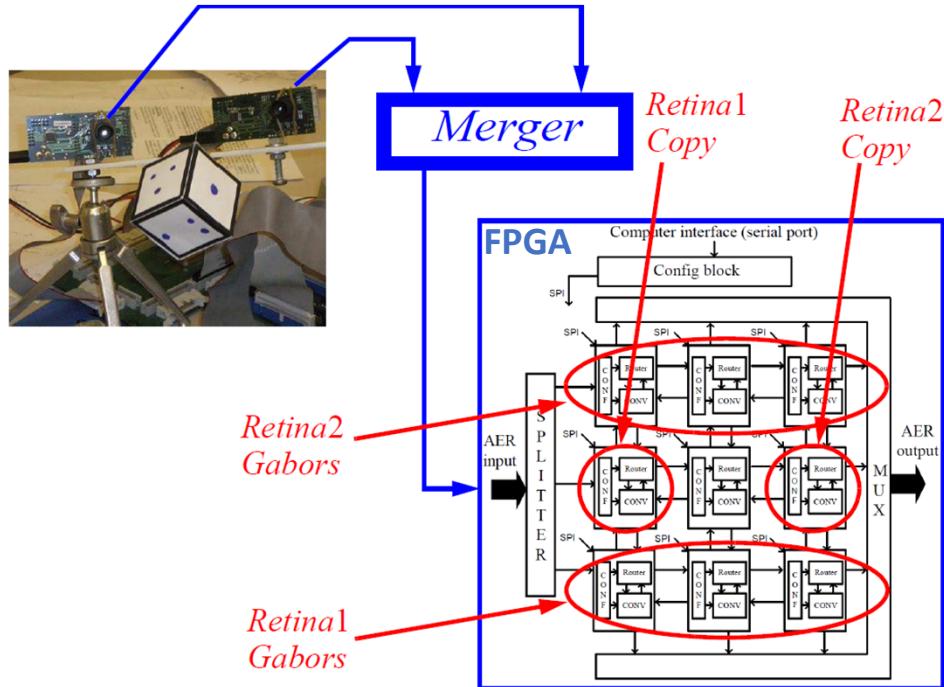
[T. Serrano-Gotarredona, et al. "ConvNets Experiments on SpiNNaker," ISCAS 2015]

[A. Yousefzadeh, et al., "On multiple AER handshaking...," IEEE Trans. On Biomedical Circ. And Syst., 2017]

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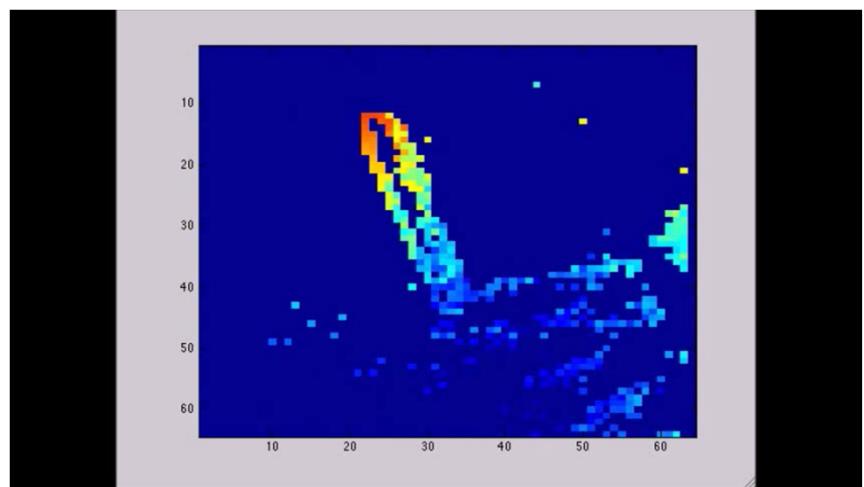
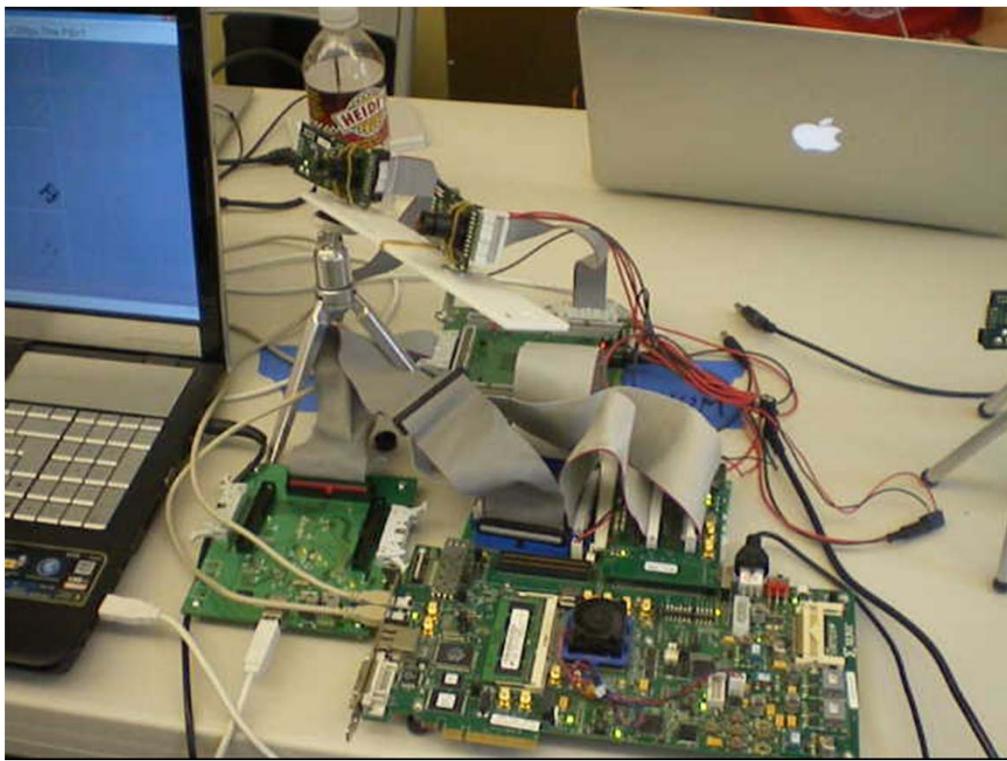
Event-Driven Convolution for Stereo Event Matching



Events match if:

- Within time window Δt
- Same polarity
- Epipolar line constraint
- Belong to same Orientation Convolution

if matched \rightarrow compute (x, y, z) in 3D space



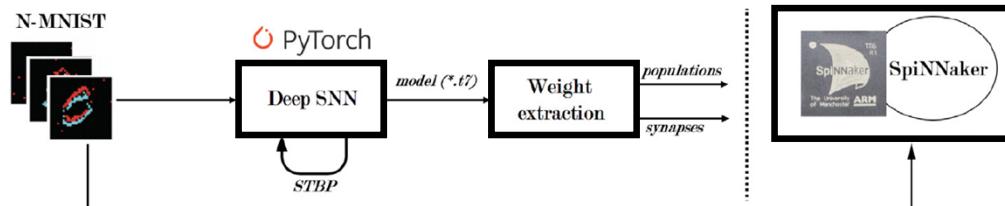
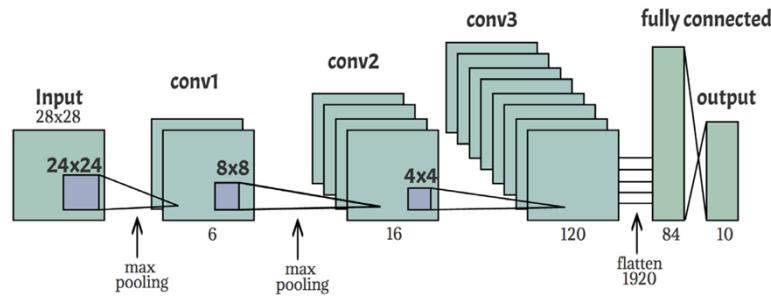
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Spatio-Temporal BP on Spiking Deep ConvNets

- STBP with modified loss function to minimize number of spikes in internal layers.

$$\ell = \frac{1}{S} \sum_{s=1}^S \left(\left\| \mathbf{y}_s - \frac{1}{T} \sum_{t=1}^T \theta_{s,L} \right\|_2^2 + \frac{\lambda_{sr}}{NT} \sum_{t=1}^T \sum_{l=1}^{L-1} \theta_{s,l} \right) \quad \lambda_{sr}: \text{regularization factor } [0,1]$$



[Patiño-Saucedo et. al., “Event-Driven implementation of deep spiking CNNs for supervised classification using the SpiNNaker neuromorphic platform”, *Neural Networks*, 121, pp. 319-328, 2020]

Experimental Results on SpiNNaker

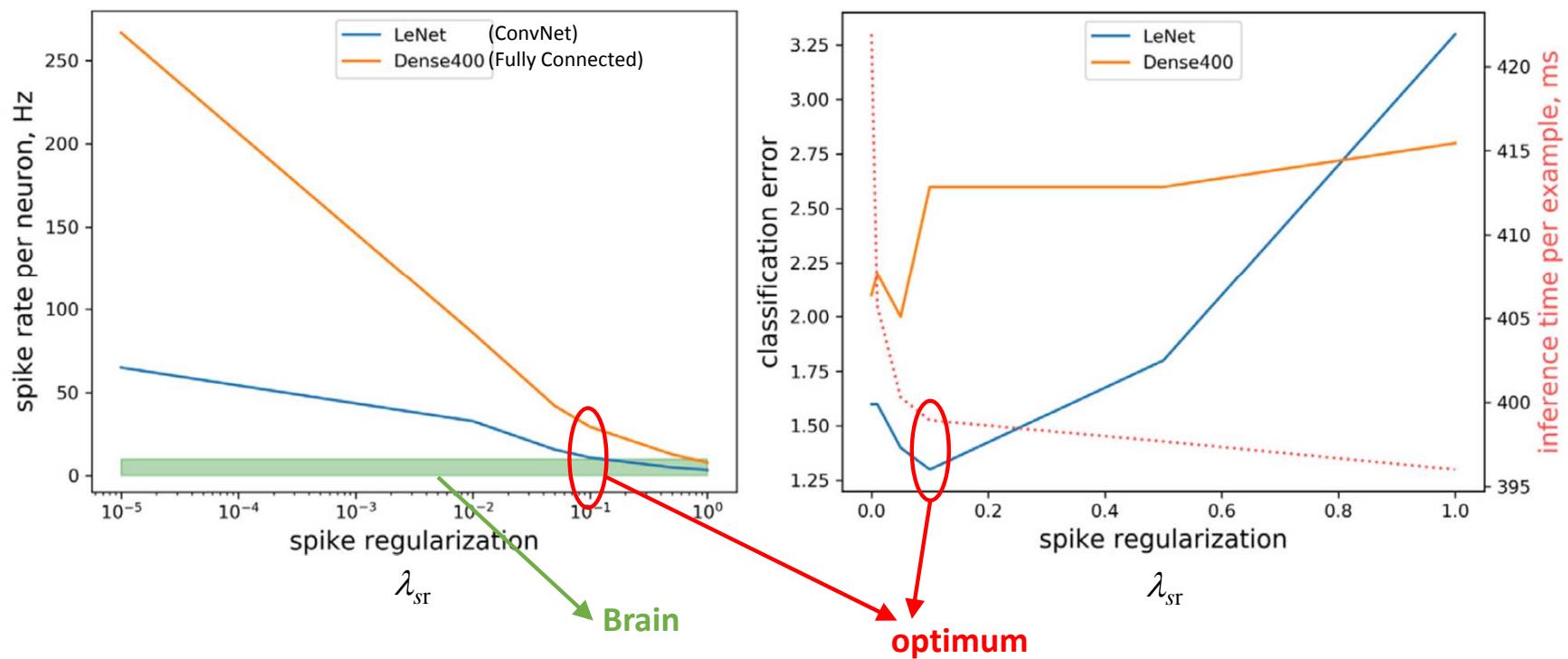


Illustration of Fully-Connected SNN

Implementation of spiking NN for
supervised N-MNIST digit
classification
[Patiño-Saucedo et. Al., 2020]

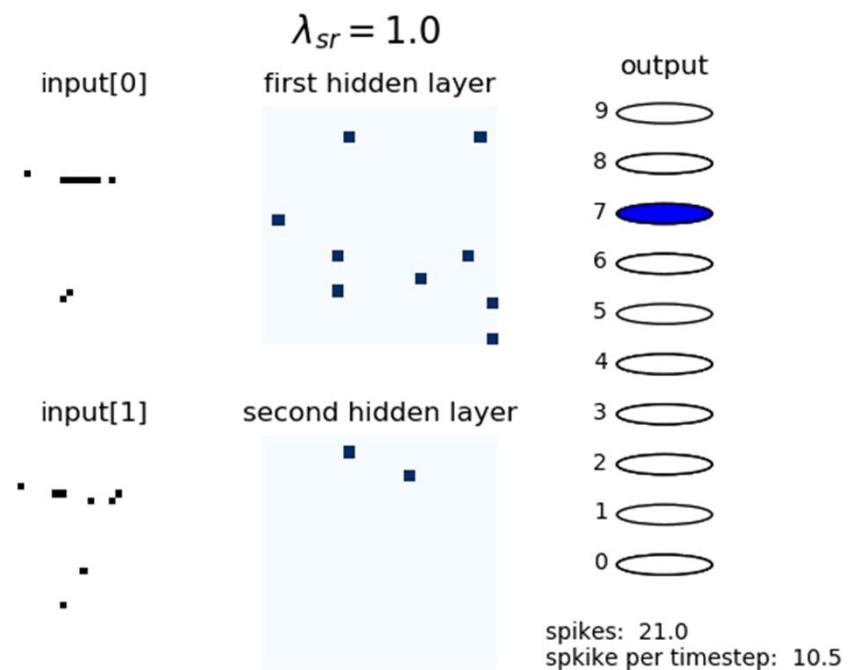
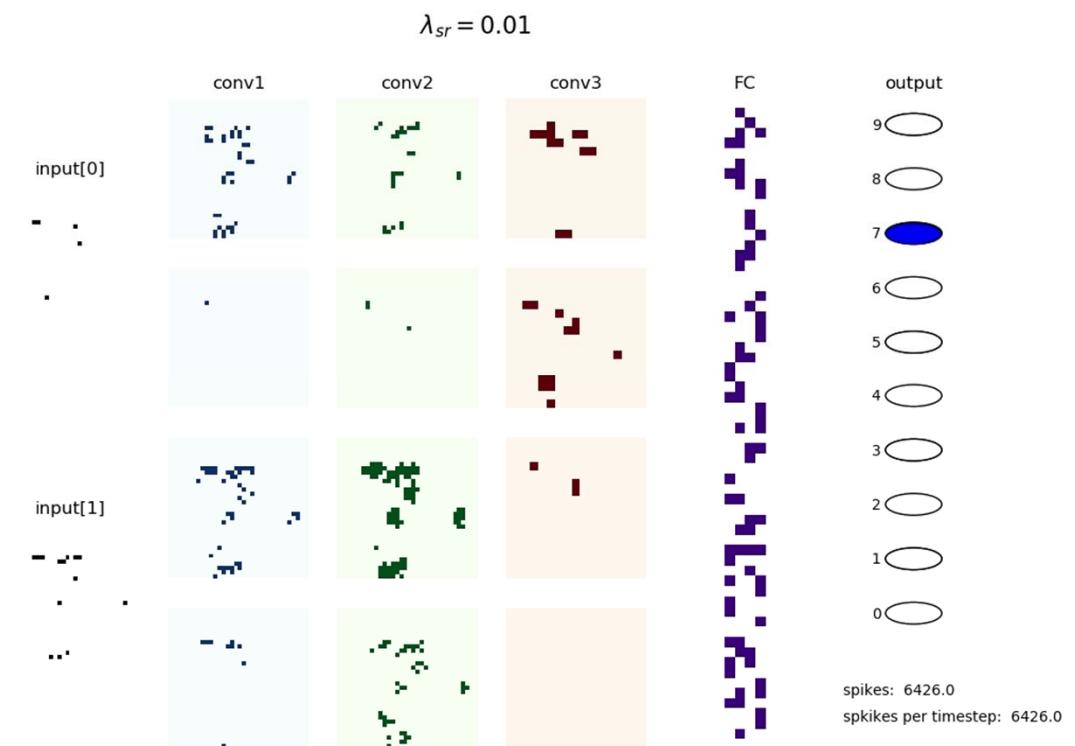


Illustration of Convolutional SNN

Implementation of spiking CNN for supervised N-MNIST digit classification

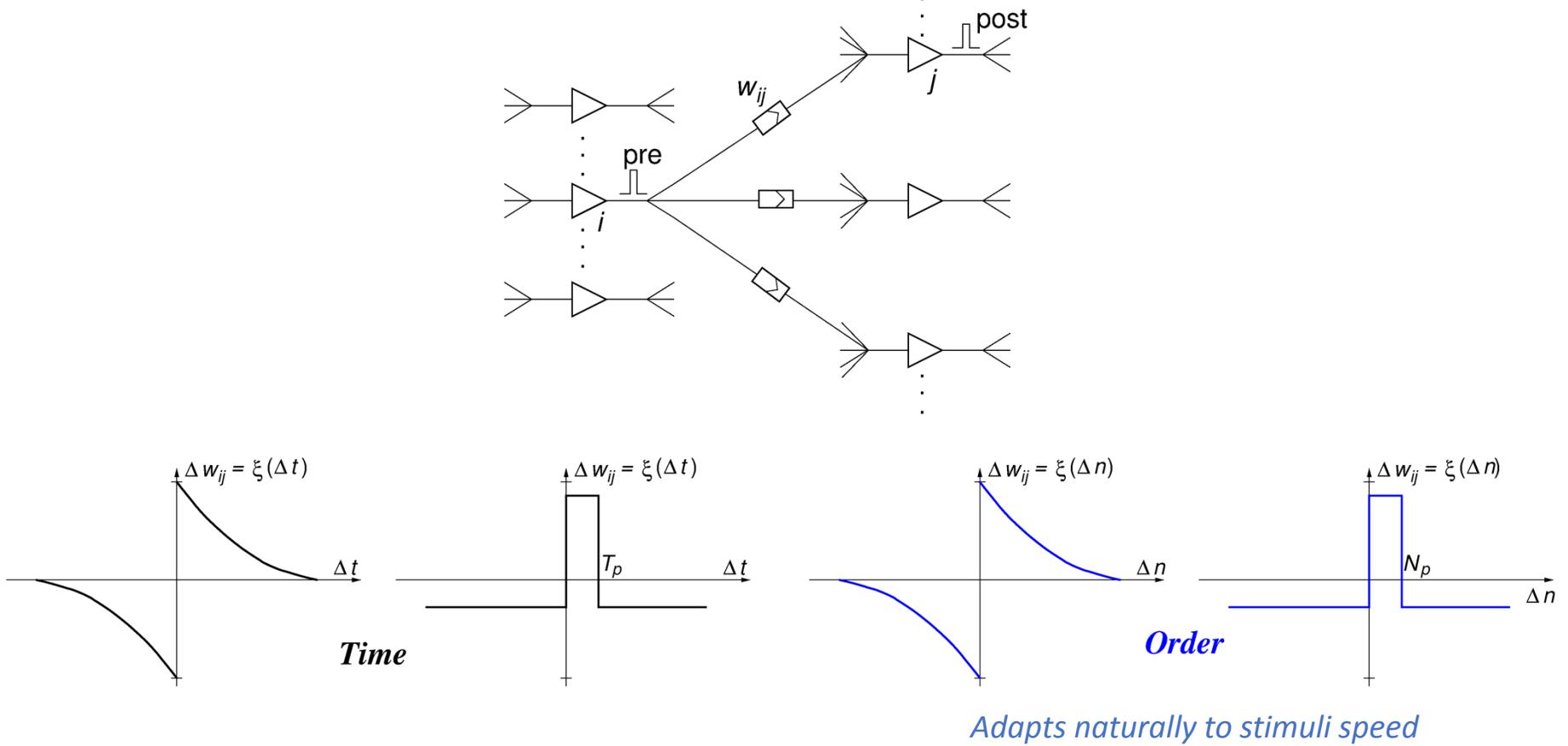
[Patiño-Saucedo et. Al., 2020]



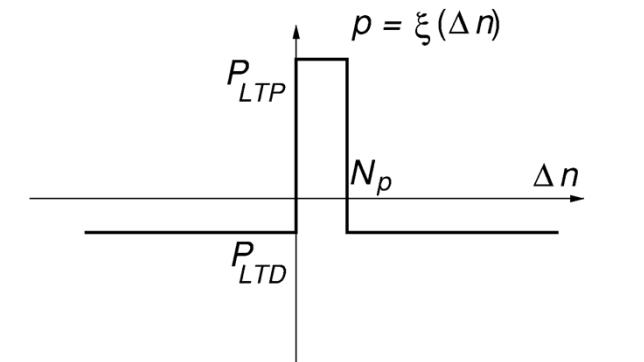
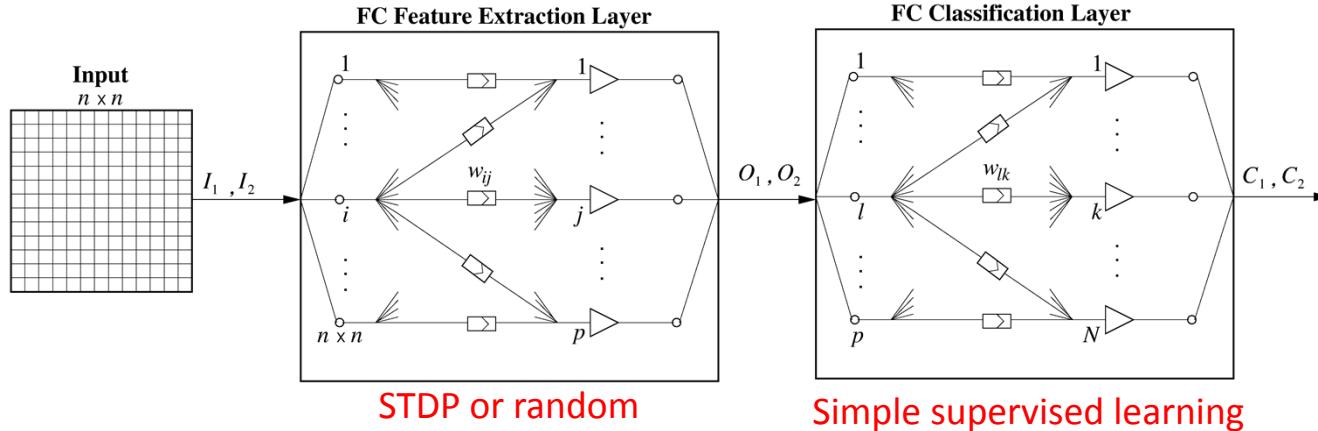
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STDP with arbitrary weights



1-bit weights stochastic STDP

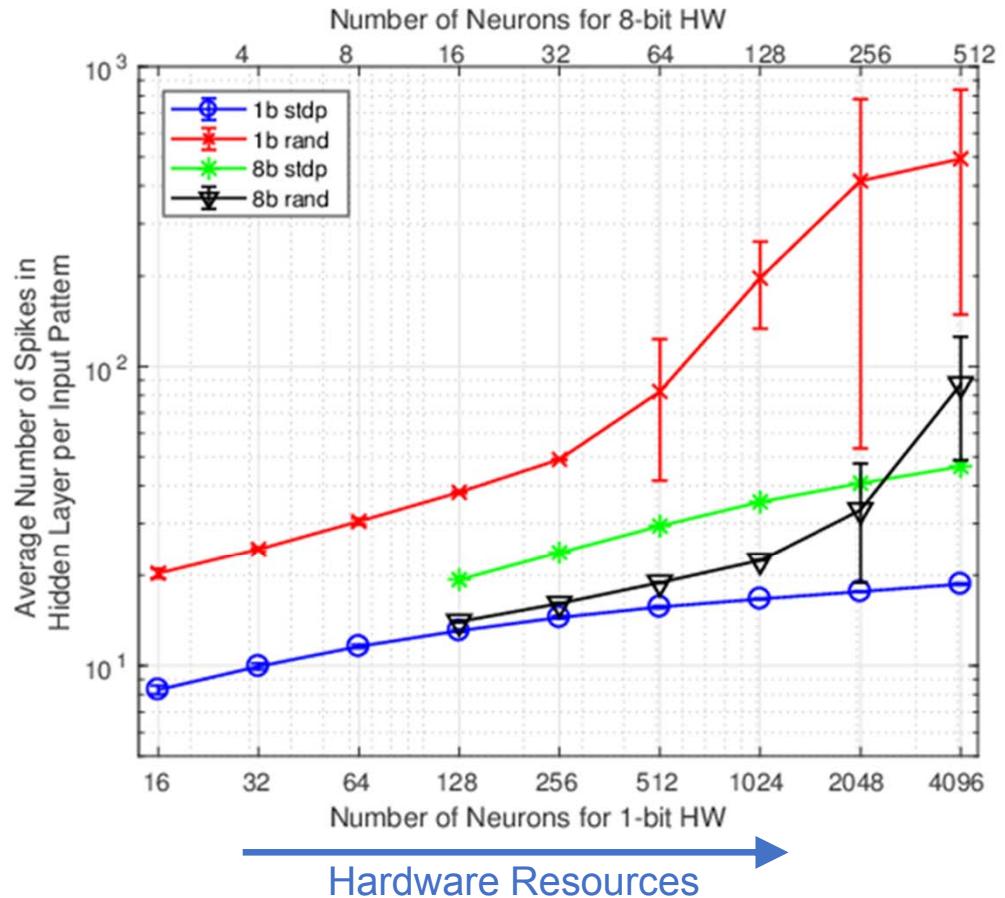
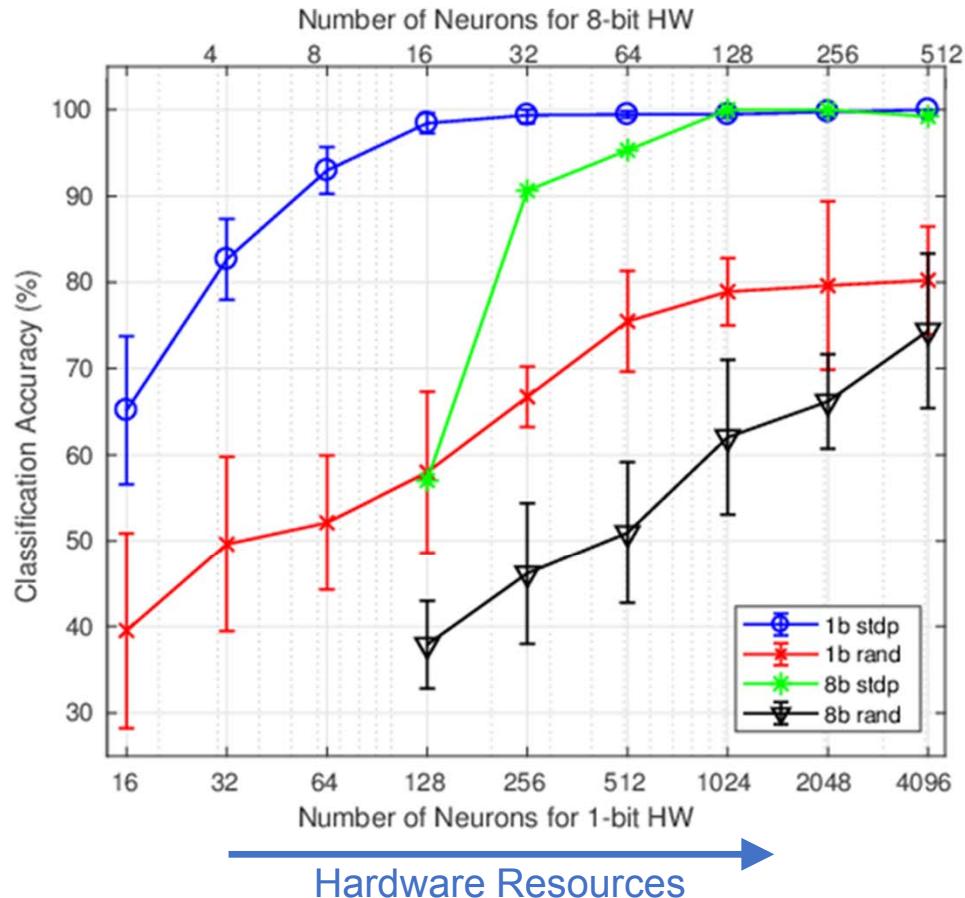


Test on FPGA (Spartan6)

Regularization techniques:

- **Homeostasis:** number of ‘1’ synapses connecting to output neuron is constant.
- **Double integrators,** each with own threshold: one for firing, one for learning.
- Each output neuron **increases threshold** after STDP update, to become more selective.
- Neuron **thresholds saturate** at a max value, and optionally may have leakage during learning.
- **Lateral inhibition** at destination neuron population, for competition.

Poker-DVS Dataset



[A. Yousefzadeh, "On Practical Issues for Stochastic STDP Hardware With 1-bit Synaptic Weights," *Front. Neuroscience*, 2018]²⁸

Conclusions

- Event-Driven Convolutions can be fast (pseudo-simultaneity)
- Filter out temporal and spatial noise
- Can do WTA and competition kernels
- Implemented on ASICs, FPGAs, and SpiNNaker
- Help for Stereo event-matching
- Efficient low-rate STBP on SpiNNaker with N-MNIST
- 1-bit weight stochastic STDP for lower resources HW with less spikes