上 海 交 通 大 学 试 卷（A 卷）

（2012 至 2013 学年 第 1 学期）

班级号_____ 学号_____ 姓名_____

课程名称 数字电子技术（期末） 成绩_____

PART I：True/Flase Write 'T' if the statement is true and 'F' if the statement is false.

1. A D flip-flop is constructed by connecting an inverter between the Set and Clock terminals of an S-R flip-flop. [ ]
2. The 555 timer has three basic operating modes: monostable, bistable, and astable. [ ]
3. A J-K flip-flop can be used as a divide-by-two frequency divider with an output duty cycle of 50%. [ ]
4. The term synchronous as applied to counter operations means that the counter is clocked so that each flip-flop in the counter is triggered at the same time. [ ]
5. Once an up/down counter begins its count sequence, it cannot be reversed. [ ]
6. In many cases counters must be strobed in order to eliminate glitches. [ ]
7. A serial-in serial-out shift register transfers data from one line of a parallel bus to another line one bit at a time. [ ]
8. An effective time delay device can be constructed by using the propagation delay characteristic of parallel shift registers. [ ]
9. An eight-bit D/A converter has a resolution of 0.125. [ ]
10. Most sequential circuits contain a combinational logic section and a memory section. [ ]

Part II: Multiple Choices (Choose the one alternative that best completes the statement or answers the question.)

1	2	3	4	5	6	7	8	9	10
11	12	13	14	15	16	17	18	19	20

我承诺，我将严格遵守考试纪律。

承诺人：

题号	Part I	Part II	Part III				
			1	2	3	4	5
得分							
批阅人(流水阅卷教师签名处)							

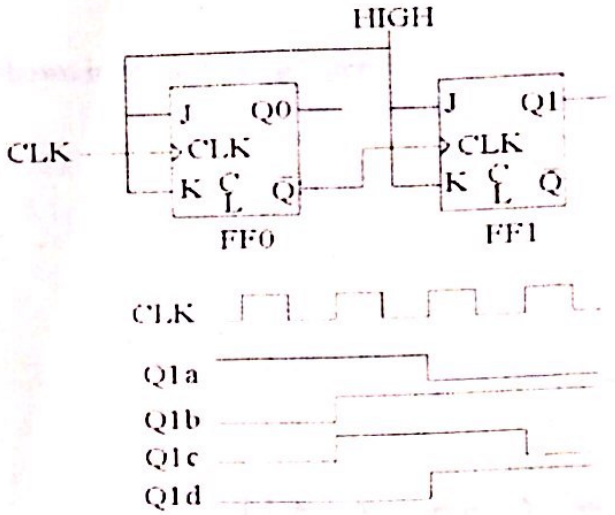
1. Which of the following is correct for a gated D latch?
   a. Q output follows the input D when the ENABLE is high.
   b. The output complement follows the input when enabled.
   c. The output toggles if one of the inputs is held high.
   d. Only one of the inputs can be high at a time.

2. Edge-triggered flip-flops must have _____.
   a. very fast response times
   b. a pulse transition detector
   c. at least two inputs to handle rising and falling edges
   d. active-low inputs and complemented outputs

3. Which of the following is not generally associated with flip-flops?
   a. Interval time
   b. Set-up time
   c. Hold time
   d. Propagation delay time

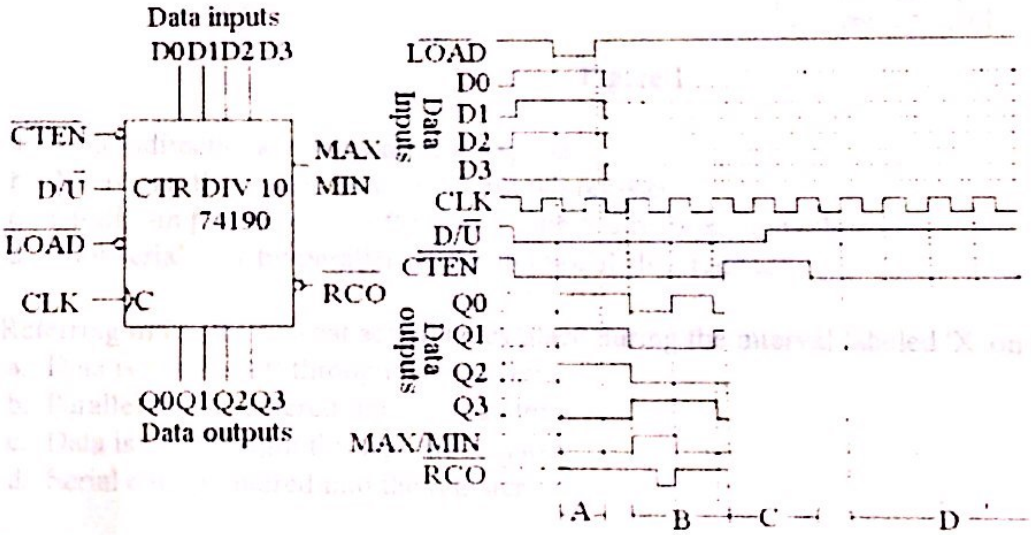
4. A retriggerable one-shot has a pulse width of 10ms. 3ms after being triggered, another trigger pulse is applied. The resulting output pulse will be _____ ms.
   a. 7
   b. 3
   c. 13
   d. 10

5. The counter shown below is a(n) _____ counter, and the correct output waveform for Q1 is _____.(The initial states of Q0 and Q1 are low.)



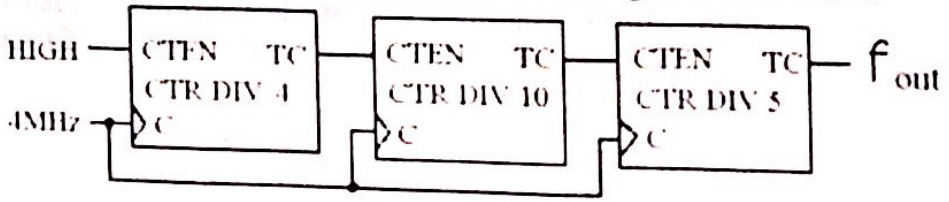
a. synchronous, Q1a
b. asynchronous, Q1b
c. asynchronous, Q1c
d. synchronous, Q1d

6. During period D on the timing diagram shown below, the decimal count sequence will be _____.



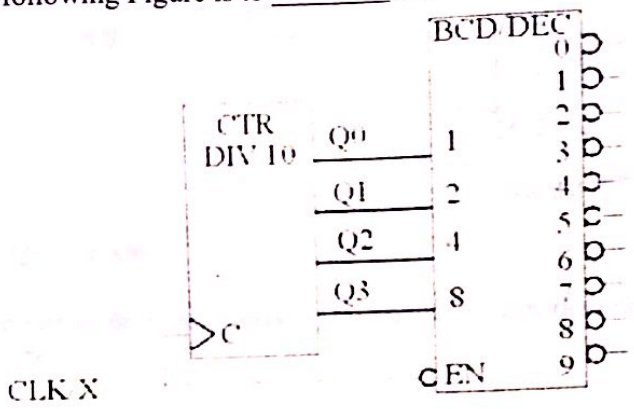
a. 8, 9, 0, 1
b. 0, 1, 9, 8
c. 7, 8, 9, 1
d. 1, 0, 9, 8

7. What is the output frequency of the counter in Figure shown below?



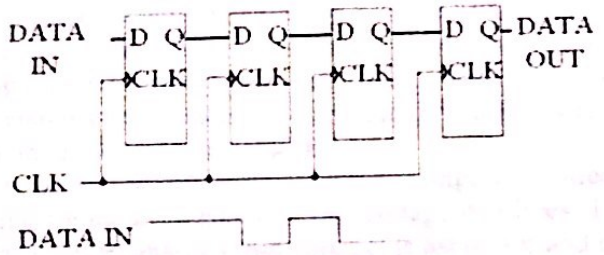
a. 210.5 kHz
b. 20 kHz
c. 800 Hz
d. 4 MHz

8. The purpose of the connection between 'C' of the 'CTR DIV 10' circuit and the 'EN' of the 'BCD/DEC' circuit in following Figure is to _____ and is referred to as _____.



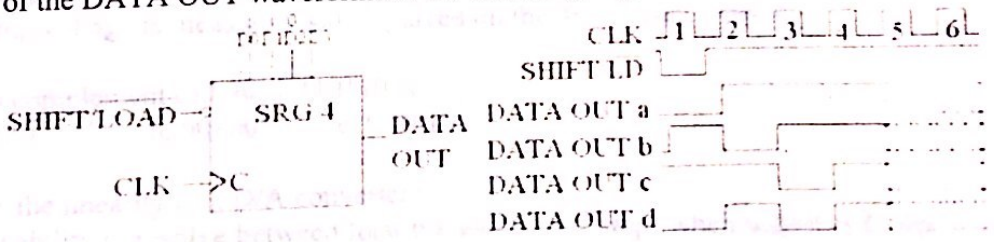
a. speed up the counter, strobing
b. clock the counter, strobing
c. reduce the number of inputs, enabling
d. eliminate glitches, strobing

9. How many clock cycles are required to enter the data into the register in the following Figure?



a. 31 b. 32 c. 4 d. 5

10. Which of the DATA OUT waveforms in the following Figure is correct?



a. DATA OUT d
b. DATA OUT c.
c. DATA OUT a.
d. DATA OUT b.

11. What type of device is shown in the following Figure?

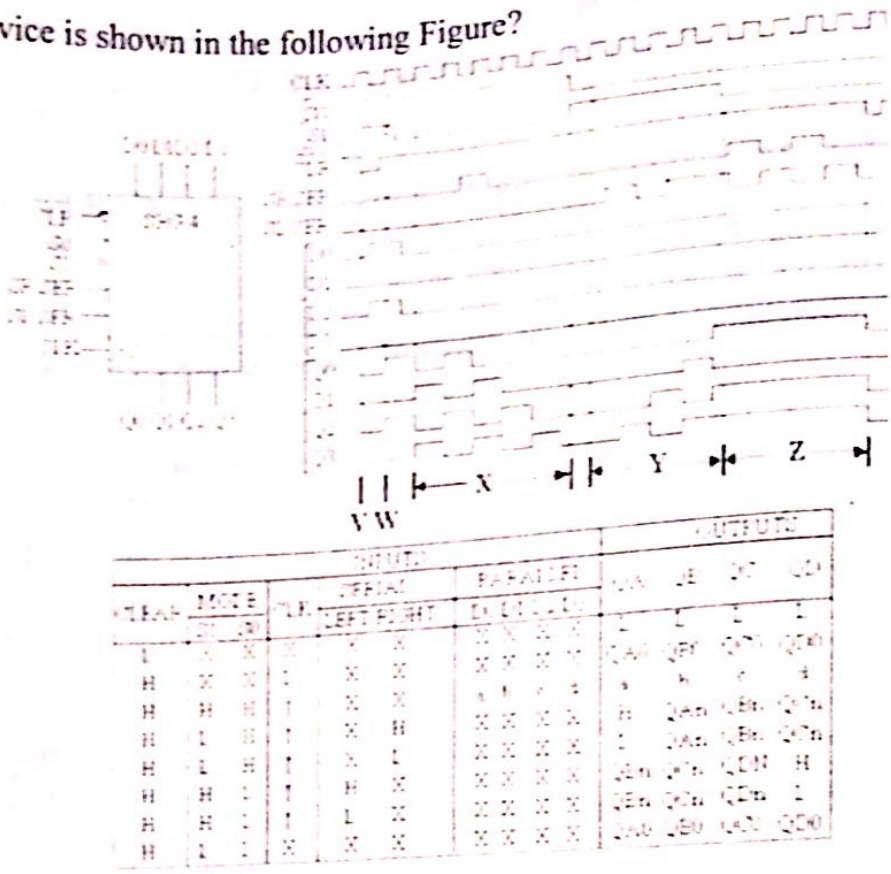


Figure 1

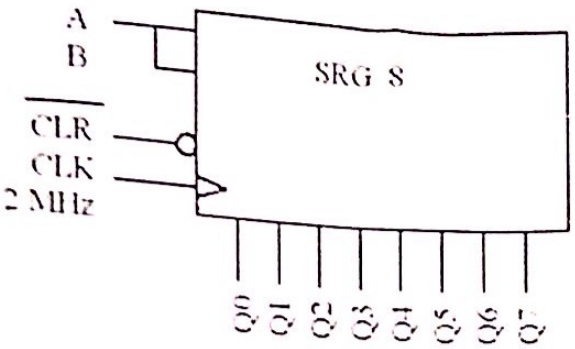
a. 4-bit bidirectional universal shift register
b. 2-way parallel-in serial-out bidirectional register
c. Parallel-in parallel-out shift register with bidirectional data flow
d. 2-bit serial-in 4-bit parallel-out bidirectional shift register

12. Referring to Figure 1, what action takes place during the interval labeled 'X' on the timing diagram?
a. Data is shifted left through the register.
b. Parallel data is entered into the register.
c. Data is shifted right through the register.
d. Serial data is entered into the register.

13. In order to use a shift register as a counter, _____.
a. serial-in serial-out register must be used.
b. the register's serial input is the counter input and the serial output is the counter output.
c. the serial output of the register is connected back to the serial input of the register.
d. the parallel inputs provide the input signal and the output signal is taken from the serial data output.

14. What is the modulus of a 6-stage Johnson counter?
a. 12 b. 64 c. 32 d. 6

15. A serial data path needs a 2000 ns delay. Which output from the circuit below will provide the correct delay?



(Data shifts from Q0 toward Q7)

a. Q7 b.Q3 c.Q1 d. Q0

16. What type of op-amp circuit does not typically have a feedback path connected between its output and either of its input pins?
   a. A comparator
   b. A current multiplier
   c. An open-loop amplifier
   d. An inverter

17. Which of the statements below best describes the basic operation of a dual-slope A/D converter?
   a. A ramp generator is used to enable a counter through a comparator. When the ramp voltage equals the input voltage the counter is latched and then reset. The counter reading is proportional to the input voltage since the ramp is changing at a constant V/second rate.
   b. Two ramps are generated: one by the input voltage and the other by a reference voltage. The input voltage ramp charges the integrating capacitor, while the reference voltage discharges the capacitor and enables the counter until the capacitor is discharged, at which time the counter value is loaded into the output latches.
   c. The input voltage is used to set the frequency of a voltage-controlled oscillator (VCO). The VCO quits changing frequency when the input voltage stabilizes. The frequency of the VCO, which is proportional to the analog input voltage, is measured and is displayed on the digital display as a voltage reading.
   d. A ramp voltage and analog input voltage are applied to a comparator. As the input voltage causes the integrating capacitor to charge, it will at some point equal the ramp voltage. The ramp voltage is measured and displayed on the digital panel meter.

18. The 2's complement of binary 110110 is _____.
   a. 110100 b. 001001 c. 001010 d. 101010

19. What is the linearity of a D/A converter?
   a. The ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.
   b. It is the reciprocal of the number of discrete steps in the D/A output.
   c. It is the comparison between the actual output of the converter and its expected output.
   d. It is the deviation between the ideal straight-line output and the actual output of the converter.

20. How many gates, including inverters, are required to implement the equation, $X = AC\overline{D} + A\overline{B}(CD + BC)$, after simplification with Boolean algebra?

a. 3 b. 5 c. 7 d. 9

Part III: SHORT ANSWER. Write the word, phrase or draw a block diagram that best completes each statement or answers the question.

1. There are 4 decoders and two OR gates. The inputs number of each OR gate is less than 8. Using the decoders and OR gates to implement the following two functions expressed in Karnaugh map. (Hint: implement the four min-terms in a same row/column with a single output of a decoder)

cd \ ab	00	01	11	10
00	1			1
01	1			1
11	1	1		1
10	1			

f

cd \ ab	00	01	11	10
00	1	1		1
01		1		1
11		1		
10	1	1		1

g

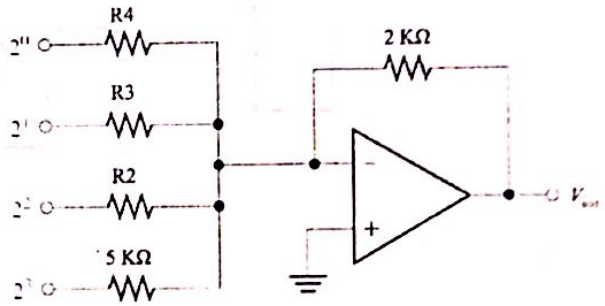
Decoder's truth table:

EN	a	b	0	1	2	3
0	x	x	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

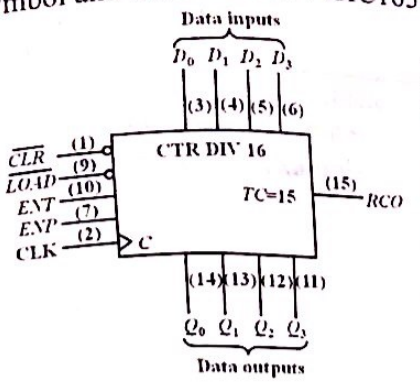
2. For the Binary-Weighted-Input Digital to Analog Converter (DAC) in the figure, please answer the questions below.

(a) Please determine the ideal resistance values for the resistors R2 ~ R4 in the DAC in the following figure.

(b) Now suppose the actual resistance values of R2 ~ R4 are 10% higher than the ideal values, respectively. Please determine the output voltage (in volts) and the conversion error (in percentage) as compared with an DAC with ideal R2 ~ R4 resistance values, when the digital input is $(1011)_2$ and input voltages are ideal (5V for HIGH and 0V for LOW).

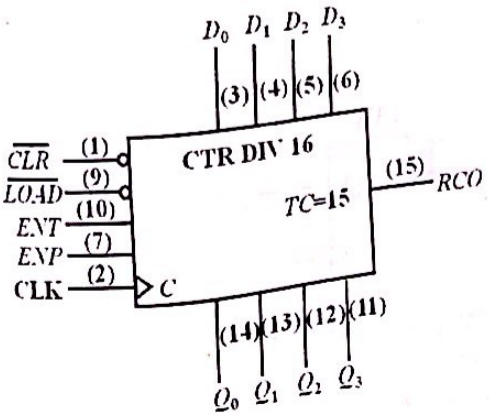


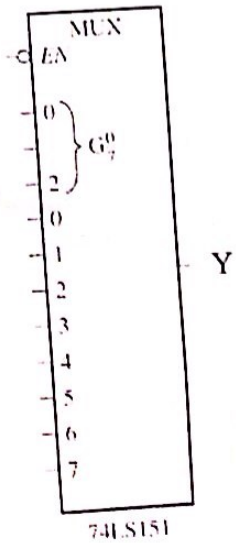
3. Design a serial signal (Y=1011100110) generator by using one 74HC163 counter and a 1 of 8 data selector.
The logic symbol and truth table of 74HC163 are as following:



Operating Mode	$\overline{CLR}$	CLK	ENP	ENT	$\overline{LOAD}$	D	Q	RCO
Reset (Clear)	0	↑	X	X	X	X	0	0
Parallel load	1	↑	X	X	0	D	D	0
Count	1	↑	1	1	1	X	Count	†
Inhibit	1	X	0	X	1	X	Q	†
	1	X	X	0	1	X	Q	0

† The RCO output is 1 when ENT is 1 and the counter is at TC (1111)
The High-to-Low transition of ENP and ENT should only occur while CLK is HIGH for conventional operation.
The Low-to-High transition of $\overline{CLR}$ and $\overline{LOAD}$ should only occur while CLK is HIGH for conventional operation.

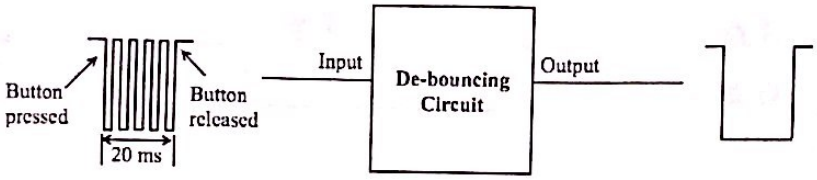


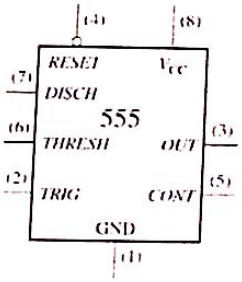


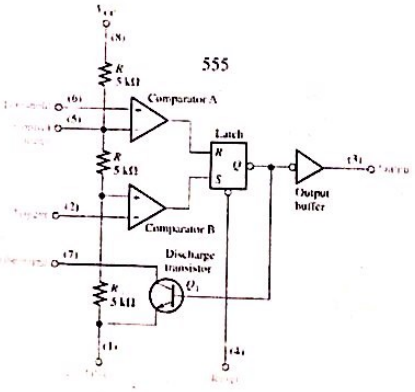
4. When a push button is pressed or released, the contacts will bounce between the *on* and *off* states for a fraction of a second. Because of this, the output from a push button must be *de-bounced* before it can be used by other digital circuits. The figure below illustrates the output from a button press. Please answer the following questions.

(a) Explain why and how a 555 timer can be used as a de-bouncing circuit;

(b) Assume the resistance value of all resistors is 10KΩ. Draw the de-bouncing circuit with proper capacitor values in the 555 timer below.



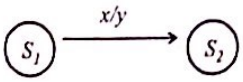




5. Design a serial detector which can detect the 1101 appeared, by using two edge triggered J-K Flip Flops. The detector has one input and one output.
The following is an example of the relationship between the input and output.

Input x	0	0	1	1	0	1	1	0	1	0	1
Output y	0	0	0	0	0	1	0	0	1	0	0

(a) Draw the state diagram of the detector.
(Hint: the state diagram has 4 states. And denote state transitions with input x and output y as the example shown on the right.)



(b) Implement the circuit.