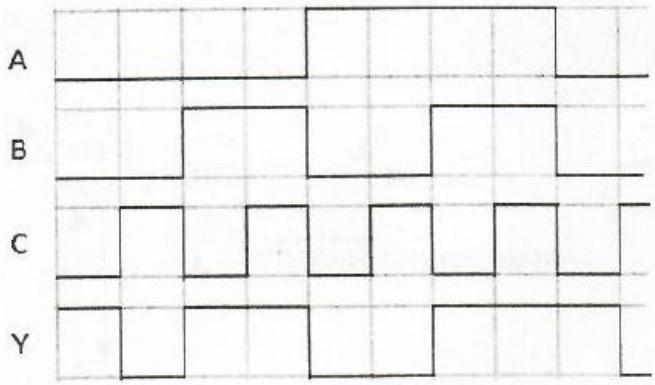
2011-2012

1. (10%) Use the minimum number of gates to implement a circuit that detects if a 4-bit binary number $A_3A_2A_1A_0$ is greater than 9. When the number is greater than 9, the output $Y=1$; otherwise $Y=0$.

2. (10%) Find the minimum POS form for the following expression

$$Y=\overline{(A\oplus B)\overline{B}(\overline{A}B\overline{C}\overline{D}+\overline{A}C\overline{D})}$$

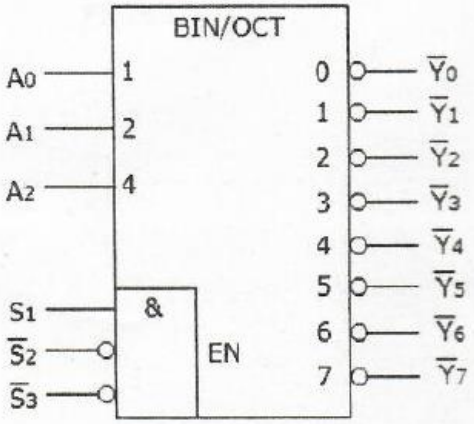
3. (15%) Use one 3-line-to-8-line decoder 74LS138 and one NAND gate to implement a circuit whose output Y and inputs A, B, and C are related as shown in Figure 1.



(a) Waveforms for the desired circuit

INPUTS					OUTPUTS							
S_1	$\overline{S_2}+\overline{S_3}$	A_2	A_1	A_0	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
0	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

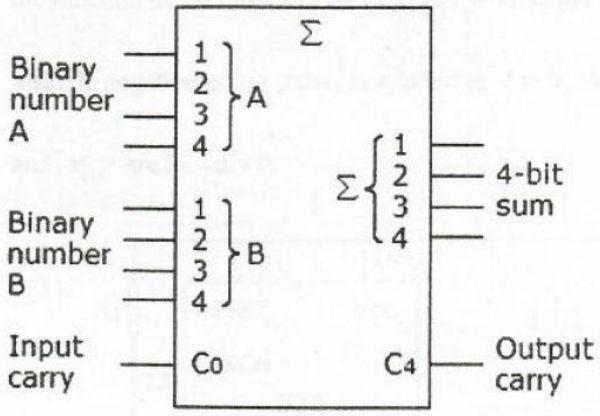
(b) Function Table for 74LS138



(c) Logic symbol for 74LS138

Figure 1

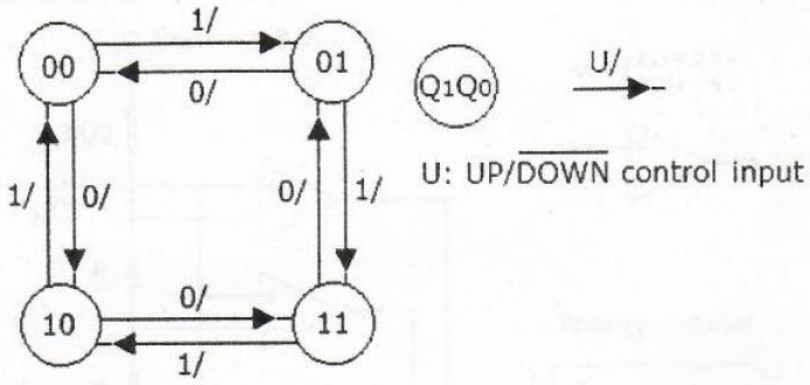
4. (10%) Use 4-bit adders to implement a circuit which adds up two 11-bit numbers. Label all critical inputs and outputs.



A 4-bit adder

Figure 2

5. (15%) Use J-K flip-flops and the minimum number of gates to implement a synchronous 2-bit up/down counter with a Gray code sequence. The counter should count up when an $\overline{\text{UP/DOWN}}$ control input is 1 and count down when the control input is 0.



State diagram for a 2-bit Gray code counter

Figure 3

6. (15%) In Figure 4, $R_1 = 150\ \text{k}\Omega$, $R_2 = R_3 = 24\ \text{k}\Omega$, $C_1 = 0.033\ \mu\text{F}$, $C_2 = C_3 = C_4 = 0.01\ \mu\text{F}$. (1) What is the function of the circuit in block I? (2) What is the function of the circuit in block 2? (3) Suppose that the input v_{IN}, a single negative-going pulse, is applied at $t = 0$, sketch the waveforms v_{O1}, v_{O2}, and v_O. Suppose that both v_{O1} and v_{O2} are initially 0.

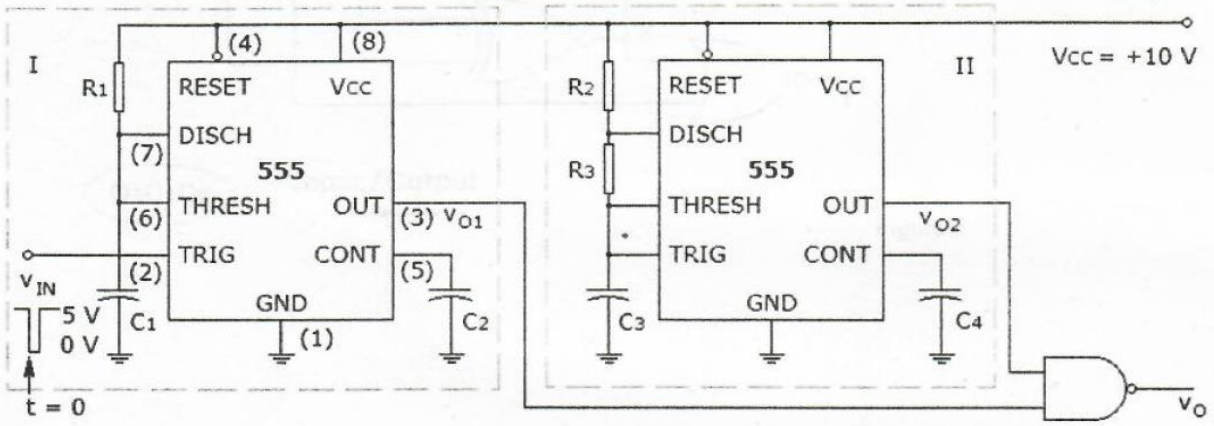


Figure 4

7. (15%) The input to the circuit in Figure 5 is $v_{IN}(t) = 4 + 4\sin(100\pi t)$ V, $0 \le t \le 20$ ms. The sampling signal has a frequency of 400 Hz. Determine the binary code sequence $D_2D_1D_0$ and the output $v_{OUT}(t)$ for $0 \le t \le 20$ ms.

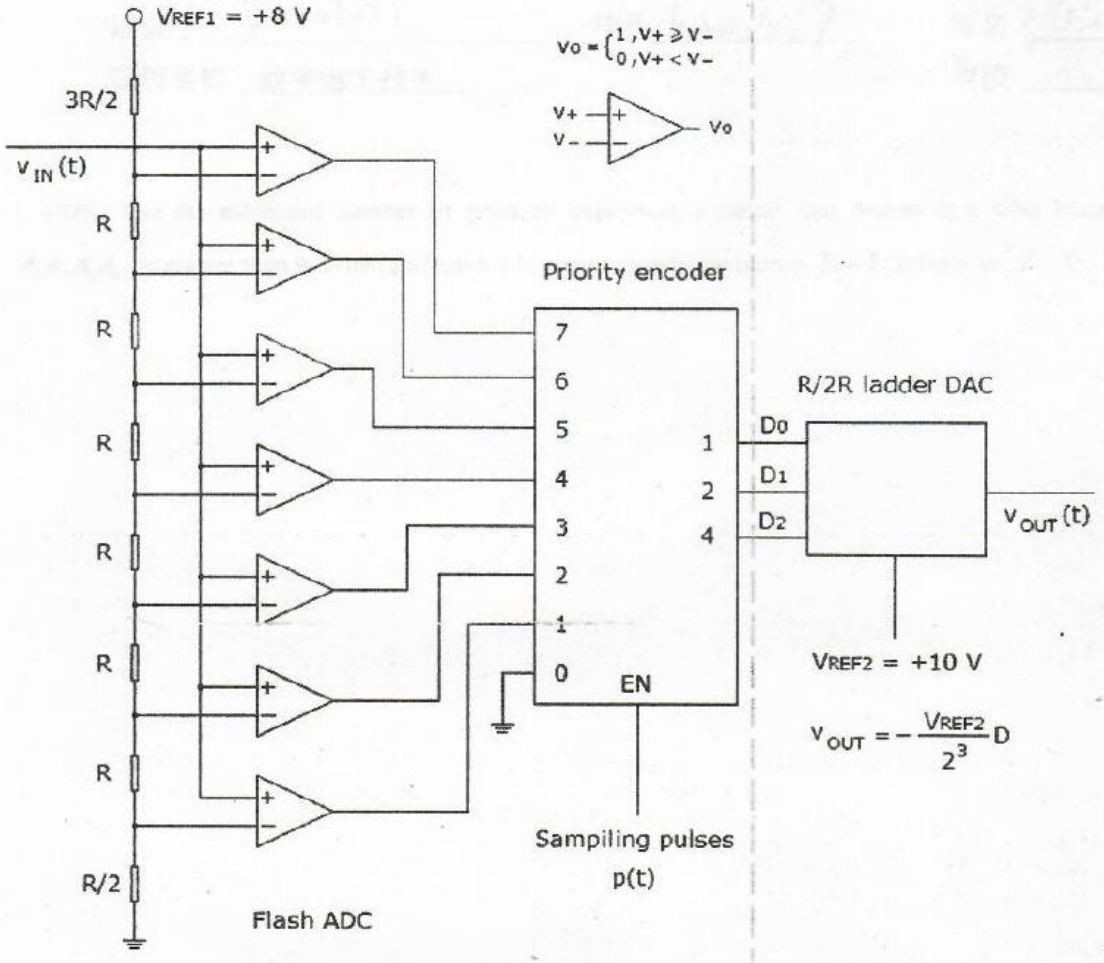


Figure 5

8. (10%) Draw the state diagram for the circuit in Figure 6. Y is the output of the circuit.

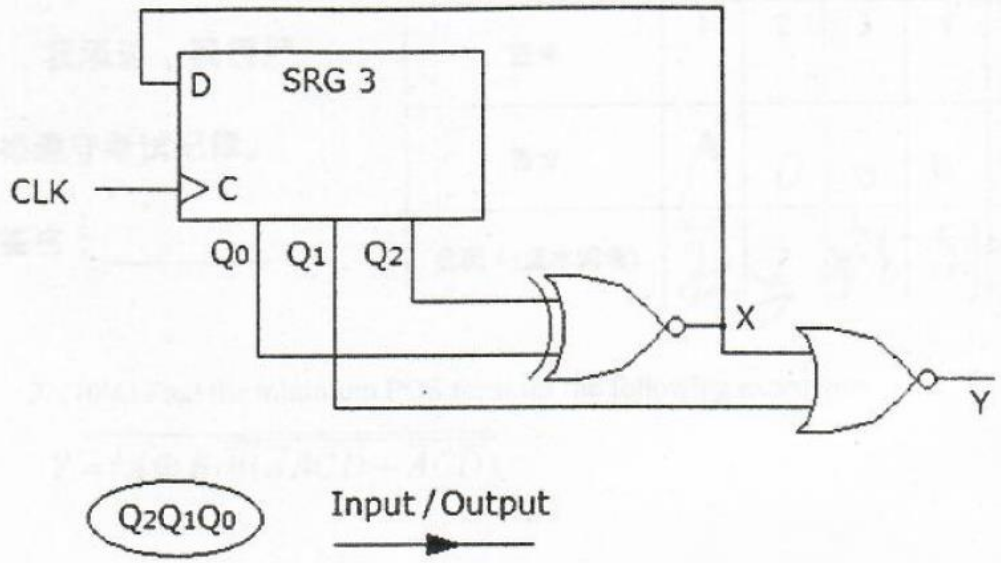


Figure 6

2015-2016

(I) True/False (20′)

1. ( ) It is possible to have an overlap between high and low levels in digital logic .

2. ( ) Full-adders cannot be used as a BCD-to-binary converter .

3. ( ) The XNOR gate will produce a high output if only one but not both of the input is HIGH .

4. ( ) NAND gates can be used to construct NOR gates .

5. ( ) The effect of an inverted output being connected to the inverting input of another gate is to effectively eliminate one of the inversions, resulting in a single inversion .

6. ( ) The BCD equivalent of 73 is 01001001 .

7. ( ) A D flip-flop is constructed by connecting an inverter between the Set and Clock terminals .

8. ( ) A J-K flip-flop associated waveforms are shown in Figl-1, the circuit is operating properly

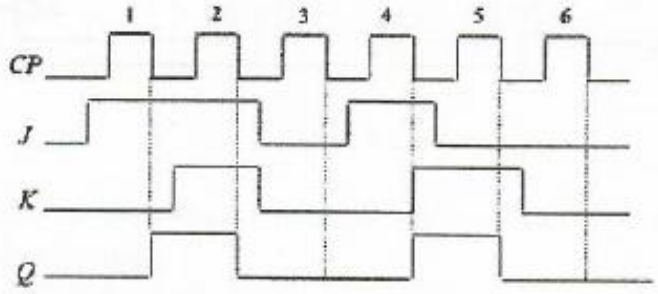


Fig 1-1

9. ( ) A 4-bit stairstep-ramp A/D converter has a clock frequency of 1000Khz and maximum input voltage 5V. The minimum sample rate will be 6250 samples/second.

10. ( ) A 8-bit D/A converter has a resolution of 0.0125 .

（二）. Choice

1. Which of the following is correct for full-adders ( )
(A) Full-adders have the capability of directly adding decimal numbers
(B) In a parallel full-adder, the first stage may be a half-adder
(C) Full-adders are limited to two inputs, since there are only two binary digits
(D) Full-adders are used to make half-adders

2. Using 4 bit adders to create a 32 bit adder ( )
(A) requires 32 adders
(B) requires 8 adders
(C) requires the carry out of the less significant adder to be connected to the carry in of the next significant adder
(D) both (B) and (C)

3. What type of device is shown in Fig 2-1, and what inputs (A3, A2, A1, A0) are required to produce the output levels as shown ( )

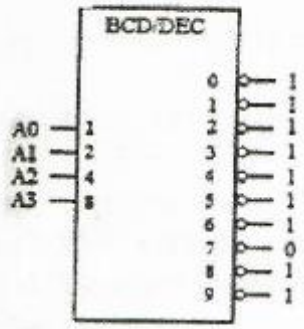


Fig 2-1

(A) A decimal to binary-coded-decimal encoder; 1, 1, 1, 0
(B) A binary-to-decimal encoder; 0, 1, 1, 1
(C) A binary-coded-decimal to decimal decoder; 1, 0, 0, 0
(D) A decimal to binary-coded-decimal encoder; 0, 0, 0, 1
(E) others

E 选项为 others

4. For the input values(A0-A3, B0-B3)given for Fig 2-2, what will be indicated on the display? 74139 is a 1-of-4 decoder ( )

(A) Data Select=1, B=6; Data Select=0, A=3

(B) Data Select=1, A=6; Data Select=0, B=3

(C) Data Select=1, A=3; Data Select=0, B=6

(D) Data Select=1, B=3; Data Select=0, A=6

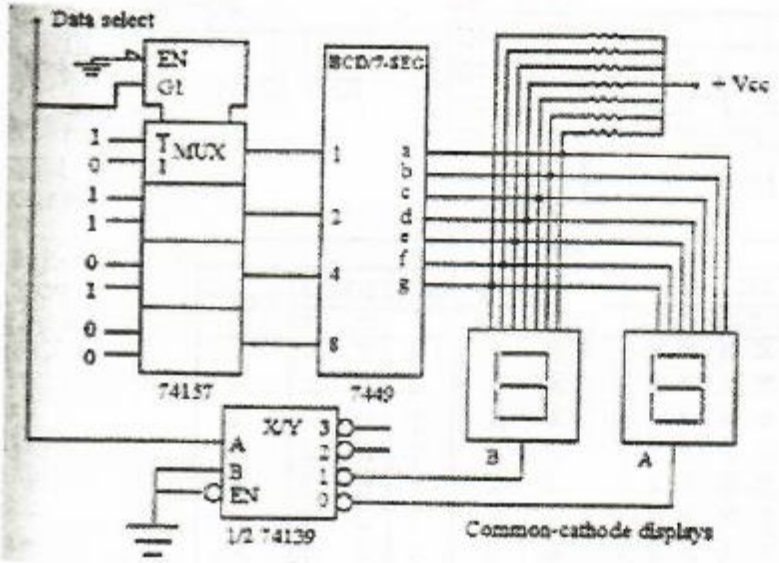


Fig 2-2

5. What is the frequency of the F_{out} in Fig 2-3 ( ) .

(A) 800Khz

(B) 20Khz

(C) 200Khz

(D) 10Khz

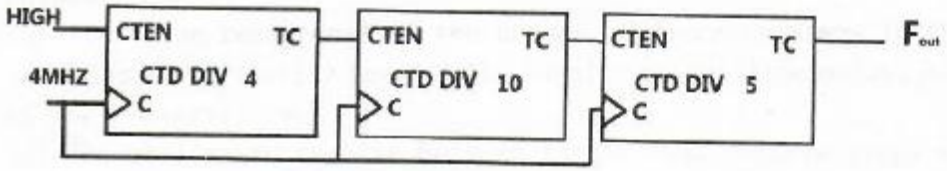


Fig 2-3

6. Which of the example below express the distributive law? ( ) .

(A) A(B+C)=AB+AC

(B) (A+B)+C=A+(B+C)

(C) A+(B+C)=AB+AC

(D) A(BC)=(AB)+C

7. The circuit shown in Fig 2-4 is a/an ( ) .

(A) 4-bit magnitude comparator

(B) 4-bit half adder

(C) 8-bit comparator

(D) 8-bit binary adder

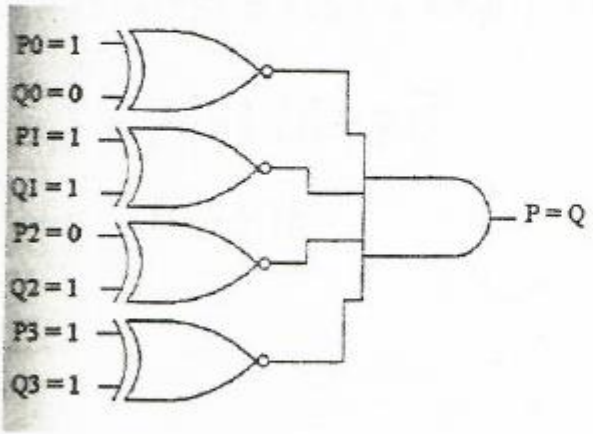


Fig 2-4

8. The state diagram of counter is Fig 2-5, The capacity of the counter is ( ) .

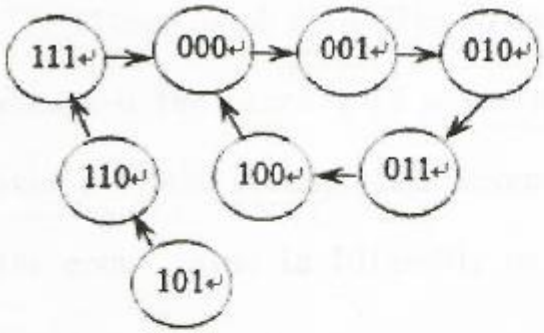


Fig 2-5

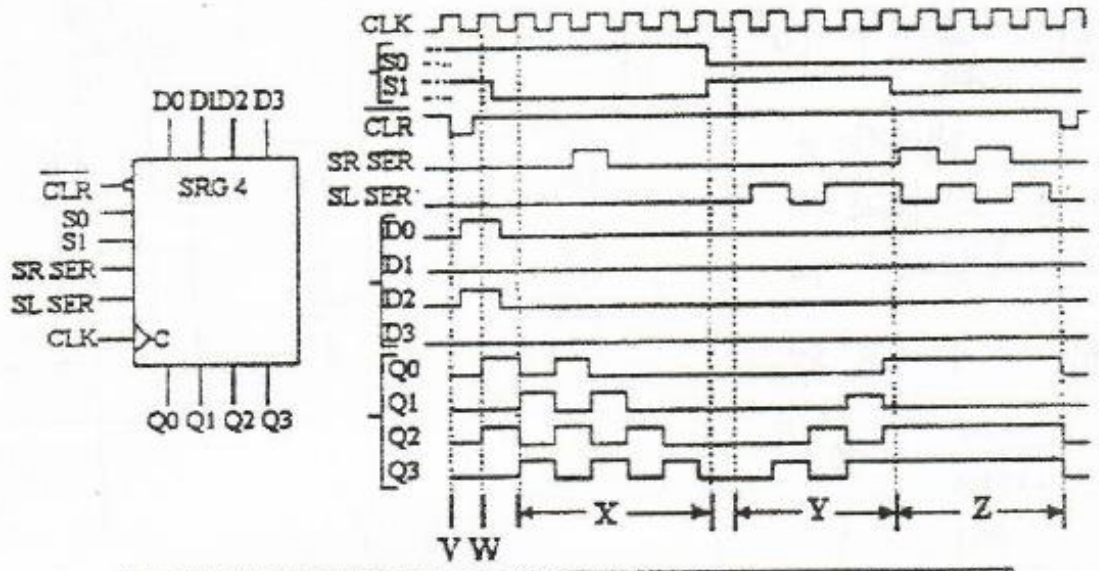
(A) 4 (B) 5 (C) 6 (D) 8

9. Referring to the function table in Fig 2-6, taking the CLEAR , S1 and S0 inputs all HIGH will do what? ( ) .

(A) The exact response will depend on what values are loaded into the parallel data inputs

(B) It will cause the parallel data inputs to be loaded and passed to the parallel data outputs (C) It will reset the parallel registers and inhibit the serial data inputs

(D) It will inhibit the operation of the register



INPUTS									OUTPUTS			
CLEAR	MODE		CLK	SERIAL		PARALLEL			QA	QB	QC	QC
	S1	S0		LEFT	RIGHT	D0	D1	D2 D3				
L	X	X	X	X	X	X	X	X X	L	L	L	L
H	X	X	L	X	X	X	X	X X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c d	a	b	c	d
H	L	H	↑	X	H	X	X	X X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X X	QBn	QCn	QDN	H
H	H	L	↑	L	X	X	X	X X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X X	QA0	QB0	QC0	QD0

F

Fig 2-6

10. What is the accuracy of D/A converter? ( )

(A) It is the comparison between the actual output of the converter and its expected output

(B) It is the reciprocal of the number of discrete steps in the D/A output

(C) It is the deviation between the ideal straight-line output and the actual output of the converter

(D) The ability to resolve between forward and reserve steps when sequenced over its entire range of inputs

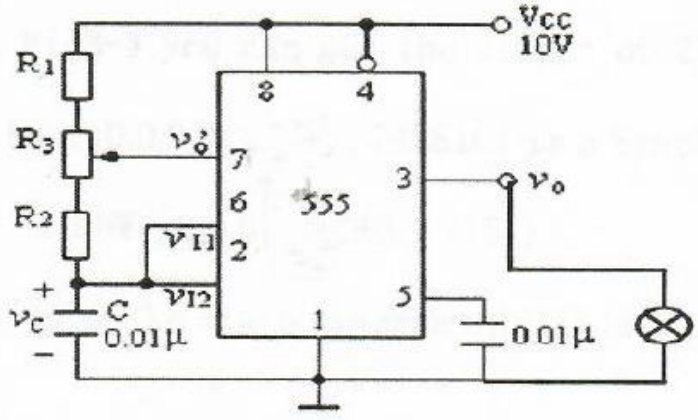
(三). **Problems**

一) Using Algebra method to simplify the function. (10′)

$$F = XZ + \bar{Y}Z + Y\bar{Q} + Z\bar{Q}C + Z\bar{Q}\,\bar{C} + X(Y + \bar{Z}) + \bar{X}YZ\bar{Q} + X\bar{Y}QC$$

二）Please use D flip-flop to design a synchronization timing circuit, when x=0, the circuit is a sextuple denotation counter(6 进制计数器); when x=1, the circuit is a Seven binary counter(7 进制计数器), and when the count value is 101(x=0), or 110(x=1), the output carry is Z= 1.

三）A 555 timer is connected for a stable operation as shown in Fig3-1, Determine the waveform of u_o (When u_o is HIGH, its voltage is 5V) and u_c, The resistance of the bulb is 5 Ohm R1=R3=10K ohm. IF I want the power of bulb is 3~3.75W . Please give the value of R2 and the frequency of u_o. (10′)



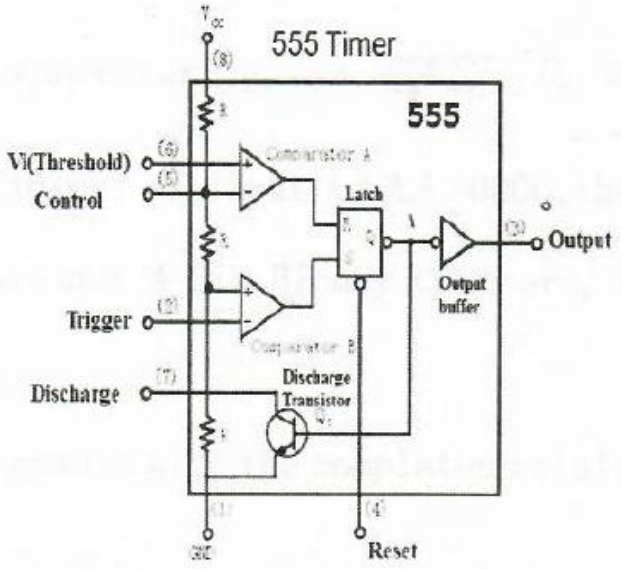


Fig 3-1

四）Analyse the circuit, determine the output waveform。(15′)

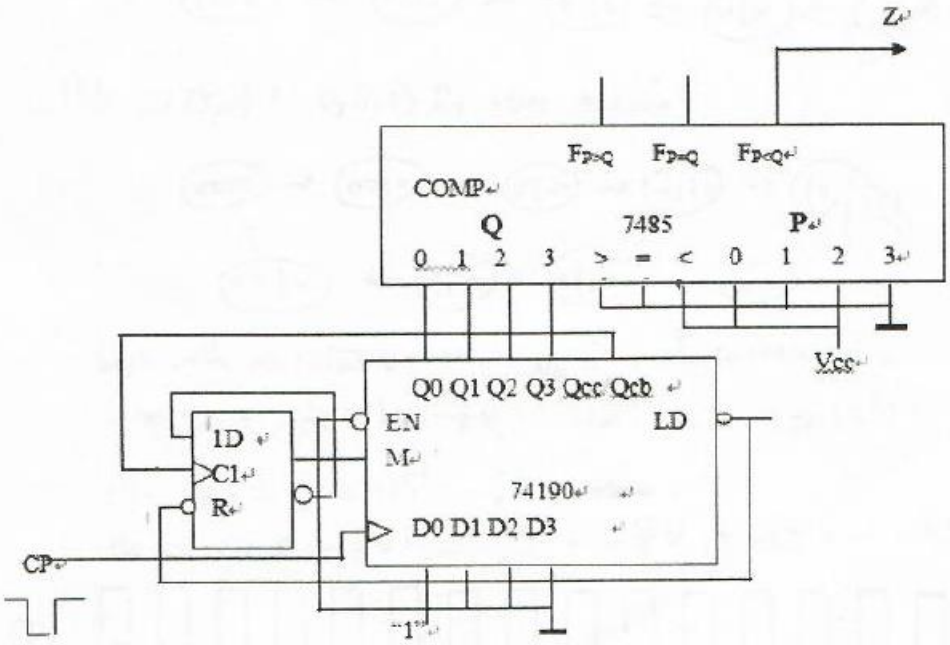


Fig 3-2

74190

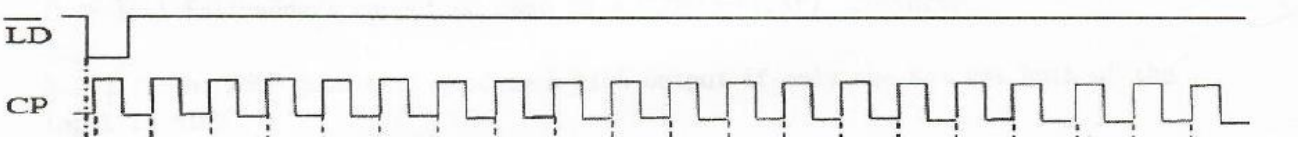
$\overline{EN}$	$\overline{LD}$	M	CP	D0	D1	D2	D3	Q0	Q1	Q2	Q3
×	0	×	×	a	b	c	d	a	b	c	d
0	1	0	↑	×	×	×	×	递增计数			
0	1	1	↑	×	×	×	×	递减计数			
1	1	×	×	×	×	×	×	保持			

$Qcc/Qcb = \overline{M}\ Q3\ \overline{Q2}\ \overline{Q1}\ Q0 + M\ \overline{Q3}\ \overline{Q2}\ \overline{Q1}\ \overline{Q0}$

Q3—Most Significant Bit ; Q0—Least Significant Bit

7485

A3	B3	A2	B2	A1	B1	A0	B0	A>B	A=B	A<B	$F_{P>Q}$	$F_{P=Q}$	$F_{P<Q}$
0	1	×	×	×	×	×	×	×	×	×	0	0	1
1	0	×	×	×	×	×	×	×	×	×	1	0	0
A3=B3		0	1	×	×	×	×	×	×	×	0	0	1
A3=B3		1	0	×	×	×	×	×	×	×	1	0	0
A3=B3		A2=B2		0	1	×	×	×	×	×	0	0	1
A3=B3		A2=B2		1	0	×	×	×	×	×	1	0	0
A3=B3		A2=B2		A1=B1		0	1	×	×	×	0	0	1
A3=B3		A2=B2		A1=B1		1	0	×	×	×	1	0	0
A3=B3		A2=B2		A1=B1		A0=B0		1	0	0	1	0	0
A3=B3		A2=B2		A1=B1		A0=B0		0	1	0	0	1	0
A3=B3		A2=B2		A1=B1		A0=B0		0	0	1	0	0	1



波形图包含 **Q0、Q1、Q2、Q3、Qcc/QcB、M、Z**

五) In Fig3-3 , AD7254 is a 8-bit D/A converter, $\mu_0 = -\frac{U_{REF}}{2^8}\sum_{i=0}^{7} D_i \cdot 2^i$。

in Fig3-4 you can get the output of 2716(eg: if input $A_3A_2A_1A_0$=0000; then output:$D_3D_2D_1D_0$=0000), 74LS161 is a Synchronous 4-Bit Binary Counters, IF L_D is LOW , $Q_DQ_CQ_BQ_A$=DCBA. (15')

(1) Draw the state diagram of 74LS161, you must give the completes results

(2) Determine the μ_0 waveform for CP (This signal is clock)

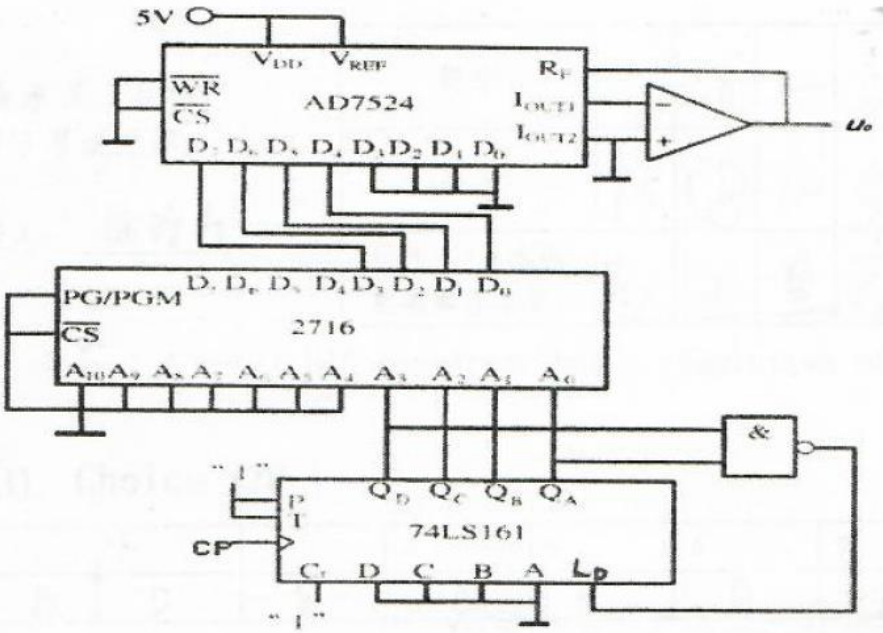


Fig 3-3

地址				数据			
A_3	A_2	A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	0
0	1	1	0	0	1	1	0
0	1	1	1	0	1	0	0
1	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	1	0
1	1	0	1	0	1	0	0
1	1	1	0	0	0	1	0
1	1	1	1	0	1	0	0

Fig 3-4