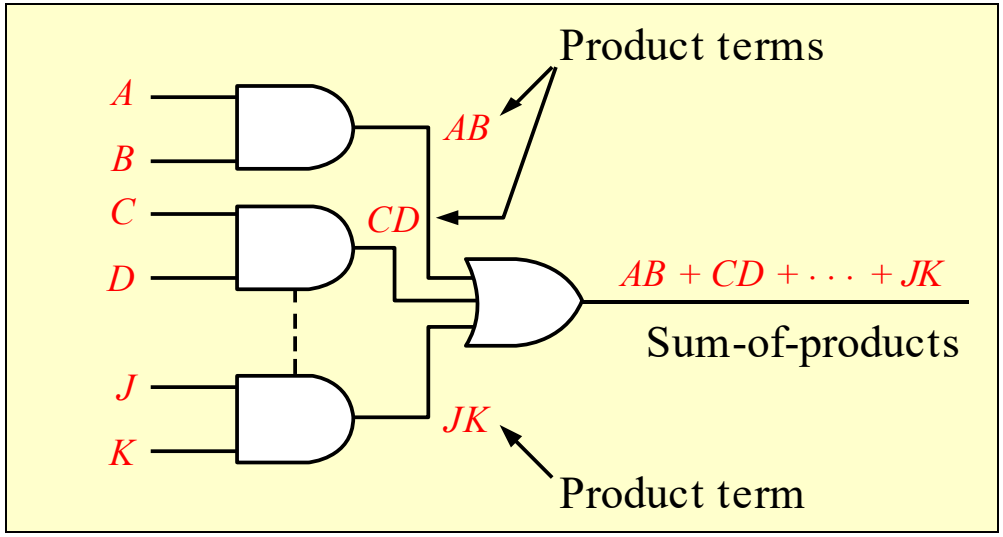
Chapter 5: Combinational Logic Analysis

- **Objectives**
  - Analysis of combinational logic
  - Implementation of combinational logic
  - NAND/NOR universal gates and applications
  - OC gates/Tri-state gates
  - Driving and noise margin

- **Reading assignment**
  - Read chapter 5 and chapter 15 in the text

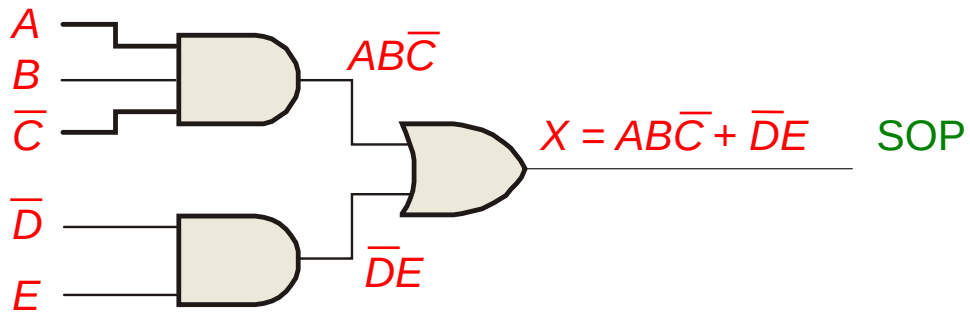
Combinational Logic Circuits

In Sum-of-Products (SOP) form, basic combinational circuits can be directly implemented with AND-OR combinations if the necessary complement terms are available.



Combinational Logic Circuits

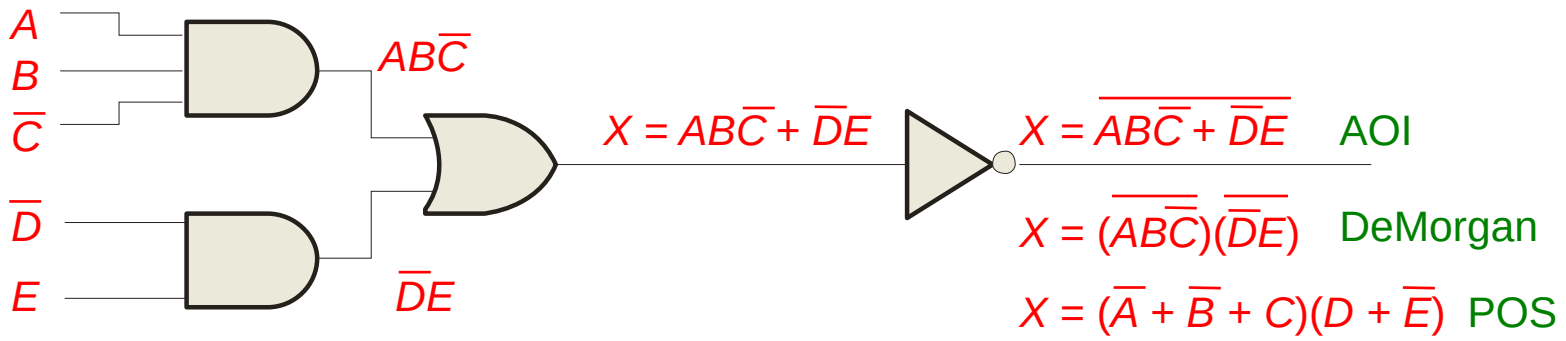
An example of an SOP implementation is shown. The SOP expression is an AND-OR combination of the input variables and the appropriate complements.



Combinational Logic Circuits

When the output of a SOP form is inverted, the circuit is called an AND-OR-Invert circuit. The AOI configuration lends itself to product-of-sums (POS) implementation.

An example of an AOI implementation is shown. The output expression can be changed to a POS expression by applying DeMorgan's theorem twice.



Exclusive-OR Logic

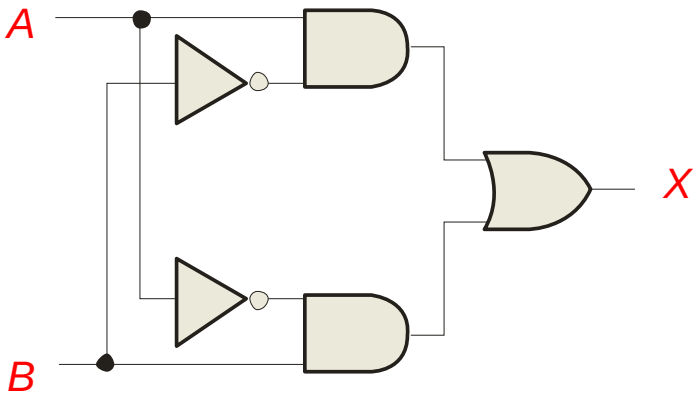
The truth table for an exclusive-OR gate is

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

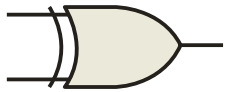
Notice that the output is HIGH whenever *A* and *B* disagree.

The Boolean expression is $X = \bar{A}B + A\bar{B}$

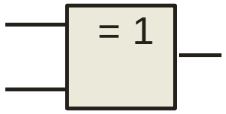
The circuit can be drawn as



Symbols:



Distinctive shape



Rectangular outline

Exclusive-NOR Logic

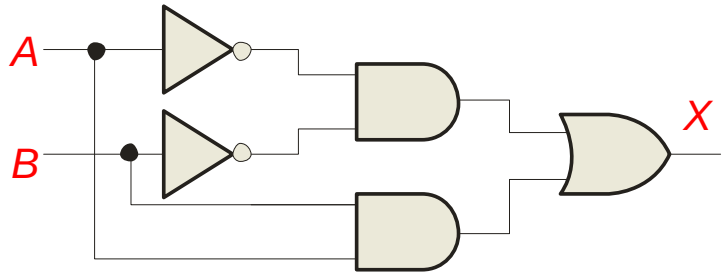
The truth table for an exclusive-NOR gate is

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1

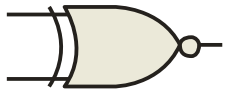
Notice that the output is HIGH whenever *A* and *B* agree.

The Boolean expression is $X = \overline{A}\,\overline{B} + AB$

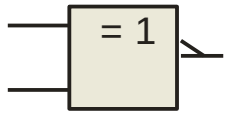
The circuit can be drawn as



Symbols:



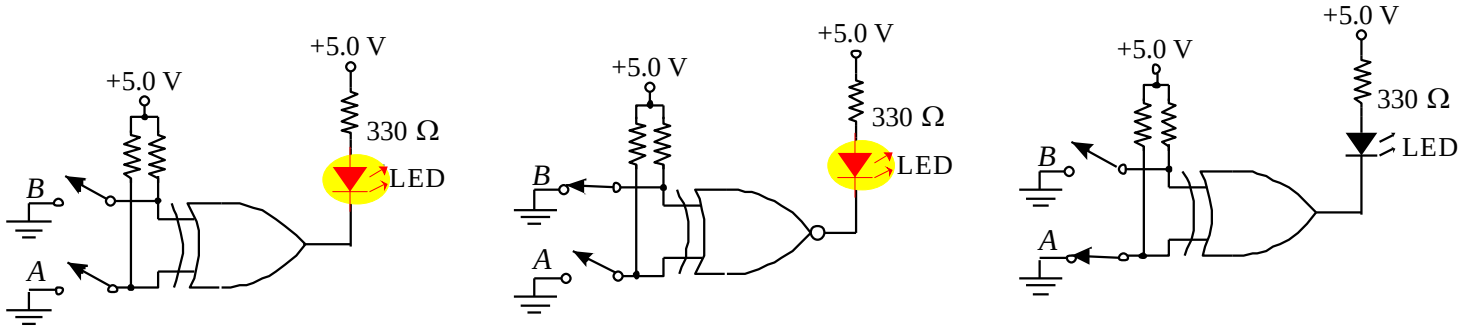
Distinctive shape



Rectangular outline

Example

For each circuit, determine if the LED should be on or off.



Solution

Circuit (a): XOR, inputs agree, output is LOW, LED is ON.

Circuit (b): XNOR, inputs disagree, output is LOW, LED is ON.

Circuit (c): XOR, inputs disagree, output is HIGH, LED is OFF.

Implementing Combinational Logic

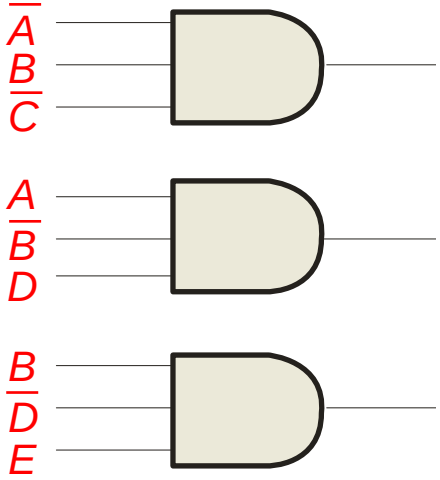
Implementing a SOP expression is done by first forming the AND terms; then the terms are ORed together.

Example

Show the circuit that will implement the Boolean expression $X = ABC + AB\overline{D} + \overline{B}DE$. (Assume that the variables and their complements are available.)

Solution

Start by forming the terms using three 3-input AND gates. Then combine the three terms using a 3-input OR gate.

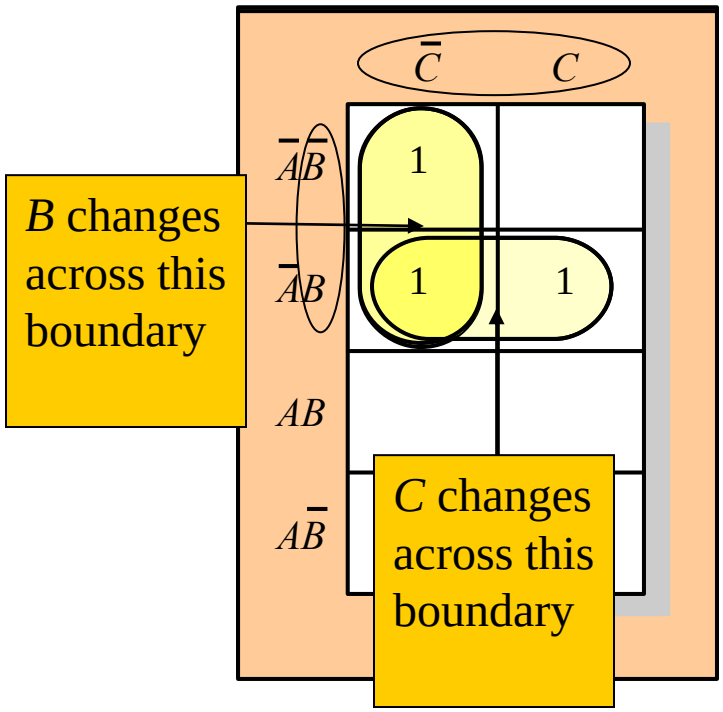


$$X = \overline{A}B\overline{C} + A\overline{B}D + B\overline{D}E$$

Karnaugh Map Implementation

For basic combinational logic circuits, the Karnaugh map can be read and the circuit drawn as a minimum SOP.

Example A Karnaugh map is drawn from a truth table. Read the minimum SOP expression and draw the circuit.



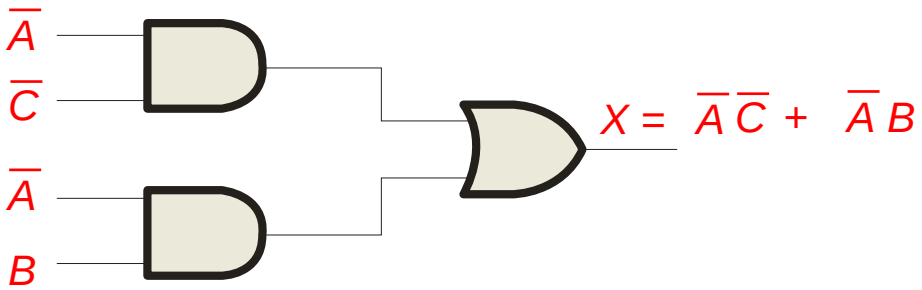
Solution

1. Group the 1's into two overlapping groups as indicated.
2. Read each group by eliminating any variable that changes across a boundary.
3. The vertical group is read $\overline{A}\,\overline{C}$.
4. The horizontal group is read $\overline{A}B$.

The circuit is on the next slide:

Solution *continued…*

Circuit:



The result is shown as a sum of products.

It is a simple matter to implement this form using only NAND gates as shown in the text and following example.

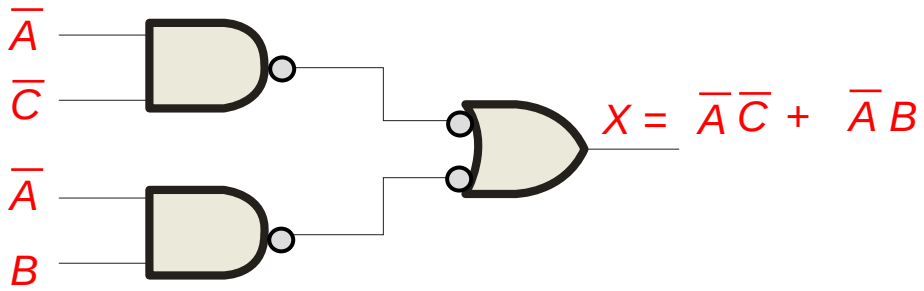
NAND Logic

Example

Convert the circuit in the previous example to one that uses only NAND gates.

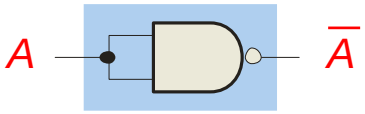
Solution

Recall from Boolean algebra that double inversion cancels. By adding inverting bubbles to above circuit, it is easily converted to NAND gates:

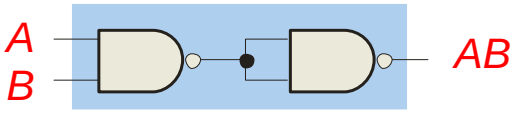


Universal Gates

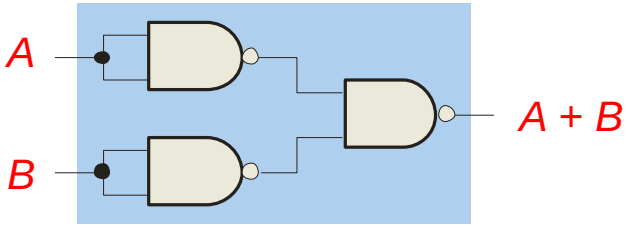
NAND gates are sometimes called **universal** gates because they can be used to produce the other basic Boolean functions.



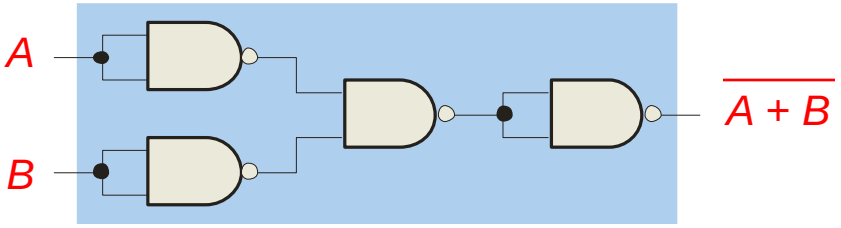
Inverter



AND gate



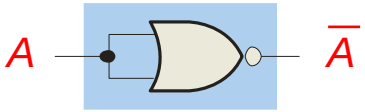
OR gate



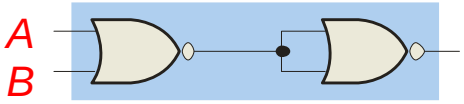
NOR gate

Universal Gates

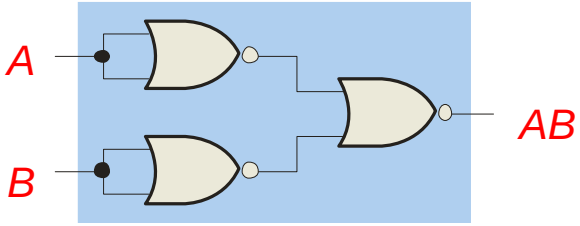
NOR gates are also **universal** gates and can form all of the basic gates.



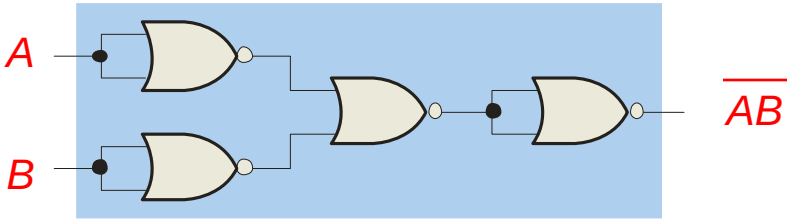
Inverter



OR gate



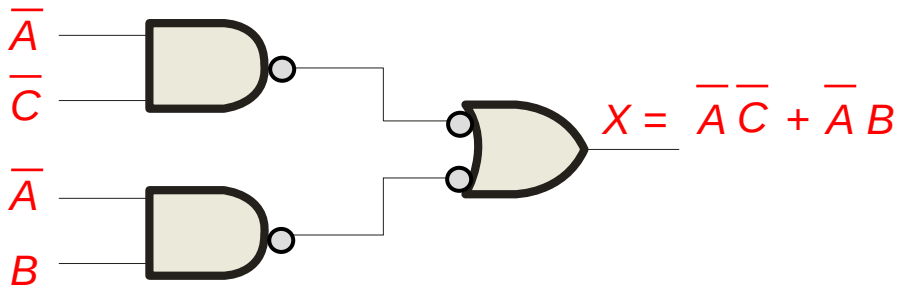
AND gate



NAND gate

NAND Logic

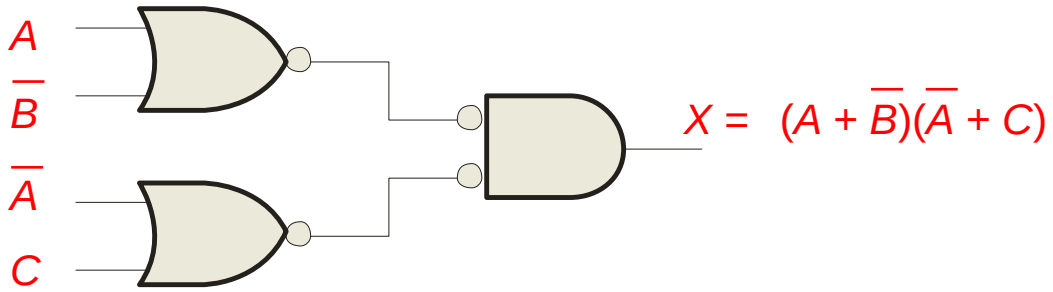
Recall from DeMorgan's theorem that $\overline{AB} = \overline{A} + \overline{B}$. By using equivalent symbols, it is simpler to read the logic of SOP forms. The earlier example shows the idea:



The logic is easy to read if you (mentally) cancel the two connected bubbles on a line.

NOR Logic

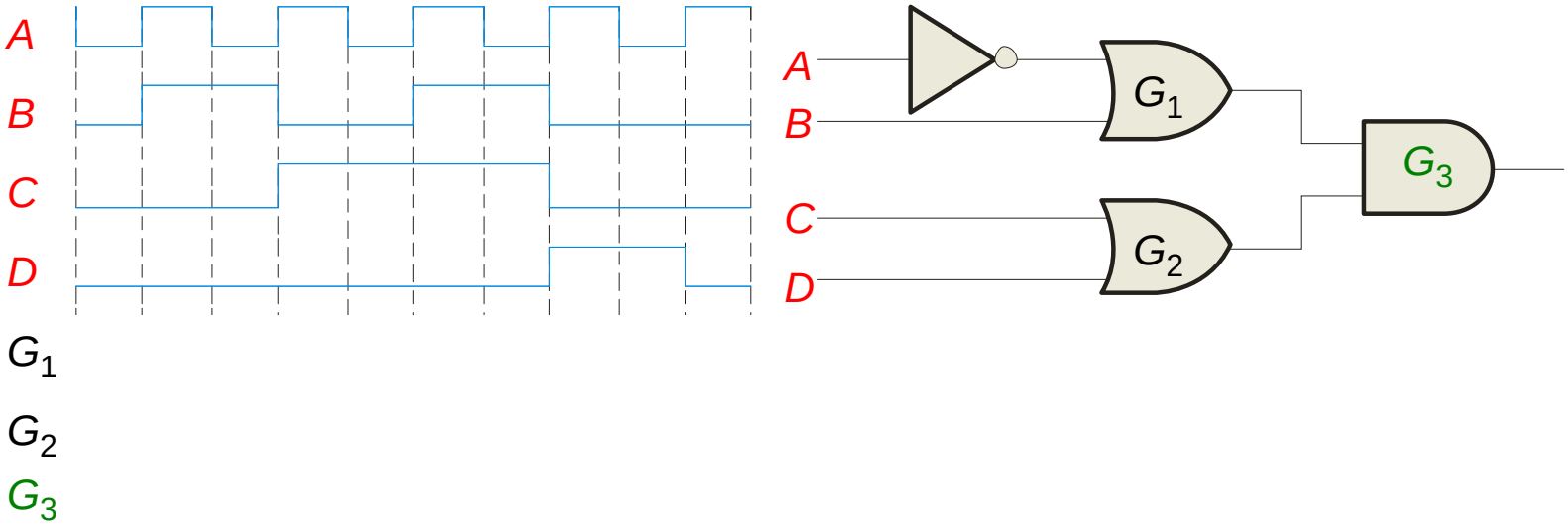
Alternatively, DeMorgan's theorem can be written as $\overline{A + B} = \overline{A}\,\overline{B}$. By using equivalent symbols, it is simpler to read the logic of POS forms. For example,



Again, the logic is easy to read if you cancel the two connected bubbles on a line.

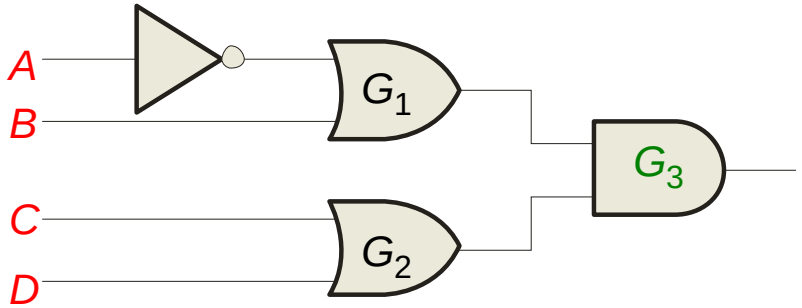
Pulsed Waveforms

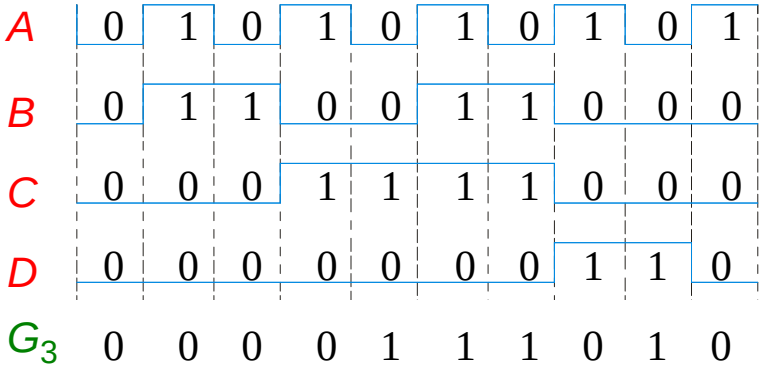
For combinational circuits with pulsed inputs, the output can be predicted by developing intermediate outputs and combining the result. For example, the circuit shown can be analyzed at the outputs of the OR gates:



Pulsed Waveforms

Alternatively, you can develop the truth table for the circuit and enter 0's and 1's on the waveforms. Then read the output from the table.



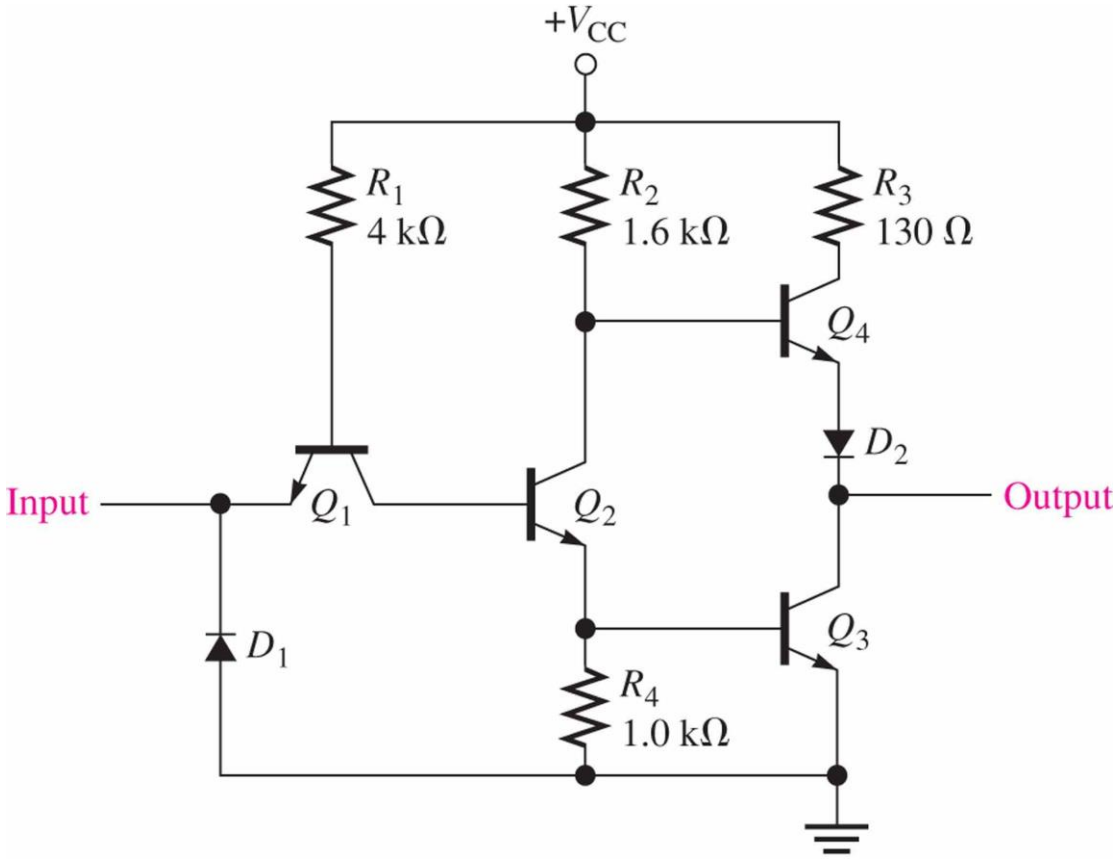


Inputs				Output
A	*B*	*C*	*D*	*X*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

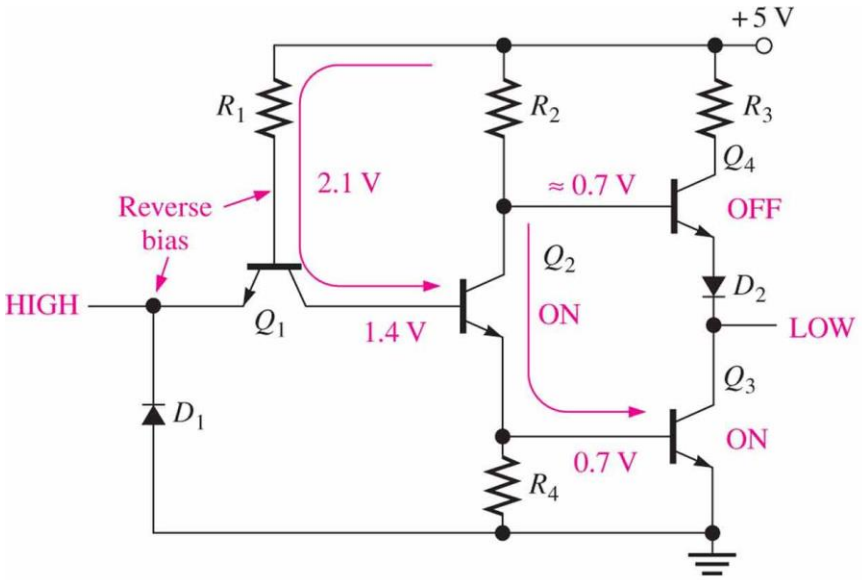
Other gates

- Open Collector gate（集电极开路门电路）
- Wired-AND（线与）
- Tri-state gate（三态门）

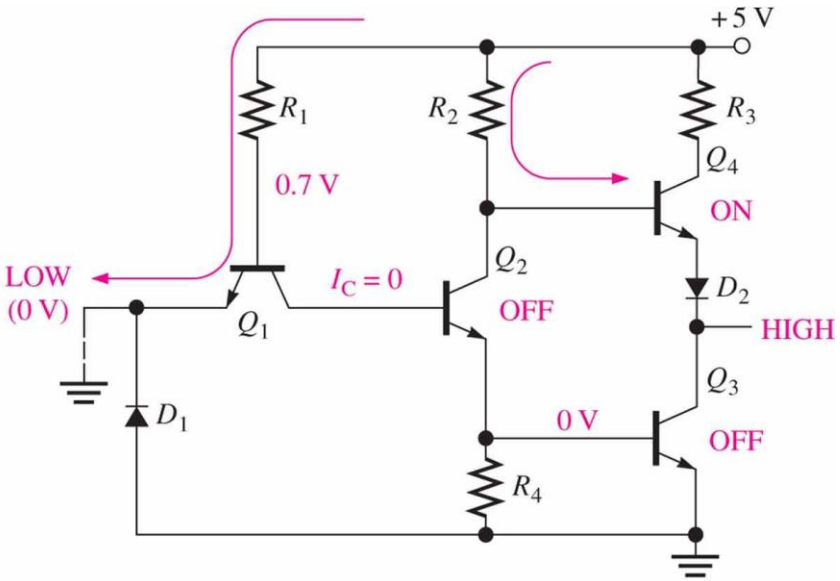
A standard TTL inverter circuit



Operation of a TTL inverter

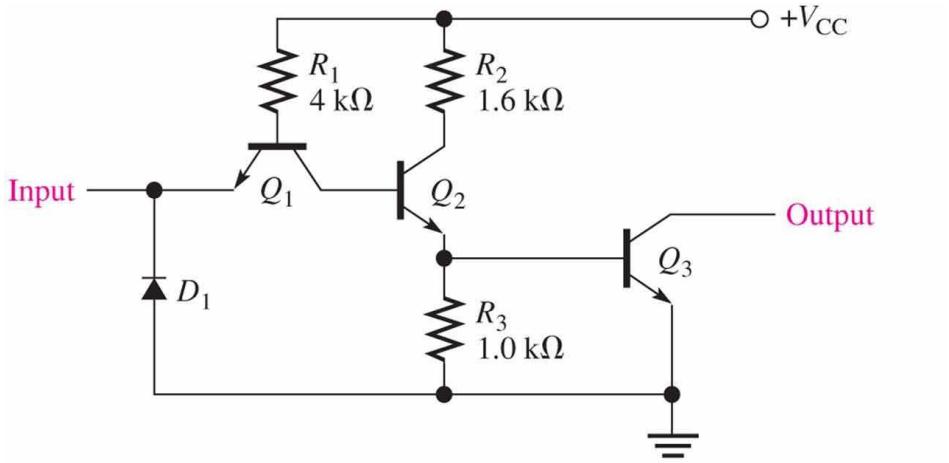


(a)

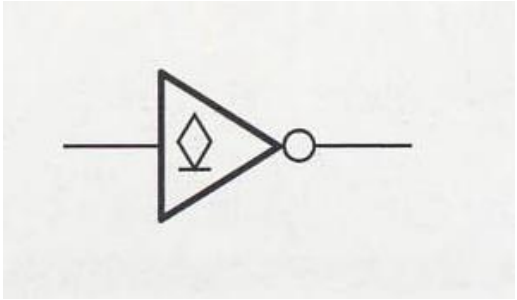


(b)

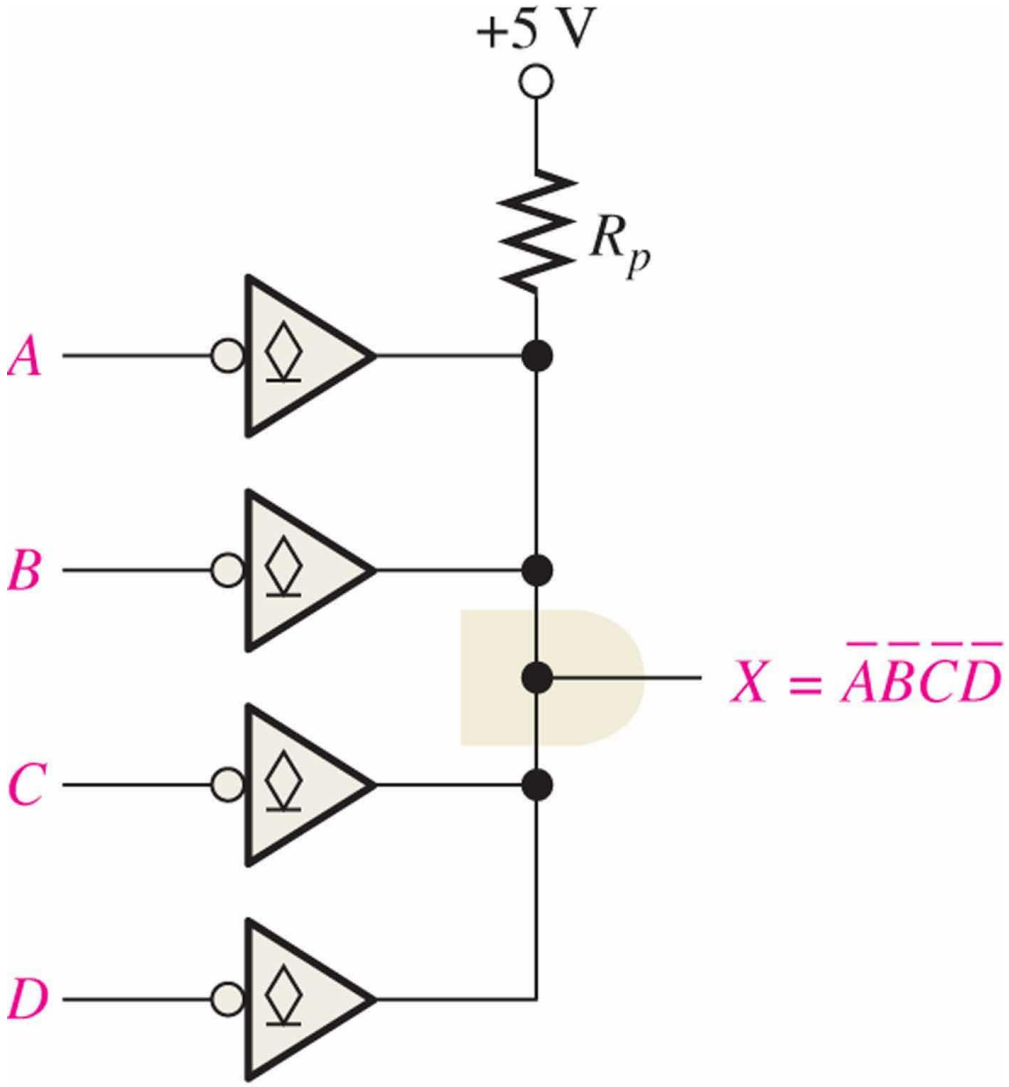
Open collector gate



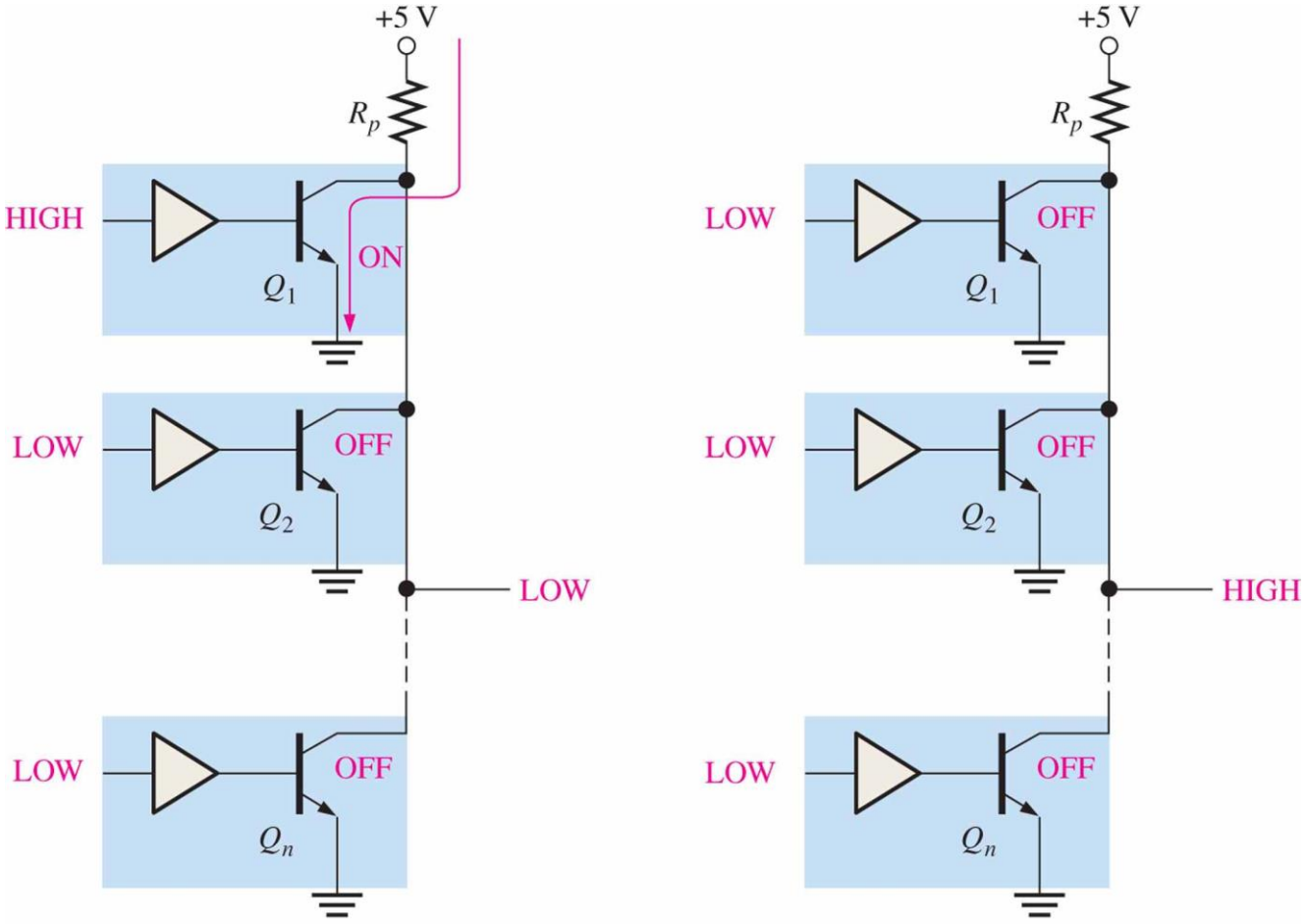
(a) Open-collector inverter circuit



A wired-AND configuration of four inverters



Open-collector wired negative-AND operation with inverters



(a) When one or more output transistors are on, the output is LOW.

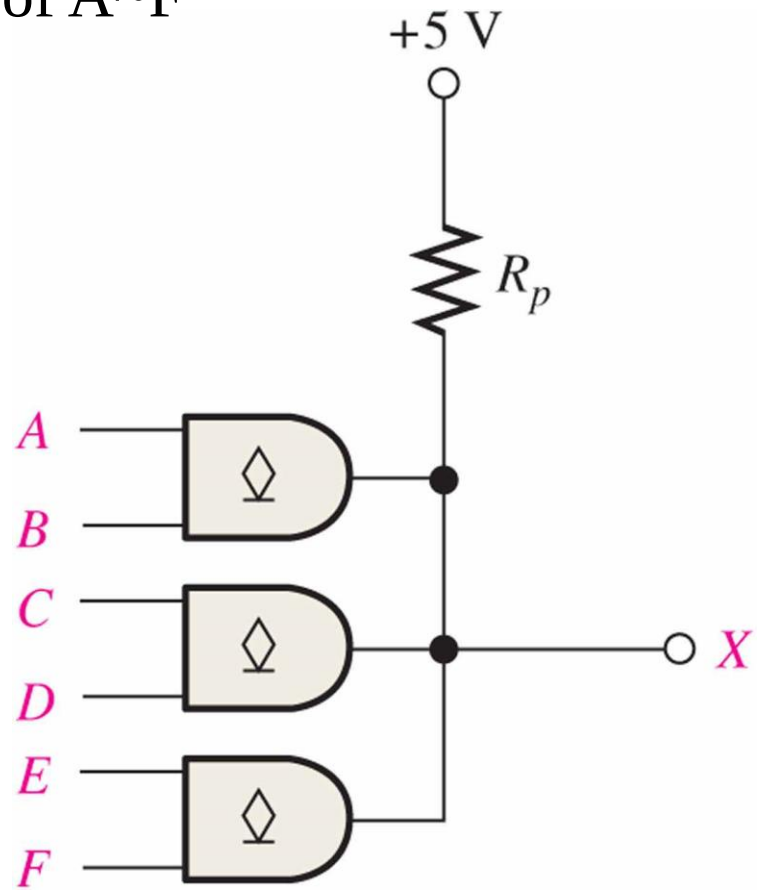
(b) When all output transistors are off, the output is HIGH.

Wired-AND

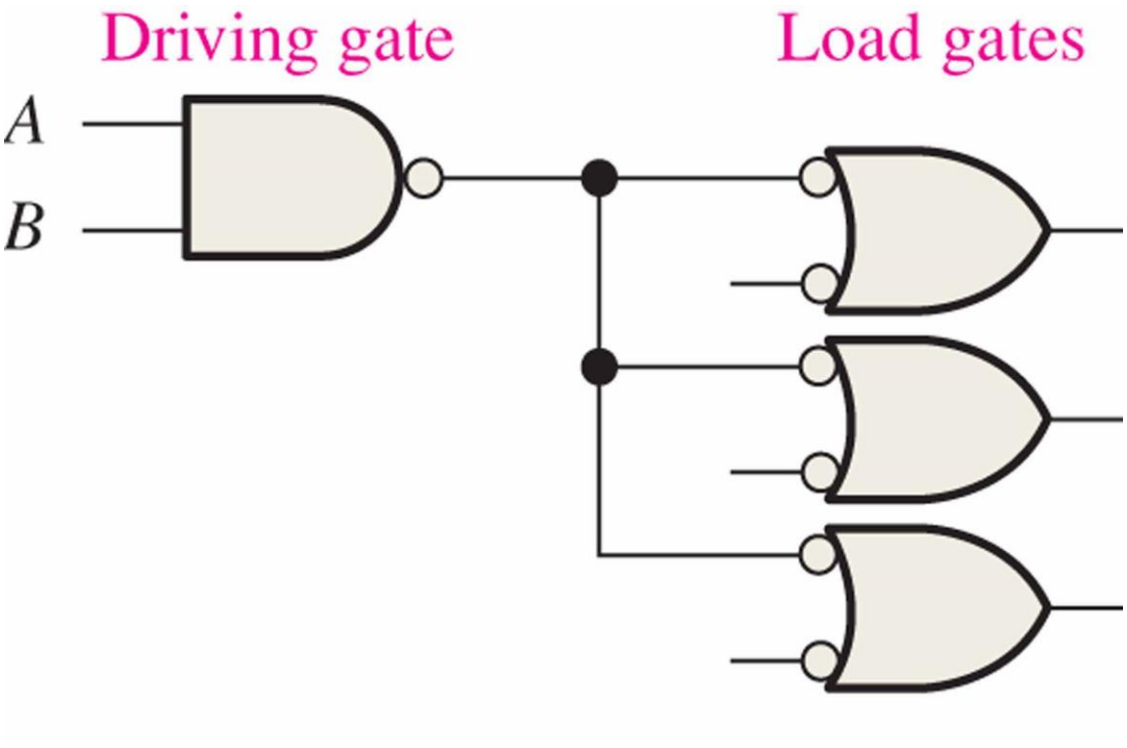
Example Determine X as a function of A~F

Solution

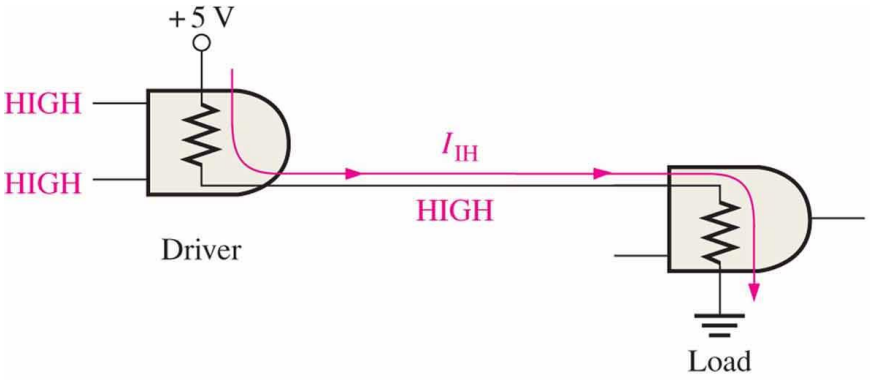
X = ABCDEF



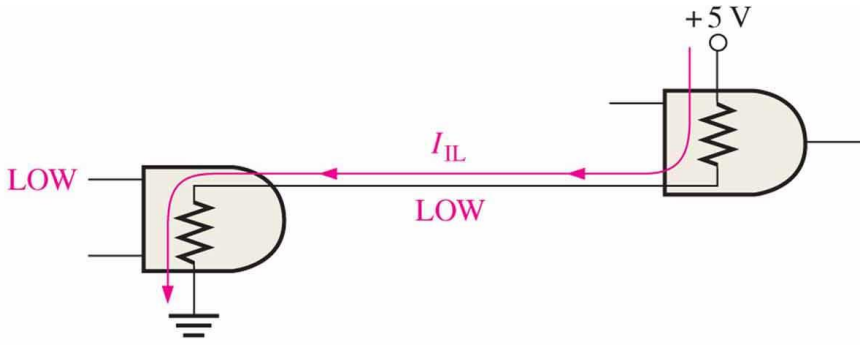
Driving and loading concepts

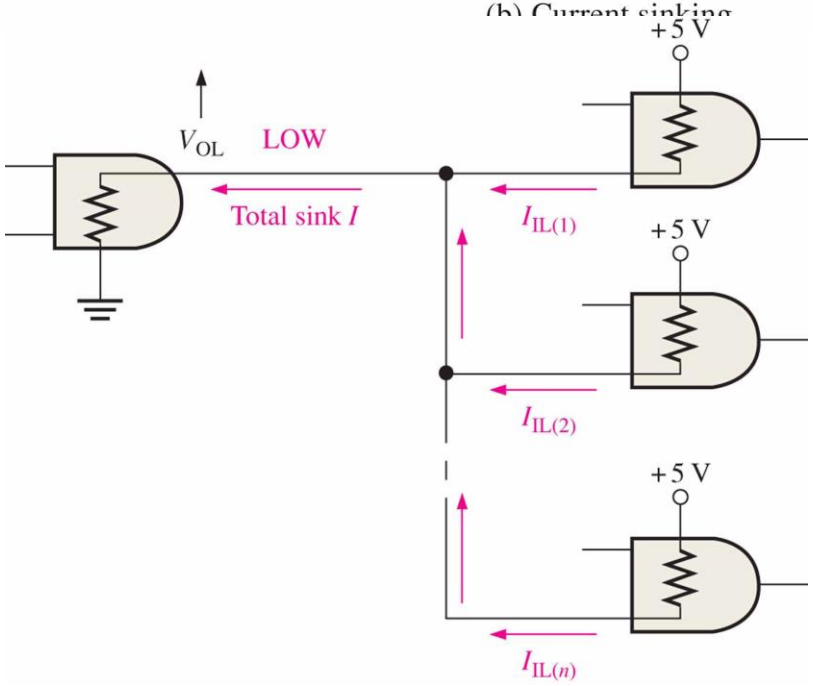


Driving and loading concepts (in TTL)

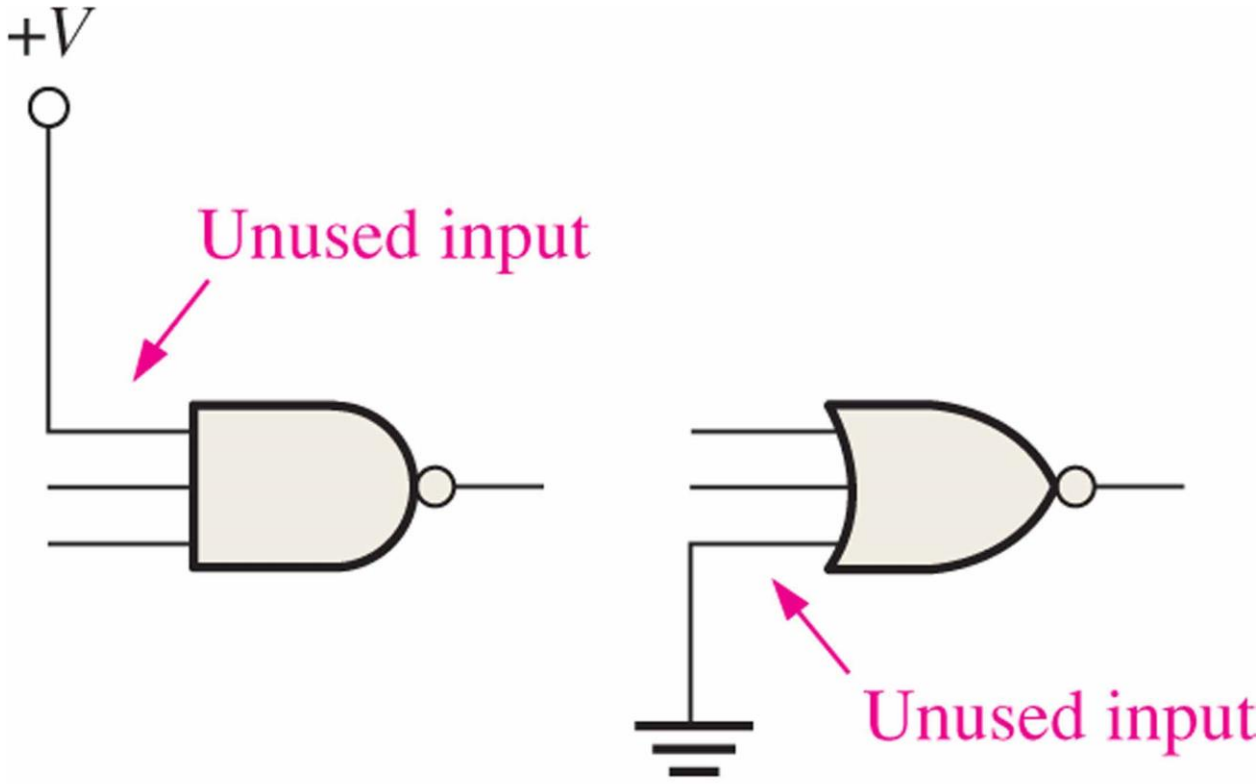


(a) Current sourcing





Handling unused CMOS inputs



Selected Key Terms

Universal gate Either a NAND or a NOR gate. The term universal refers to a property of a gate that permits any logic function to be implemented by that gate or by a combination of gates of that kind.

Negative-OR The dual operation of a NAND gate when the inputs are active-LOW.

Negative-AND The dual operation of a NOR gate when the inputs are active-LOW.

Homework

- pp. 302 (International Ed.)
- 2(b), 4(d,e), 8, 10(g), 16, 20(b), 22(b), 26(g), 28

- pp.888 (International Ed.)
- 2, 14, 22