上 海 交 通 大 学 试 卷（E 卷）

（2021 至 2022 学年 第 2 学期）

班级号_____ 学号_____ 姓名_____

课程名称_____EST2501 数字电子技术_____ 成绩_____

PART I：True/False (20%)

Answers to Questions 1-10 (filling in T for truth statement or F for false statement)

1	2	3	4	5	6	7	8	9	10

1. ( ) The inputs to an AND gate are: A=1, B=0, C=1. The output will be LOW.

2. ( ) The commutative law of Boolean addition states that A+B=A B

3. ( ) Digital systems can process, store, and transmit data more efficiently and can assign infinite values to each point.

4. ( ) A HIGH logic level can be any voltage between a specified minimum value and a specified maximum value.

5. ( ) NAND gates cannot be used to construct NOR gates.

6. ( ) Clock waveforms carry pieces of information such as letters and numbers.

7. ( ) By connecting the $\bar{Q}$ to the data input, the D Flip-Flop works at the toggle mode.

8. ( ) Once an up/down counter begins its count sequence, it cannot be reversed.

9. ( ) The following circuit in Figure 1 is a retriggerable one-shot.

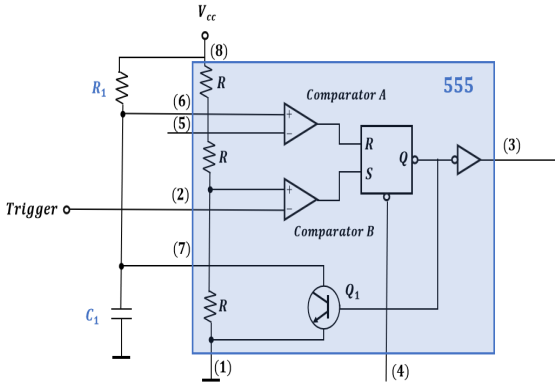


Figure 1

我承诺，我将严格遵守考试纪律。

承诺人：_____.

题号	Part I	Part II	Part III	Part IV			
				1	2	3	4
得分							
批阅人(流水阅卷教师签名处)							

10. ( ) The circuit of the look-ahead carry adder is more complex than the ripple carry adder.

Part II: **Filling the blanks(20%)**

1. There are 580 students to be numbered in binary system. How many bits at least will be used ?

_____

2. Please give the 2's complement of $(-47)_{10}$ in 8 bits binary system. _____

3. In Figure 2, the frequency of CP is 8KHz, please answer following questions:

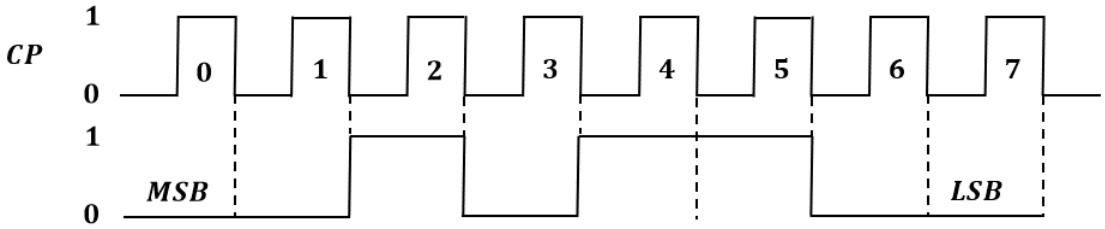


Figure 2

(1) The binary code of the waveform under the CP is _____.

(2) By using serial data transfer method, how long will it take to transfer the code?_____

(3) By using parallel data transfer method, how long will it take to transfer the code? _____

4. A retriggerable one-shot has a pulse width of 10ms; 3ms after being triggered, another trigger pulse is applied. The resulting output pulse will be_____ms.

5. The relationship between a NOR gate and a negative-AND gate with two inputs A and B is expressed by _____=_____.

6. In the following Figure 3, the modulus of the counter is _____, and the output frequency of the counter is _____.

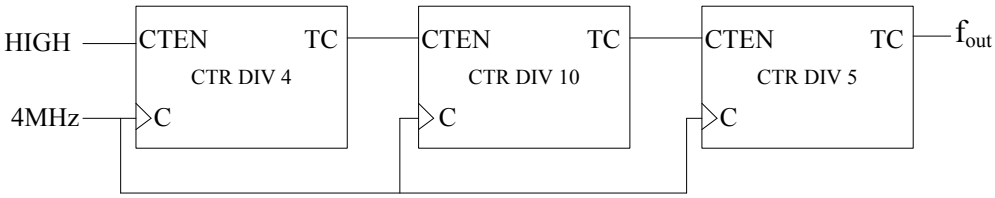


Figure 3

7. For a 3-bit asynchronous counter, if the edge triggered J-K FFs has a propagation delay of 10ns, the maximum clock frequency at which the counter can be operated is _____MHz.

Part III: Choice (Choose the one alternative that best completes the statement or answers the question) (20%)

Answers to Questions 1-10

1	2	3	4	5	6	7	8	9	10

1. Which type of gate can be used to add two bits?

   (A) NAND (B) NOR (C) XOR (D)XNAND

2. Pulse width is defined as the_____.

   (A) time that the pulse remains at the HIGH level.

   (B) time difference between the rising and falling edges.

   (C) length of the pulse measured at the LOW level.

   (D) duration of the pulse at the 50% level.

3. What is the BCD form of 438 in odd parity? (The parity bit is the LSB)

(A) 0100000110100

(B) 0100001110001

(C) 1010000111000

(D) 1000001101000

4. What is the Gray code for the binary-to-Gray converter's output when the input binary is 1001?

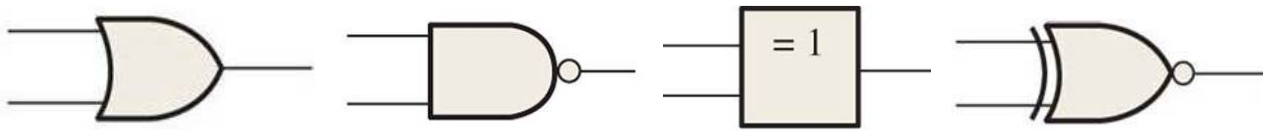
(A) 0110

(B) 1011

(C) 1101

(D) 1001

5. Which in the following Figure 4 is the standard logic symbol of XNOR?



(A) (B) (C) (D)

Figure 4

6. When performing binary addition using the 2's complement method, an overflow can occur if _____.

(A) both numbers have the same magnitude.

(B) one number is negative and the other is positive.

(C) the second number is much greater than the first.

(D) both numbers have the same sign.

7. How many XOR gates will be used in a binary odd parity checker with four inputs? _____

(A) 2 (B) 3 (C) 4 (D) 5

8. Which of the following statements about the Mealy model of sequential circuit is correct?

(A) The outputs only depend on inputs.

(B) The outputs only depend on current state.

(C) The outputs depend on current state and inputs.

(D) The outputs are independent of inputs or current state.

9. How many minterms will make the logic function F(A,B,C,D)=$\bar{A}B + C\overline{D}$ =1?

(A) 5 (B) 6 (C) 7 (D) 8

10. For the S-R latch in Figure 5 , if S=R=0, what is the value of Q?

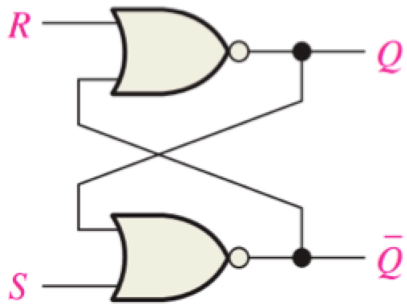


Figure 5

(A) no change (B) invalid (C) 0 (D) 1

Part IV: Analysis or Design (40%)

1. Analyze the circuit in Figure 6. Find the expression of output Y and use the Karnaugh map to find the minimum SOP form and the minimum POS form of Y. (6%)

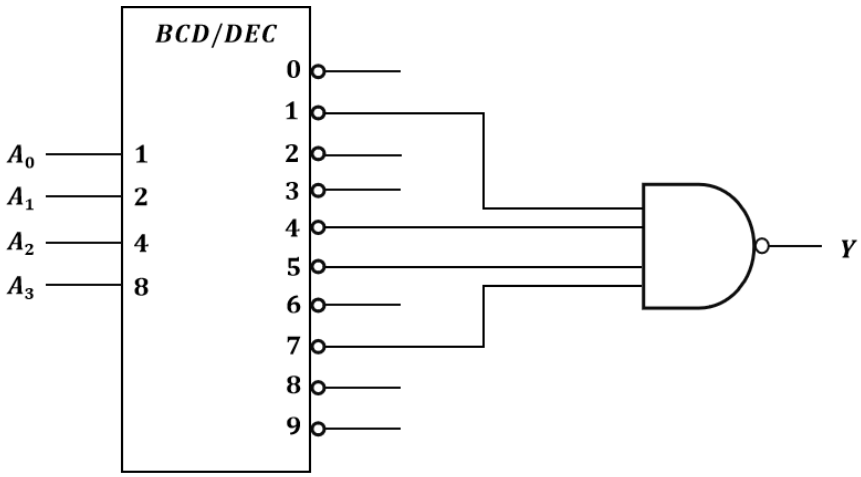


Figure 6

2. Use an 1 of 8 Multiplexer to implement a two bits binary(A_1A_0;B_1B_0) comparator . The output will be 1 if A > B, otherwise the output will be 0. Finish the connection of the pins of the circuit in Figure 7. (10%)

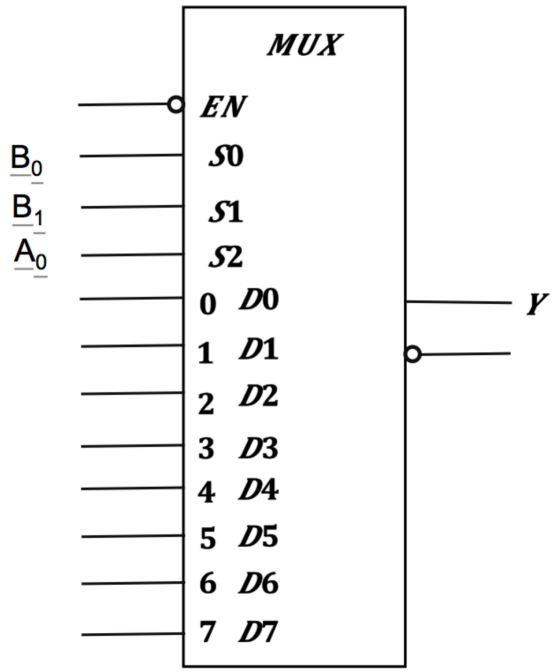


Figure 7

3. Analyze the circuit in Figure 8. Give its excitation equations, transition equations and the output equation. Draw the transition table and the state diagram of the circuit. (12%)

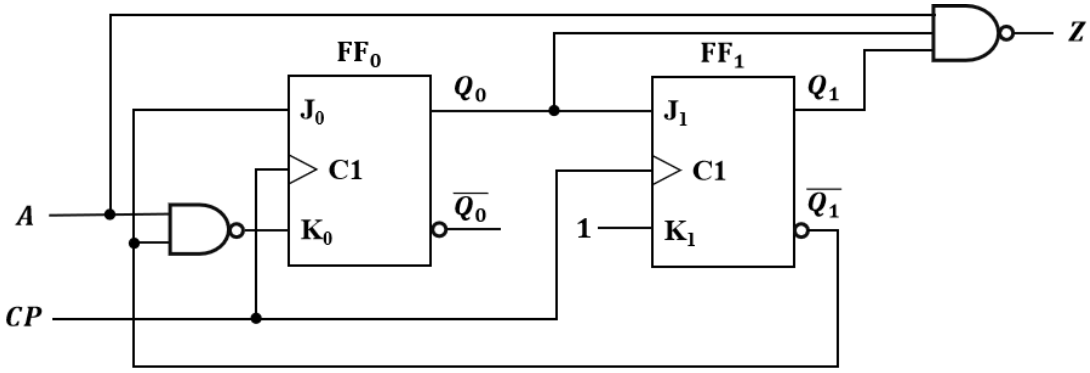


Figure 8

4. Develop a synchronous sequential circuit with the state transition table shown in Table 1 using JK Flip-Flops and gates. (12%)

$Q_1^nQ_0^n$	$Q_1^{n+1}Q_0^{n+1}$/Y	
	A=0	A=1
00	01/0	11/0
01	10/0	00/0
10	11/0	01/0
11	00/1	10/1

Table 1