上 海 交 通 大 学 试 卷（A 卷）

（ 2020 至 2021 学年 第 1 学期 ）

班级号_____ 学号_____ 姓名_____

课程名称 EI243 数字电子技术 成绩_____

PART I Multiple Choice (单选题, 40%)

1. The pulse width of the nonideal pulse in Figure 1 is defined by ( ).

(A) a (B) b (C) c (D) d

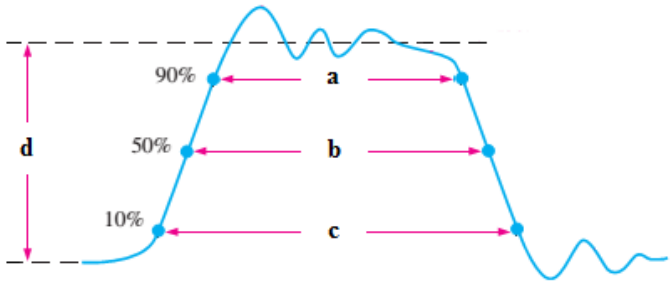

Figure 1

2. Figure 2 is an example of a ( ) diagram.

(A) circuit (B) logic (C) state (D) timing

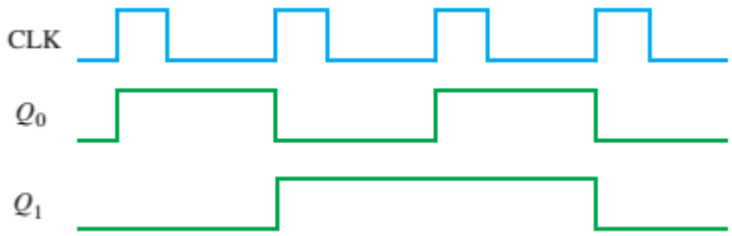

Figure 2

3. In BCD addition, if a 4-bit sum is greater than 9, or if a carry out of the 4-bit group is generated, add ( ) to the 4-bit sum.

(A) 2 (0010) (B) 4 (0100) (C) 6 (0110) (D) 8 (1000)

4. The OR operation is equivalent to ( ).

(A) Boolean addition (B) Boolean multiplication (C) Boolean negation (D) mod-2 addition

5. The data selection function is performed by a logic circuit called a/an ( ).

(A) decoder (B) demultiplexer (C) encoder (D) multiplexer

6. The logic expression $A\overline{B}\,\overline{C}\,\overline{D}+AB\overline{C}D$ is equivalent to ( ).

我承诺，我将严格遵守考试纪律。

承诺人：_____.

题号	I	II	III			
	1-20	21-32	33	34	/	/
得分					/	/
批阅人(流水阅卷教师签名处)					/	/

(A) $A\overline{C}(\overline{B}\,\overline{D}+BD)$ (B) $A\overline{C}\,\overline{B\oplus D}$ (C) $A\overline{C}\,\overline{\overline{B}D+B\overline{D}}$ (D) all of the above

7. ( ) is a POS expression.

(A) $AB+CD$ (B) $\overline{\overline{A+B}+\overline{C+D}}$ (C) $(A+B)(C+D)$ (D) $\overline{\overline{AB}\,\overline{CD}}$

8. The AND operation is the dual of the ( ) operation.

(A) NAND (B) negative OR (C) OR (D) none of the above

9. The logic expressions for the circuit in Figure 3 are ( ), and $Z=\overline{X+Y}$.

(A) $X=\overline{A}_1B_1+\overline{A_1\oplus B_1}\,\overline{A}_0B_0, Y=\overline{A_1\oplus B_1}\,\overline{A_0\oplus B_0}$

(B) $X=A_1\overline{B}_1+\overline{A_1\oplus B_1}\,A_0\overline{B}_0, Y=\overline{A_1\oplus B_1}\,\overline{A_0\oplus B_0}$

(C) $X=\overline{A}_1B_1+(A_1\oplus B_1)\overline{A}_0B_0, Y=(A_1\oplus B_1)(A_0\oplus B_0)$

(D) $X=A_1\overline{B}_1+(A_1\oplus B_1)A_0\overline{B}_0, Y=(A_1\oplus B_1)(A_0\oplus B_0)$

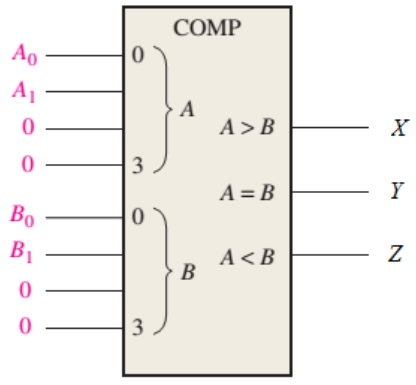

Figure 3

10. The logic expression for the circuit in Figure 4 is ( ).

(A) $\overline{A}\,\overline{B}C+\overline{A}B\overline{C}+AB\overline{C}+ABC$

(B) $\overline{A}\,\overline{B}C+A\overline{B}\,\overline{C}+AB\overline{C}+ABC$

(C) $\overline{A}\,\overline{B}\,\overline{C}+\overline{A}BC+A\overline{B}\,\overline{C}+A\overline{B}C$

(D) none of the above

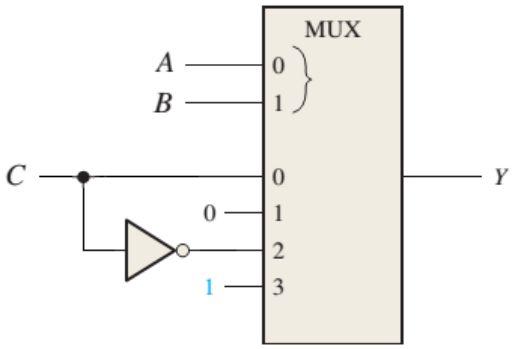

Figure 4

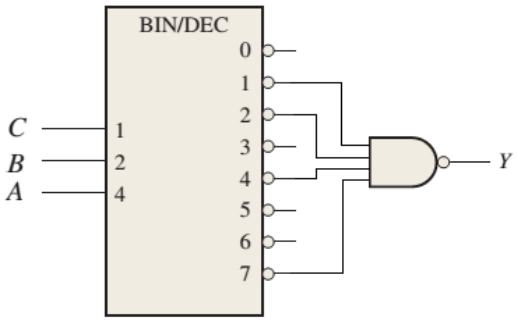

Figure 5

11. The expression for the circuit in Figure 5 is ( ).

(A) $\overline{A}\,\overline{B}\,\overline{C}+\overline{A}BC+A\overline{B}C+AB\overline{C}$

(B) $\overline{A}\,\overline{B}C+\overline{A}B\overline{C}+A\overline{B}\,\overline{C}+ABC$

(C) $\overline{A}\,\overline{B}C+\overline{A}B\overline{C}+\overline{A}BC+ABC$

(D) none of the above

12. Consider the circuit in Figure 6. If $D=(D_2D_1D_0)_2$, $Y=(Y_4Y_3Y_2Y_1Y_0)_2$, then ( ).

(A) $Y=D$ (B) $Y=2D$ (C) $Y=3D$ (D) none of the above

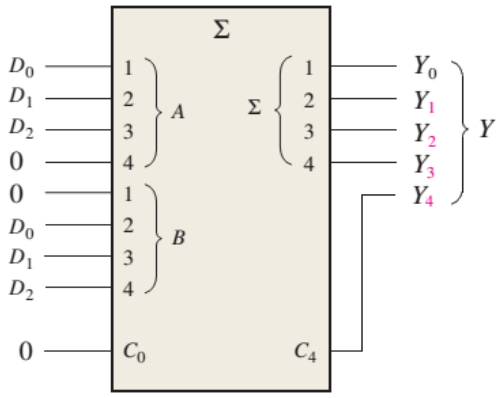

Figure 6

13. A combinational circuit accepts a 2-bit number $A=(A_1A_0)_2$ and produces a 5-bit binary number $X=(X_4X_3X_2X_1X_0)_2$. If $X=A^3$, then $X_4=$( ).

(A) 0 (B) A_0 (C) A_1 (D) A_1A_0

14. Draw the Q output relative to the clock with the input as shown in Figure 7. Assume that Q is initially LOW. ( )

(A) a (B) b (C) c (D) none of the above

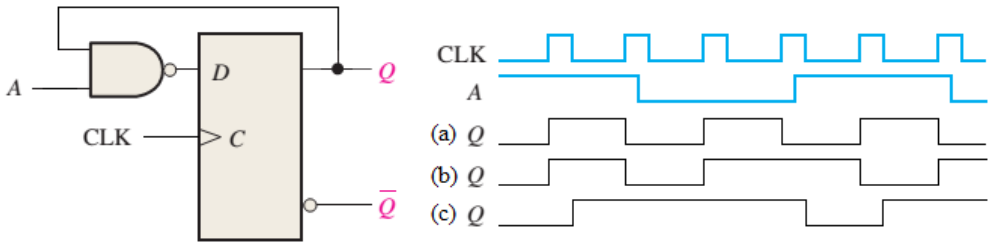

Figure 7

15. Draw the Q output relative to the clock with the inputs as shown in Figure 8. Assume that Q is initially LOW.

(A) a (B) b (C) c (D) none of the above

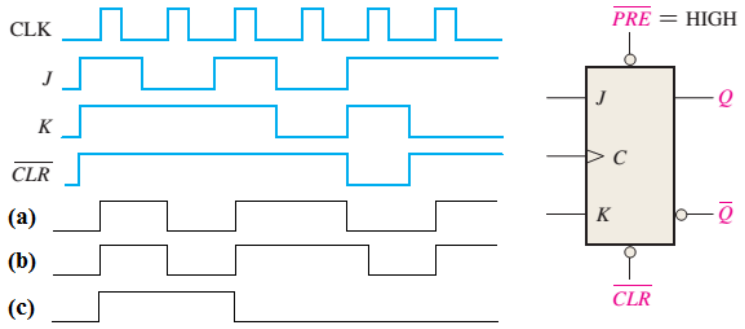

Figure 8

16. Figure 9 shows the logic symbol for a ( ) one-shot.

(A) negative-edge triggered nonretriggerable

(B) negative-edge triggered retriggerable

(C) positive-edge triggered nonretriggerable

(D) positive-edge triggered retriggerable

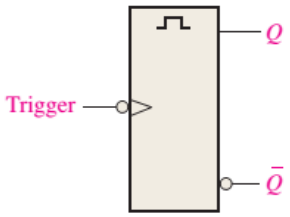

Figure 9

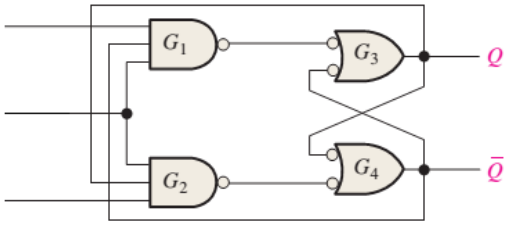

Figure 10

17. Figure 10 shows a ( ).

(A) D flip-flop (B) D latch (C) J-K latch (D) J-K flip-flop

18. In the general sequential logic model in Figure 11, the outputs of the memory are called the ( ) variables of the sequential logic.

(A) excitation (B) input (C) output (D) state

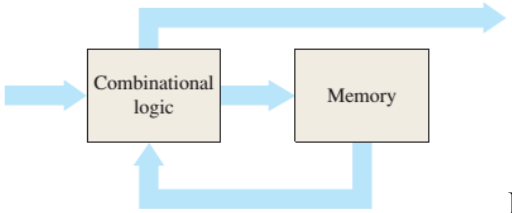

Figure 11

19. We need at least ( ) flip-flops to design a counter to produce the following binary sequence: 0, 9, 1, 8, 2, 7, 3, 6, 0, …

(A) 4 (B) 3 (C) 2 (D) 1

20. For the cascaded counter configuration in Figure 12, the waveform at point ( ) has a frequency of 1 kHz.

(A) ① (B) ② (C) ③ (D) ④

Figure 12

PART II Filling Blanks（填空题, 36%）

21. Figure 13 shows the operation of a two-input ( ) gate.

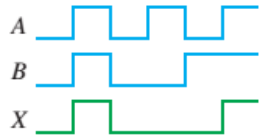

Figure 13

22. Convert the unsigned binary number 101 0110 to decimal. ( )

23. Convert the decimal number 177.8125 to binary. ( )

24. Determine the decimal value of the signed binary number in the 2's complement form: 1011 0001. ( )

25. Add the two hexadecimal numbers: $1A58_{16}$ and $81D0_{16}$. ( )

26. Determine the minimum expression for the circuit in Figure 14 .

( )

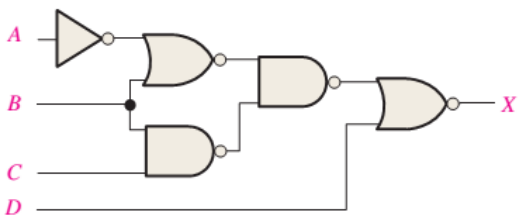

Figure 14

27. Write the NOR-NOR expression for the truth in Figure 15. Minimization is not required.

(　　)

28. Minimize the expression: $X = A\overline{B}D + \overline{A}\overline{B}\overline{C}D + \overline{B}CD + \overline{A\overline{B} + C}(B + D)$.

(　　)

29. Determine the even parity bit for the 7-bit group: 101 0111. (　　)

30. Determine the modulus of the cascaded counter in Figure 16. (　　)

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Figure 15

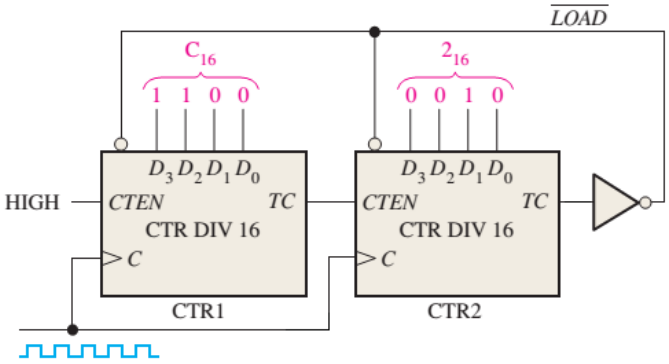

Figure 16

31. Determine the modulus of the counter in Figure 17. (　　)

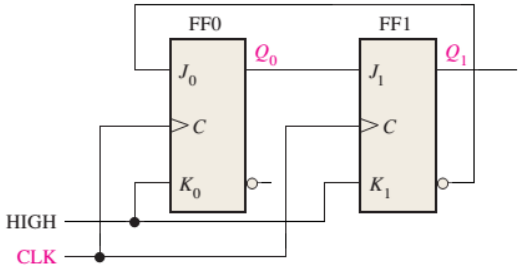

Figure 17

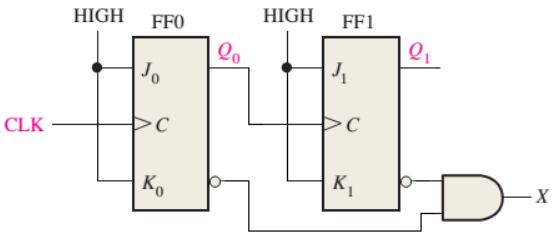

Figure 18

32. Figure 18 shows a 2-bit asynchronous counter connected to a decoder (the AND gate). Decoding glitch can be seen when the counter state Q_1Q_0 changes from (　　) to (　　).

PART III Design (设计题, 24%)

33. Design a circuit with three input variables that will only produce a 1 output when two or three input variables are 1s. (9%)

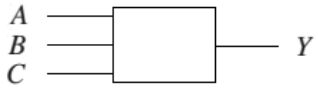

Figure 19

34. Design a synchronous counter with the binary count sequence 000, 001, 010, 011, 100, 000, …. Use D flip-flops. (15%)