Technische Universität Braunschweig

Chair for Chip Design for Embedded Computing

Topics for Student Projects

Bachelor Thesis, Master Thesis, HiWi

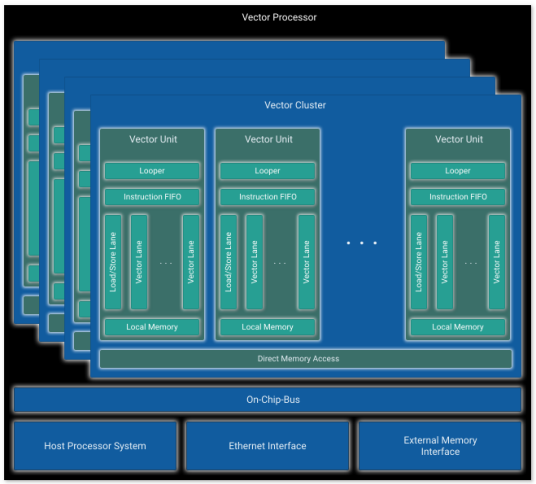
Chair for Chip Design for Embedded Computing, 11. November 2021

General Information

- we offer different topics for Master's Thesis, Bachleor's Thesis & student assistant jobs (HiWi)
- this document provides a brief overview of topics the institute offers to students
- the topic language can be English or German
- if you are interested in a specific topic, you can contact the employee yourself

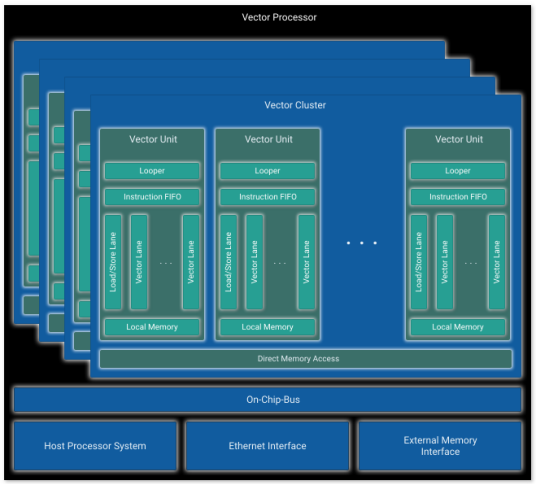
TTA Controller for a Vectorprocessor Architecture

- **Type**: Master Thesis
- **Description**: A controller for the vectorprocessor architecture controls command issue as well as also it performs synchronisation of vector instruction execution in clustered vector units and data-transfer of the DMA. Currently a MIPS core is implemented to generate those control structure. A Transport-Triggered-Architecture looks promising for those tasks in terms of performance and flexibility.
- **Requirements**: VHDL, C/C++, Makefiles
- **Link**: openasip.org/
- **Contact person**: M. Sc. Sven Gesper
  s.gesper@tu-braunschweig.de



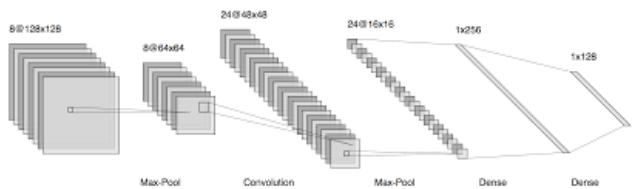
Verification Framework for Vector Instructions on a Scalable Vertical Vectorprocessor Architecture

- **Type**: Bachelor/Master Thesis
- **Description**: A Framework shall be created to perform testing of the complex vectorprocessor architecture. Beside varying vector lengths and structures, further concepts as chaining, clustering and segmentation have to be considered in generation of the test framework. The Test-cases should create a high coverage.
- **Requirements**: C++, Verification, Simulation
- **Link**: Projektwebseite
- **Contact person**: M. Sc. Sven Gesper
  s.gesper@tu-braunschweig.de



CNN execution schematics on a Vectorprocessor Architecture

- **Type**: Master Thesis
- **Description**: Execution (Inference) of CNNs may use different orders of execution. During convolution, the reuse of loaded data (kernels, input, accumulation result) is preferred to reduce repetition of data transfers. The Vectorprocessor Architecture allows different executions schematics which shall be implemented and analysed (run-time and utilization). Combined schematics (differentiation by layer) may result in highest performance, which shall be evaluated.
- **Requirements**: C++, CNNs
- **Link**: Projektwebseite
- **Contact person**: M. Sc. Sven Gesper
  s.gesper@tu-braunschweig.de



Optimize an LLVM-based Compiler for Kavuaka (ASIC)

- **Type**: Bachelor/Master Thesis
- **Description**: Extend the Kavuaka LLVM-based compiler with the following features: Heap/Stack implementation, Memory access (64 bit aligned access), complex pattern Custom Instr (8 bit ComplexMAC), implement missing ISA parts. We have a tutorial on how to adapt LLVM.
- **Requirements**: C++ skills
- **Link**: LLVM Intro LLVM Home Clang
- **Contact person**: M.Sc. Fabian Stuckmann f.stuckmann@tu-braunschweig.de

LLVM Logo, source

Implement Clang (C/C++-Compiler) for Kavuaka (ASIC)

- **Type**: Bachelor/Master Thesis
- **Description**: Currently the Compiler optimizations are based on an ARM frontend. We want to write a native Kavuaka C++ Compiler. This goal contains adding Kavuaka specific optimization passes in the Middle-End.
- **Requirements**: C++ skills
- **Link**: LLVM Intro LLVM Home Clang
- **Contact person**: M.Sc. Fabian Stuckmann f.stuckmann@tu-braunschweig.de

LLVM Logo, source

Vectorization and Middle End Optimizations in a LLVM Compiler for Kavuaka (ASIC)

- **Type**: Bachelor Thesis
- **Description**: Implement automatic vectorization with polly for Kavuaka. Understand why Middle optimizations differ for e.g. CMAC with different VLIW word widths.
- **Requirements**: C++ skills
- **Link**:Polly LLVM Intro LLVM Home
- **Contact person**: M.Sc. Fabian Stuckmann f.stuckmann@tu-braunschweig.de

LLVM Logo, source

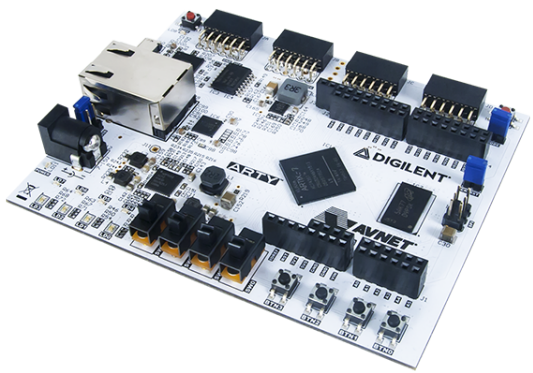
Extend a Verification Framework based on the RE-VERSI approach

- **Type**: Bachelor/Master Thesis
- **Description**: We have a runtime validation framework of Application Specific Instruction-Set Processors and want to extend the functionality.
- **Requirements**: None
- **Contact person**: M.Sc. Fabian Stuckmann f.stuckmann@tu-braunschweig.de

LLVM Logo, source

Implementation of an Evaluation Framework for a Neutron Irradiation Experiment of an FPGA

- **Type**: student assistant (HiWi)
- **Description**: implementation of a framework with the following features: runs on an Arty A7 Artix-7 FPGA Development Board, Ethernet-based communication to a external host, reading data from FPGA and simple evaluation of these data
- **Requirements**: C/C++ knowledge, VHDL (optional, we offer to teach the student VHDL basics)
- **Link**:
- **Contact person**: M.Sc. Gia Bao Thieu
  g.thieu@tu-braunschweig.de



Arty A7 Dev Board, source