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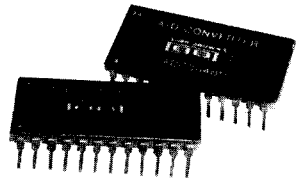


ADC804

Serial Output ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 17μsec CONVERSION TIME
- SERIAL OUTPUT—Ideal for applications requiring isolation or long-distance data transmission
- <500mW POWER DISSIPATION
- 24-PIN DUAL-WIDE HERMETIC PACKAGE
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- TWO TEMPERATURE RANGES AVAILABLE:
  ADC804BH for −25°C to +85°C Operation
  ADC804SH for −55°C to +125°C Operation
- NO MISSING CODES −25°C TO +85°C

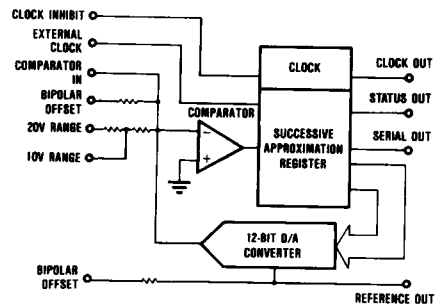
DESCRIPTION

The ADC804 is a 12-bit successive approximation analog-to-digital converter, custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic funtions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). The ADC804 has two grades, one completely specified for −25°C to +85°C operation (ADC804BH), and the other for −55°C to +125°C operation (ADC804SH).

The maximum conversion time of 17μsec makes the ADC804 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 59kHz. In addition, an external clock may be used to synchronize the converter to the system clock or to obtain faster operation. As an added benefit for ADC80 users employing the serial output capability, the ADC804 is designed to replace or provide an alternate source to ADC80 with a minimum of circuit board changes and it provides a 40% reduction in conversion time.

Data is available in serial form with corresponding clock and status signals. Elimination of the parallel output capability enables the ADC804 to be the smallest fully self-contained 12-bit ADC available today. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC804 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic supply. It is packaged in a hermetic 24-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

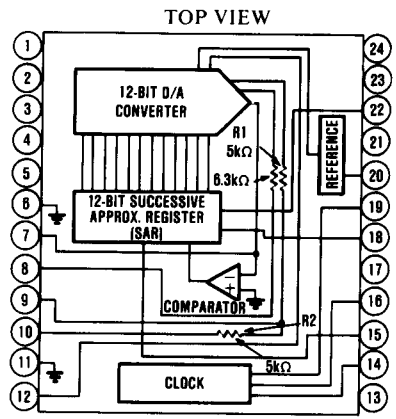
MODEL	ADC804BH			ADC804SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +5, 0 to +10			*		V
Bipolar		±2.5, ±5, ±10			*		V
Impedance: 0 to +5V, ±2.5V		2.3			*		kΩ
0 to +10V, +5V		4.6			*		kΩ
±10V		9.2			*		kΩ
DIGITAL							
Logic Characteristics (over specification temperature range)							
V_{IH} (logic "1")	2.0		5.5	*		*	V
V_{IL} (logic "0")	−0.3		+0.8	*		*	V
I_{IH} (V_{IN} = +2.7V)			−150			*	μA
I_{IL} (V_{IN} = +0.4V)			500			*	μA
Convert Command Pulse Width	100		1200	*		*	nsec
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[1]		±0.1	±0.3		*	*	% of FSR[2]
Offset Error[1]: Unipolar		±0.05	±0.2		*	*	% of FSR
Bipolar		±0.1	±0.3		*	*	% of FSR
Linearity Error			±0.012			*	% of FSR
Differential Linearity Error			±1			*	LSB
Inherent Quantization Error		1/2			*		LSB
POWER SUPPLY SENSITIVITY							
+13.5V ≤ +V_{CC} ≤ +16.5V or +11.4V ≤ +V_{CC} ≤ +12.6V		±0.003	±0.009		*	*	% of FSR/%V_{CC}
−16.5V ≤ −V_{CC} ≤ −13.5V or −12.6V ≤ −V_{CC} ≤ −11.4V		±0.003	±0.009		*	*	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005		*	*	% of FSR/%V_{DD}
DRIFT							
Total Accuracy, Bipolar[3]		±10	±23		*	*	ppm/°C
Gain		±15	±30		*	*	ppm/°C
Offset: Unipolar		±3			*		ppm of FSR/°C
Bipolar		±7	±15		*	*	ppm of FSR/°C
Linearity Error Drift		±1	±3		*	*	ppm of FSR/°C
Differential Linearity over Temperature Range			+1, −3/4			*	LSB
No Missing Code Temperature Range	−25		+85	−55		+125	°C
Monotonicity Over Temperature Range		Guaranteed			Guaranteed		
CONVERSION TIME[4]		15	17		*	*	μsec
OUTPUTS							
DIGITAL(Clock Out, Status, Serial Out)							
Output Codes, Serial (NRZ)[5]		CSB,COB			*		
Logic Levels: Logic 0 (I_{sink} ≤ 3.2mA)			+0.4			*	V
Logic 1 (I_{source} ≤ 80μA)	+2.4			*			V
Internal Clock Frequency		92.3			*		kHz
INTERNAL REFERENCE VOLTAGE							
Voltage	+6.2	+6.3	+6.4	*	*	*	V
Source Current Available for External Loads[6]	200			*			μA
Temperature Coefficient		±10	±30		*	*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, ±V_{CC}	±11.4	±15	±16.5	*	*	*	V
V_{DD}	+4.5	+5.0	+5.5	*	*	*	V
Current, +I_{CC}		5	8.5		*	*	mA
−I_{CC}		21	26		*	*	mA
I_{DD}		11	15		*	*	mA
Power Dissipation (±V_{CC} = 15V)		450	595		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	*		*	°C

*Same as specification for ADC804BH.

NOTES: (1) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustments" section. (2) FSR means full-scale range and is 20V for ±10V Range, 10V for ±5V and 0 to +10V ranges, etc. (3) Includes drift due to linearity, gain, and offset drifts. (4) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. (5) CSB means Complementary Straight Binary, and COB means Complementary Offset Binary, NRZ means non-return-to-zero coding. See Table I for additional information. (6) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specifications.

CONNECTION DIAGRAM

Pin 1 - N/C
Pin 2 - N/C
Pin 3 - N/C
Pin 4 - N/C
Pin 5 - V_{DD}
Pin 6 - Digital Common
Pin 7 - Comparator In
Pin 8 - Bipolar Offset
Pin 9 - R1 10V Range
Pin 10 - R2 20V Range
Pin 11 - Analog Common
Pin 12 - Gain Adjust
Pin 24 - N/C
Pin 23 - N/C
Pin 22 - Serial Out
Pin 21 - $-V_{CC}$
Pin 20 - Reference Out (+6.3V)
Pin 19 - Clock Out
Pin 18 - Status
Pin 17 - N/C
Pin 16 - Clock Inhibit
Pin 15 - External Clock
Pin 14 - Convert Command
Pin 13 - $+V_{CC}$



ABSOLUTE MAXIMUM RATINGS

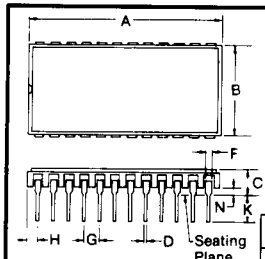
$+V_{CC}$ to Analog Common ..... 0 to +16.5V
$-V_{CC}$ to Analog Common ..... 0 to −16.5V
V_{DD} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common ..... −0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common ..... ±16.5V
Reference Output ..... Indefinite Short to Common, Momentary Short to V_{CC}

Power Dissipation 1000mW
Lead Temperature, Soldering ..... +300°C, 10sec
Thermal Resistance, θ_{JA} ..... 60°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.238	1.262	31.45	32.05
B	.586	.602	14.88	15.29
C	.160	.196	4.06	4.98
D	.016	.020	0.41	0.51
F	.038	.042	0.97	1.07
G	.100 BASIC		2.54 BASIC	
H	.067	.085	1.70	2.16
J	.008	.012	0.20	0.30
K	.170 BASIC		4.32 BASIC	
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

ORDERING INFORMATION

Model	Temperature Range
ADC804BH	−25°C to +85°C
ADC804BHQ	−25°C to +85°C
ADC804SH	−55°C to +125°C
ADC804SHQ	−55°C to +125°C
BURN-IN SCREENING OPTION See text for details.	
Model	**Burn-In Temp. (160h)[1]**
ADC804BH-BI	+125°C
ADC804SHQ	+125°C

NOTE: Or equivalent combination. See text.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers. The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1, which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and

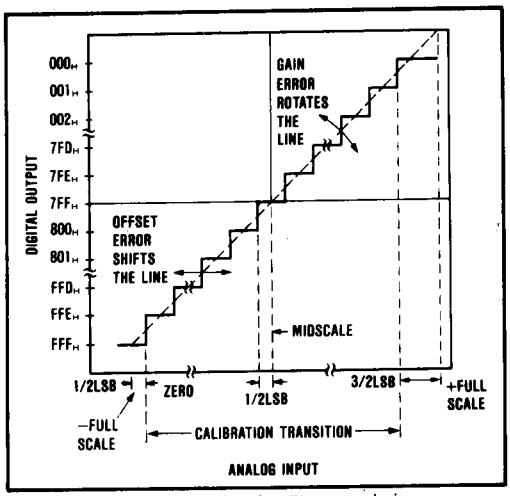


FIGURE 1. ADC804 Transfer Characteristic Terminology.

code definitions for each possible ADC804 analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC804 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. The ADC804BH is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range of −25°C to +85°C, and the ADC804SH displays no missing codes over the temperature range of −55°C to +125°C.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC804 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC804 follows this convention. Thus, bipolar offset error for the ADC804 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC804 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

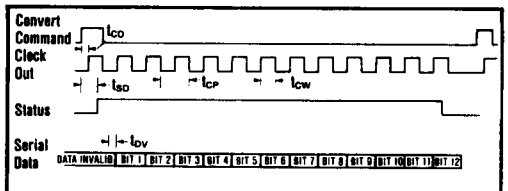
Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB*	COB*	COB*	CSB**	CSB**
One Least Significant Bit (LSB)	FSR/2^n n = 12	20V/2^n 4.88mV	10V/2^n 2.44mV	5V/2^n 1.22mV	10V/2^n 2.44mV	5V/2^n 1.22mV
Transition Values MSB LSB 001_H to 000_H 800_H to $7FF_H$ FFF_H to FFE_H	 +Full Scale Mid Scale −Full Scale	 +10V − 3/2LSB 0 −10V + 1/2LSB	 +5V − 3/2LSB 0 −5V + 1/2LSB	 +2.5V − 3/2LSB 0 −2.5V + 1/2LSB	 + 10V − 3/2LSB +5V 0 + 1/2LSB	 +5V − 3/2LSB + 2.5V 0 + 1/2LSB

*COB = Complementary Offset Binary **CSB = Complementary Straight Binary

course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC804 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 1.2μsec to obtain the specified conversion time with internal clock, the ADC804 will accept longer convert commands with no loss of accuracy, assuming that the



Symbol	Parameter	Typ	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.1	μsec
t_{CW}	Nominal clock pulse width	0.55	μsec
t_{SD}	Status delay from convert command	130	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC804 Timing Diagram (normal values at +25°C with internal clock).

analog input signal is stable. In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 600nsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 15μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the thirteenth clock pulse. A new conversion may not be initiated until 50nsec after the fall of the thirteenth clock pulse. Additional convert commands applied during conversion will be ignored.

DEFINITION OF DIGITAL CODES

Two binary codes are available on the serial output of the ADC804, complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input ranges. Both are complementary codes, meaning that logic "0" is true. Serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. All clock pulses available from the ADC804 have a nominal pulse width of 550nsec to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC804 but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use a wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC804 as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC804 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC804 offers five standard input ranges: 0V to+5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate

input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may be easily increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 6.

TABLE II. ADC804 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 8 To Pin	Connect Pin 10 To	Connect Input Signal To
±10V	COB	7	Input Signal	10
±5V	COB	7	Open	9
±2.5V	COB	7	Pin 7	9
0 to +5V	CSB	11	Pin 7	9
0 to +10V	CSB	11	Open	9

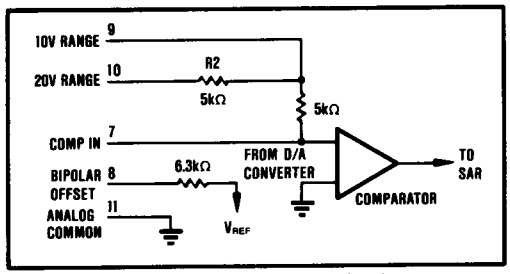


FIGURE 3. ACD804 Input Scaling Circuit.

REPLACEMENT OF ADC80

As illustrated in Figure 4, a circuit board configured for use of the ADC80 serial output capability may be very easily adapted to also use the ADC804, or to achieve space savings due to the smaller package of the ADC804. The pin assignments of the ADC804 have been chosen to allow it to fit neatly into one corner of the ADC80 layout. When replacing ADC80 with ADC804, a board space improvement of approximately 1.25 square inches (8.06cm^2) is obtained.

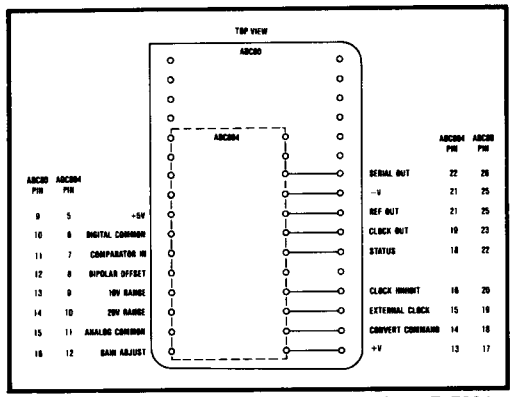


FIGURE 4. Adapting an ADC80 Layout for ADC804.

CALIBRATION

Optional External Gain and Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC804 as shown in Figures 5 and 6 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These potentiometers may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 12 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

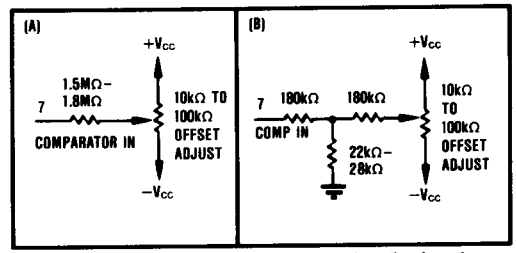


FIGURE 5. Two Methods of Connecting Optional Offset Adjust.

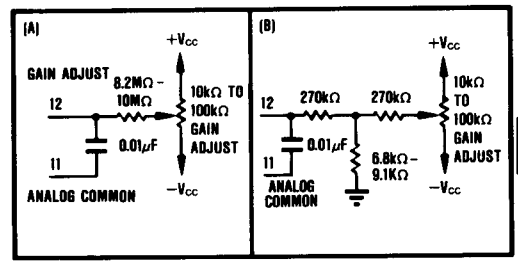


FIGURE 6. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 5. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V + 2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE$_H$ and FFF$_H$ with approximately 50% occurrence of each of the two codes. In other words, the potentiomter is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 6. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V − 7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC804 is extremely versatile in that it can be operated with either internal or external clock. Thus, use of an available system clock enables synchronization of the converter to the rest of the system to optimize performance in a noisy environment.

When operating with the internal clock, pin 15 (external clock input) and pin 16 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC804. Pin 16 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 15.

See Figures 7 through 10 for diagrams to implement the various clock options.

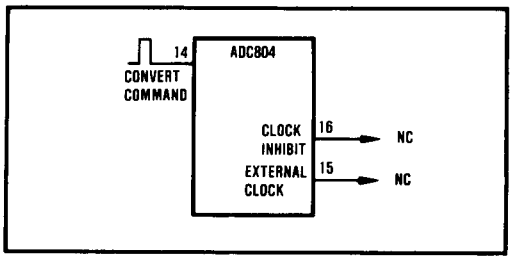


FIGURE 7. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models

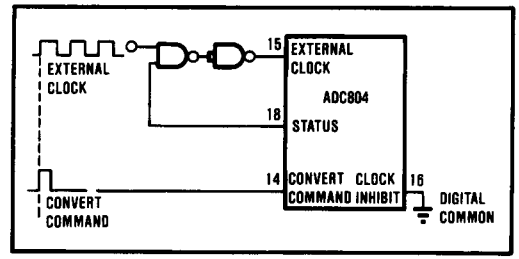


FIGURE 8. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

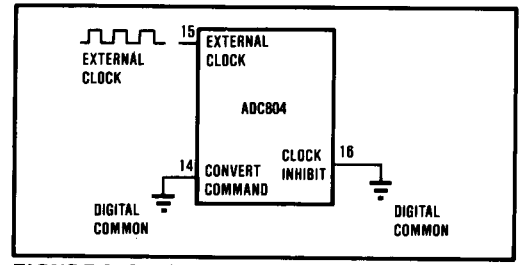


FIGURE 9. Continuous Conversion with external Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

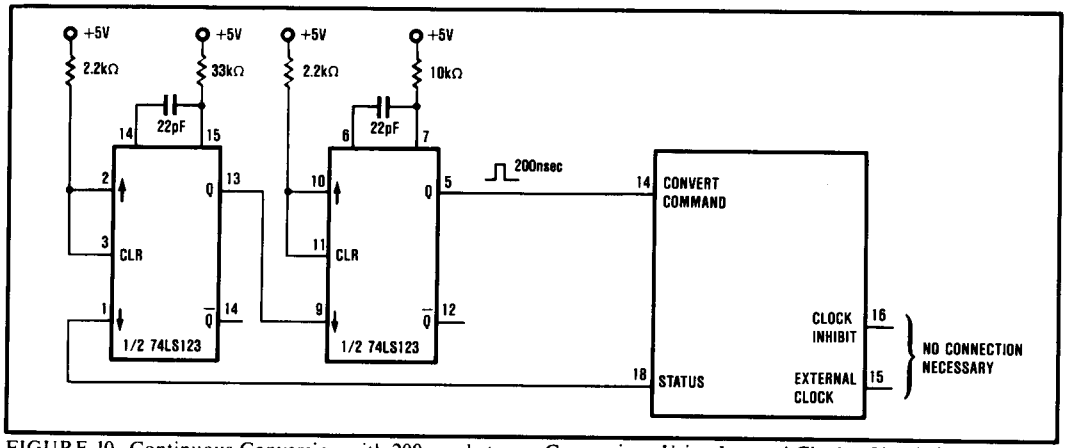


FIGURE 10. Continuous Conversion with 200nsec between Conversions Using Internal Clock. (Circuit insures that the conversion process will start when power is applied.)

are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

BURN-IN SCREENING

Burn-in screening is an option available for the ADC804. Burn-in duration is 160 hours at +125°C ambient temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "BI" to the base model number.

TABLE III. Screening Flow for ADC804xHQ

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-In	1015, B	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC4118	