

CSE4117 – Microprocessors



HOMEWORK-4

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EXPLANATIONS

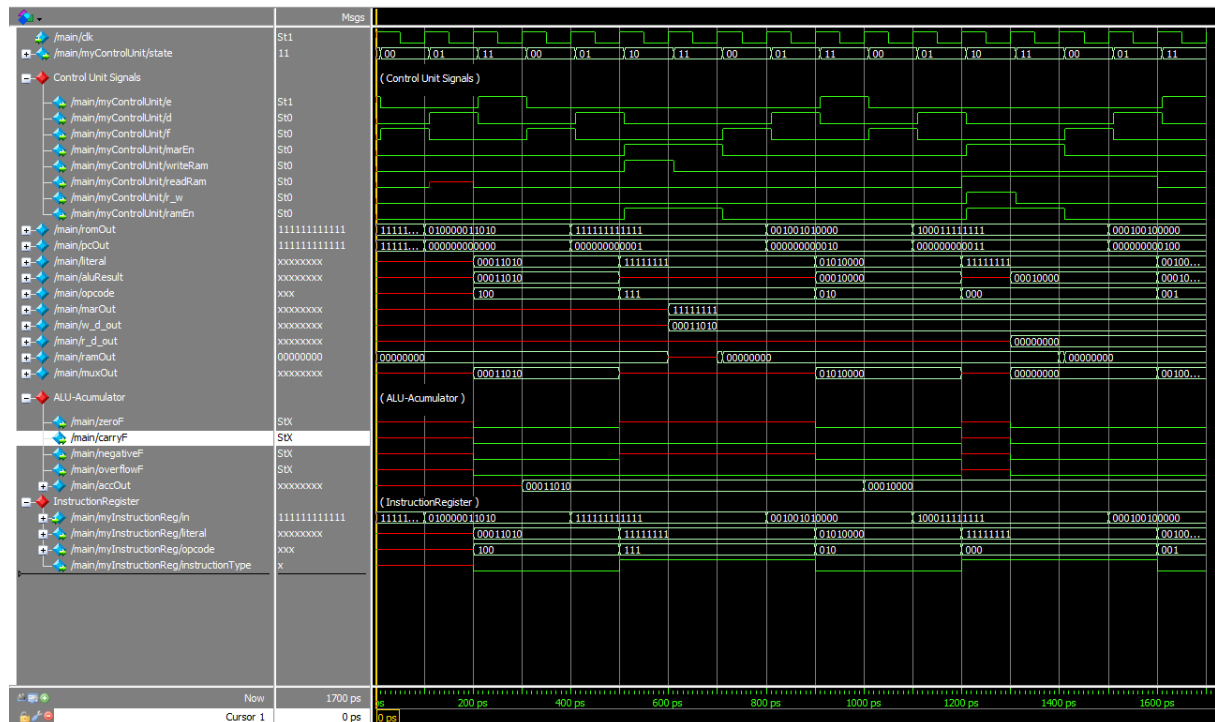
In this homework, firstly we combined the ram in our second homework and the last version of the alu that we designed. Also we added a rom to take the instructions.

The control unit produces **ramEn**, **r_w**, **readRam**, **writeRam**, **marEn** in addition to 'fetch', 'decode' and 'execute', then these signals connects to related structures. To produce these signals respectively we implemented a final state machine in the control unit.

We simulated our model and we obtained partially successful results.

In the simulation below there are five instructions executed which are (1 bit instruction type, 3 bits operation code, 8 bits literal / address):

- MOVA 26 (0 100 00011010) => // Accumulator = 26
- STORER 0xFF (1 111 11111111) => // The value at address 0xFF = 26
- ANDA 80 (0 010 01010000) => // Accumulator = Accumulator & 80
- ADDR 0xFF (1 000 11111111) => // Accumulator = Accumulator + The value at address 0xFF
- SUBA 32 (0 001 00100000) => // Accumulator = 32 - Accumulator



OUR SOURCE CODE:

Main:

```
// Aydin DUYGU - 150118981
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```

```
//-----
```

```
module onebitsubtractor(input a, input b, input c_in, output c_out, output result);
```

```
assign c_out = (~a&b)|(b&c_in)|(~a&c_in);
```

```
assign result = (a ^ b) ^ c_in;
```

```
endmodule
```

```
//-----
```

```
module twobitsubtractor(input [1:0]a,input [1:0]b, input c_in, output c_out, output [1:0] result);
```

```
wire cout;
```

```
onebitsubtractor s0(a[0],b[0],c_in,cout,result[0]);
```

```
onebitsubtractor s1(a[1],b[1],cout,c_out,result[1]);
```

```
endmodule
```

```
//-----
```

```
module fourbitsubtractor(input [3:0]a,input [3:0]b, input c_in, output c_out, output [3:0] result);
```

```
wire cout;
```

```
twobitsubtractor s0(a[1:0],b[1:0],c_in,cout,result[1:0]);
```

```
twobitsubtractor s1(a[3:2],b[3:2],cout,c_out,result[3:2]);
```

```
endmodule
```

```
//-----
```

```
module eightbitsubtractor(input [7:0]a,input [7:0]b, input c_in, output c_out, output [7:0] result);
```

```
wire cout;
```

```
fourbitsubtractor s0(a[3:0],b[3:0],c_in,cout,result[3:0]);
```

```
fourbitsubtractor s1(a[7:4],b[7:4],cout,c_out,result[7:4]);
```

```
endmodule
```

```
//-----
```

```
module fulladder(
```

```
input [7:0] a,
```

```
input [7:0] b,
```

```
input c_in,
```

```
output reg c_out,
```

```
output reg [7:0] resultFullAdder);
```

```
always @(a or b or c_in)
```

```
begin
```

```
{c_out, resultFullAdder} = a+b+c_in;
```

```
end
```

```
endmodule
```

```
//-----
```

```
module mux2to1(in0,in1,sel0,out);
```

```
input[7:0] in0,in1;
```

```
input sel0;
```

```
output[7:0] out;
```

```
assign out[7] = (in0[7] & ~sel0)|(in1[7] & sel0);
```

```
assign out[6] = (in0[6] & ~sel0)|(in1[6] & sel0);
assign out[5] = (in0[5] & ~sel0)|(in1[5] & sel0);
assign out[4] = (in0[4] & ~sel0)|(in1[4] & sel0);
assign out[3] = (in0[3] & ~sel0)|(in1[3] & sel0);
assign out[2] = (in0[2] & ~sel0)|(in1[2] & sel0);
assign out[1] = (in0[1] & ~sel0)|(in1[1] & sel0);
assign out[0] = (in0[0] & ~sel0)|(in1[0] & sel0);
```

```
endmodule
```

```
//-----
module mux4to1(in0,in1,in2,in3,sel0,sel1,out);
```

```
input[7:0] in0,in1,in2,in3;
input sel0,sel1;
output[7:0] out;
wire[7:0] w1,w2;
```

```
mux2to1 m1(in0,in1,sel0,w1);
mux2to1 m2(in2,in3,sel0,w2);
mux2to1 m3(w1,w2,sel1,out);
```

```
endmodule
```

```
//-----
module mux_8to1(in0,in1,in2,in3,in4,in5,in6,in7,sel0,sel1,sel2,out);
```

```
input[7:0] in0,in1,in2,in3,in4,in5,in6,in7;
input sel0,sel1,sel2;
output[7:0] out;
wire[7:0] w1,w2;
```

```
mux4to1 m1(in0,in1,in2,in3,sel0,sel1,w1);
mux4to1 m2(in4,in5,in6,in7,sel0,sel1,w2);
mux2to1 m3(w1,w2,sel2,out);
```

```
endmodule
```

```
//-----
module alu(a, b, opSel, zeroF, carryF, negativeF, overflowF, result);
```

```
input [7:0] a, b;
input [2:0] opSel;
output zeroF, negativeF, carryF, overflowF;
output [7:0] result;
wire [7:0] result0, result1, result2, result3, result4, result5, result6, result7;
wire carryFS, carryFA;
```

```
fulladder f(a, b, 0, carryFA, result0);
eightbitsubtractor s(a, b, 0, carryFS, result1);
assign result2 = a & b;
assign result3 = a | b;
assign result4 = a;
assign result5 = b << 1;
assign result6 = b >> 1;
assign result7 = a ^ b;
```

```
    mux_8to1 mux1(result0, result1, result2, result3, result4, result5, result6, result7, opSel[0], opSel[1], opSel[2],
result);
```

```
    assign zeroF = ~(result[7] | result[6] | result[5] | result[4] | result[3] | result[2] | result[1] | result[0]);
    assign negativeF = result[7] ;
```

```
    assign overflowF = (((~a[7] & ~b[7] & result[7]) | (a[7] & b[7] & ~result[7])) & (~opSel[0] & ~opSel[1] &
~opSel[2])) |
                        (((~a[7] & b[7] & result[7]) | (a[7] & ~b[7] & ~result[7])) & (opSel[0] & ~opSel[1] &
~opSel[2]));
```

```
    assign carryF = (~opSel[0] & ~opSel[1] & ~opSel[2] & carryFA) | (opSel[0] & ~opSel[1] & ~opSel[2] &
carryFS);
```

```
endmodule
```

```
//-----
// FIRST ASSIGNMENT UNTIL HERE
//-----
```

```
//-----
module accumulator(accIn, e, clk, accOut);
```

```
    input [7:0] accIn;
    input e, clk;
    output [7:0] accOut;
    reg [7:0] accOut;
```

```
    always @ (posedge clk) begin
        if(e == 1)
            accOut = accIn;
        end
    endmodule
```

```
//-----
module instruction_register(in, d, clk, literal, opcode, instructionType);
```

```
    // instructionType: 1bit + opcode: 3 bits + value: 8 bits
    input [11:0] in;
    input d, clk;
    output [7:0] literal;
    reg [7:0] literal;
    output [2:0] opcode;
    reg [2:0] opcode;
```

```
    output instructionType;
    reg instructionType;
```

```
    always @ (posedge clk)
    begin
        if (d == 1) begin
```

```

literal[0] <= in[0];
literal[1] <= in[1];
literal[2] <= in[2];
literal[3] <= in[3];
literal[4] <= in[4];
literal[5] <= in[5];
literal[6] <= in[6];
literal[7] <= in[7];
opcode[0] <= in[8];
opcode[1] <= in[9];
opcode[2] <= in[10];
instructionType<=in[11];
end
end

endmodule

//-----
module controlUnit(instructionTypeInput,opcode,clk,state,e,d,f,marEn,writeRam,readRam,r_w,ramEn);

input instructionTypeInput;
input [2:0] opcode;

input clk;
output e,d,f,marEn,writeRam,readRam,r_w,ramEn;

output [1:0] state;
reg [1:0] state = 2'b11;

reg firstRun=1;
reg instructionType;

assign f=(~state[1])&(~state[0]);
assign d=(~state[1])&(state[0]);
assign e=(state[1])&(state[0])&(~instructionType);
assign marEn=((state[1])&(state[0])&instructionType)&(state[1]&~state[0]);
assign writeRam=(instructionType&(opcode[2]&opcode[1]&opcode[0])&((state[1])&(~state[0])));

assign readRam=(instructionType&( ~(opcode[2]&opcode[1]&opcode[0])));

assign r_w=(instructionType&( ~(opcode[2]&opcode[1]&opcode[0]))&((state[1])&(~state[0])));

assign ramEn=((state[1])&(state[0])&instructionType)&(state[1]&~state[0]);

initial begin
if(firstRun==1) instructionType<=0;

else instructionType<=instructionTypeInput;
end

```

```

always@(*) begin

    if(~state[1]&state[0])begin
        firstRun<=0;
        instructionType<=instructionTypeInput;
        end

end

always @ (posedge clk)begin

    #10

    state[0]<=(~state[0]&~state[1])|(state[0]&~state[1]&~instructionType)|(instructionType&state[1]&~state[0]);
    state[1]<=(~state[1]&state[0])|(instructionType&state[1]&~state[0]);

end

endmodule

//-----

module programCounter(clk,f,out);

input clk,f;
output[11:0] out;
reg[11:0] out=12'b111111111111;

always @ (posedge clk)

begin

if(f==1) begin
out=out+1;
end
end

endmodule

//-----

module mar(clk, in, out, en);

input clk,en;
input [7:0] in;
output [7:0] out;
reg [7:0] out;

always @ (posedge clk)

begin

if(en==1)out<=in;

```

```
end
```

```
endmodule
```

```
//-----
```

```
module w_d (clk, in, out, en);
```

```
    input clk,en;  
    input [7:0] in;  
    output [7:0] out;  
    reg [7:0] out;
```

```
    always @ (posedge clk)
```

```
        begin
```

```
            if(en==1)out<=in;
```

```
        end
```

```
endmodule
```

```
//-----
```

```
module r_d (clk, in, out, en);
```

```
    input clk,en;  
    input [7:0] in;  
    output [7:0] out;  
    reg [7:0] out;
```

```
    always @ (posedge clk)begin
```

```
        if(en==1)out<=in;
```

```
    end
```

```
endmodule
```

```
//-----
```

```
module main(clk,zeroF, carryF, negativeF, overflowF);
```

```
    input clk;
```

```
    wire [11:0] romOut,pcOut;  
    wire [7:0] literal,aluResult;  
    wire instructionType;  
    wire [2:0] opcode;  
    wire e,d,f;  
    wire [7:0] marOut,w_d_out,r_d_out,ramOut,muxOut;  
    wire marEn,readRam,writeRam,r_w,ramEn;
```

```
    output zeroF, carryF, negativeF, overflowF;
```



```

wire [7:0] accOut;

controlUnit myControlUnit(instructionType,opcode,clk,state,e,d,f,marEn,writeRam,readRam,r_w,ramEn);

programCounter pc(clk,f,pcOut);

rom myrom(pcOut,romOut);

instruction_register myInstructionReg(romOut,d, clk, literal, opcode,instructionType);

mar mymar(clk,literal,marOut,marEn);

w_d mywd(clk,accOut,w_d_out,writeRam);

ram myram(w_d_out,r_w,clk,ramOut,marOut,ramEn);

r_d myrd(clk,ramOut,r_d_out,readRam);

mux2to1 mymux(literal,r_d_out,instructionType,muxOut);

alu myALU(muxOut, accOut, opcode, zeroF, carryF, negativeF, overflowF, aluResult);
accumulator myAccumulator(aluResult, e, clk, accOut);

endmodule

```

RAM:

```

module dflipflop(d, q, clk);

input d, clk;
output q;
reg q;
always @ (posedge clk)
begin

q <= d;
end

endmodule

//-----
module binarycell(sel, dataIn, rw, clk, dataOut);

input dataIn, clk, sel, rw;
output dataOut;
wire w1, w2, q;
reg dataOut;

```

```

assign w1 = (sel & ~rw);

assign w2 = w1 ? dataIn : dataOut;

dflop binflop(w2, q, clk);

always @ ( * ) begin

dataOut <= (sel & q);
end

endmodule

//-----
module decoder_4to16(a1, a2, a3, a4, e, dOut);
input  a1, a2, a3, a4, e;
output [15:0] dOut;

assign dOut[0] = (~a1) & (~a2) & (~a3) & (~a4) & (e);
assign dOut[1] = (~a1) & (~a2) & (~a3) & (a4) & (e);
assign dOut[2] = (~a1) & (~a2) & (a3) & (~a4) & (e);
assign dOut[3] = (~a1) & (~a2) & (a3) & (a4) & (e);
assign dOut[4] = (~a1) & (a2) & (~a3) & (~a4) & (e);
assign dOut[5] = (~a1) & (a2) & (~a3) & (a4) & (e);
assign dOut[6] = (~a1) & (a2) & (a3) & (~a4) & (e);
assign dOut[7] = (~a1) & (a2) & (a3) & (a4) & (e);
assign dOut[8] = (a1) & (~a2) & (~a3) & (~a4) & (e);
assign dOut[9] = (a1) & (~a2) & (~a3) & (a4) & (e);
assign dOut[10] = (a1) & (~a2) & (a3) & (~a4) & (e);
assign dOut[11] = (a1) & (~a2) & (a3) & (a4) & (e);
assign dOut[12] = (a1) & (a2) & (~a3) & (~a4) & (e);
assign dOut[13] = (a1) & (a2) & (~a3) & (a4) & (e);
assign dOut[14] = (a1) & (a2) & (a3) & (~a4) & (e);
assign dOut[15] = (a1) & (a2) & (a3) & (a4) & (e);

endmodule

//-----
module RamPart(dOut, data, rw, clk, out);

input [15:0] dOut;
input [7:0] data;
input rw, clk;
output [7:0] out;

wire out0000_1, out0001_1, out0010_1, out0011_1, out0100_1, out0101_1, out0110_1, out0111_1, out1000_1,
out1001_1, out1010_1, out1011_1, out1100_1, out1101_1, out1110_1, out1111_1;
wire out0000_2, out0001_2, out0010_2, out0011_2, out0100_2, out0101_2, out0110_2, out0111_2, out1000_2,
out1001_2, out1010_2, out1011_2, out1100_2, out1101_2, out1110_2, out1111_2;
wire out0000_3, out0001_3, out0010_3, out0011_3, out0100_3, out0101_3, out0110_3, out0111_3, out1000_3,
out1001_3, out1010_3, out1011_3, out1100_3, out1101_3, out1110_3, out1111_3;
wire out0000_4, out0001_4, out0010_4, out0011_4, out0100_4, out0101_4, out0110_4, out0111_4, out1000_4,
out1001_4, out1010_4, out1011_4, out1100_4, out1101_4, out1110_4, out1111_4;

```

```

wire out0000_5 , out0001_5 , out0010_5 , out0011_5 , out0100_5 , out0101_5 , out0110_5 , out0111_5 , out1000_5 ,
out1001_5 , out1010_5 , out1011_5 , out1100_5 , out1101_5 , out1110_5 , out1111_5;
wire out0000_6 , out0001_6 , out0010_6 , out0011_6 , out0100_6 , out0101_6 , out0110_6 , out0111_6 , out1000_6 ,
out1001_6 , out1010_6 , out1011_6 , out1100_6 , out1101_6 , out1110_6 , out1111_6;
wire out0000_7 , out0001_7 , out0010_7 , out0011_7 , out0100_7 , out0101_7 , out0110_7 , out0111_7 , out1000_7 ,
out1001_7 , out1010_7 , out1011_7 , out1100_7 , out1101_7 , out1110_7 , out1111_7;
wire out0000_8 , out0001_8 , out0010_8 , out0011_8 , out0100_8 , out0101_8 , out0110_8 , out0111_8 , out1000_8 ,
out1001_8 , out1010_8 , out1011_8 , out1100_8 , out1101_8 , out1110_8 , out1111_8;

```

```

//module binarycell(en,data,rw,clk,out);
binarycell cell_0000_1(dOut[0],data[0],rw,clk,out0000_1);
binarycell cell_0001_1(dOut[1],data[0],rw,clk,out0001_1);
binarycell cell_0010_1(dOut[2],data[0],rw,clk,out0010_1);
binarycell cell_0011_1(dOut[3],data[0],rw,clk,out0011_1);
binarycell cell_0100_1(dOut[4],data[0],rw,clk,out0100_1);
binarycell cell_0101_1(dOut[5],data[0],rw,clk,out0101_1);
binarycell cell_0110_1(dOut[6],data[0],rw,clk,out0110_1);
binarycell cell_0111_1(dOut[7],data[0],rw,clk,out0111_1);
binarycell cell_1000_1(dOut[8],data[0],rw,clk,out1000_1);
binarycell cell_1001_1(dOut[9],data[0],rw,clk,out1001_1);
binarycell cell_1010_1(dOut[10],data[0],rw,clk,out1010_1);
binarycell cell_1011_1(dOut[11],data[0],rw,clk,out1011_1);
binarycell cell_1100_1(dOut[12],data[0],rw,clk,out1100_1);
binarycell cell_1101_1(dOut[13],data[0],rw,clk,out1101_1);
binarycell cell_1110_1(dOut[14],data[0],rw,clk,out1110_1);
binarycell cell_1111_1(dOut[15],data[0],rw,clk,out1111_1);

```

```

binarycell cell_0000_2(dOut[0],data[1],rw,clk,out0000_2);
binarycell cell_0001_2(dOut[1],data[1],rw,clk,out0001_2);
binarycell cell_0010_2(dOut[2],data[1],rw,clk,out0010_2);
binarycell cell_0011_2(dOut[3],data[1],rw,clk,out0011_2);
binarycell cell_0100_2(dOut[4],data[1],rw,clk,out0100_2);
binarycell cell_0101_2(dOut[5],data[1],rw,clk,out0101_2);
binarycell cell_0110_2(dOut[6],data[1],rw,clk,out0110_2);
binarycell cell_0111_2(dOut[7],data[1],rw,clk,out0111_2);
binarycell cell_1000_2(dOut[8],data[1],rw,clk,out1000_2);
binarycell cell_1001_2(dOut[9],data[1],rw,clk,out1001_2);
binarycell cell_1010_2(dOut[10],data[1],rw,clk,out1010_2);
binarycell cell_1011_2(dOut[11],data[1],rw,clk,out1011_2);
binarycell cell_1100_2(dOut[12],data[1],rw,clk,out1100_2);
binarycell cell_1101_2(dOut[13],data[1],rw,clk,out1101_2);
binarycell cell_1110_2(dOut[14],data[1],rw,clk,out1110_2);
binarycell cell_1111_2(dOut[15],data[1],rw,clk,out1111_2);

```

```

binarycell cell_0000_3(dOut[0],data[2],rw,clk,out0000_3);
binarycell cell_0001_3(dOut[1],data[2],rw,clk,out0001_3);
binarycell cell_0010_3(dOut[2],data[2],rw,clk,out0010_3);
binarycell cell_0011_3(dOut[3],data[2],rw,clk,out0011_3);
binarycell cell_0100_3(dOut[4],data[2],rw,clk,out0100_3);
binarycell cell_0101_3(dOut[5],data[2],rw,clk,out0101_3);
binarycell cell_0110_3(dOut[6],data[2],rw,clk,out0110_3);
binarycell cell_0111_3(dOut[7],data[2],rw,clk,out0111_3);
binarycell cell_1000_3(dOut[8],data[2],rw,clk,out1000_3);
binarycell cell_1001_3(dOut[9],data[2],rw,clk,out1001_3);

```

```
binarycell cell_1010_3(dOut[10],data[2],rw,clk,out1010_3);
binarycell cell_1011_3(dOut[11],data[2],rw,clk,out1011_3);
binarycell cell_1100_3(dOut[12],data[2],rw,clk,out1100_3);
binarycell cell_1101_3(dOut[13],data[2],rw,clk,out1101_3);
binarycell cell_1110_3(dOut[14],data[2],rw,clk,out1110_3);
binarycell cell_1111_3(dOut[15],data[2],rw,clk,out1111_3);
```

```
binarycell cell_0000_4(dOut[0],data[3],rw,clk,out0000_4);
binarycell cell_0001_4(dOut[1],data[3],rw,clk,out0001_4);
binarycell cell_0010_4(dOut[2],data[3],rw,clk,out0010_4);
binarycell cell_0011_4(dOut[3],data[3],rw,clk,out0011_4);
binarycell cell_0100_4(dOut[4],data[3],rw,clk,out0100_4);
binarycell cell_0101_4(dOut[5],data[3],rw,clk,out0101_4);
binarycell cell_0110_4(dOut[6],data[3],rw,clk,out0110_4);
binarycell cell_0111_4(dOut[7],data[3],rw,clk,out0111_4);
binarycell cell_1000_4(dOut[8],data[3],rw,clk,out1000_4);
binarycell cell_1001_4(dOut[9],data[3],rw,clk,out1001_4);
binarycell cell_1010_4(dOut[10],data[3],rw,clk,out1010_4);
binarycell cell_1011_4(dOut[11],data[3],rw,clk,out1011_4);
binarycell cell_1100_4(dOut[12],data[3],rw,clk,out1100_4);
binarycell cell_1101_4(dOut[13],data[3],rw,clk,out1101_4);
binarycell cell_1110_4(dOut[14],data[3],rw,clk,out1110_4);
binarycell cell_1111_4(dOut[15],data[3],rw,clk,out1111_4);
```

```
binarycell cell_0000_5(dOut[0],data[4],rw,clk,out0000_5);
binarycell cell_0001_5(dOut[1],data[4],rw,clk,out0001_5);
binarycell cell_0010_5(dOut[2],data[4],rw,clk,out0010_5);
binarycell cell_0011_5(dOut[3],data[4],rw,clk,out0011_5);
binarycell cell_0100_5(dOut[4],data[4],rw,clk,out0100_5);
binarycell cell_0101_5(dOut[5],data[4],rw,clk,out0101_5);
binarycell cell_0110_5(dOut[6],data[4],rw,clk,out0110_5);
binarycell cell_0111_5(dOut[7],data[4],rw,clk,out0111_5);
binarycell cell_1000_5(dOut[8],data[4],rw,clk,out1000_5);
binarycell cell_1001_5(dOut[9],data[4],rw,clk,out1001_5);
binarycell cell_1010_5(dOut[10],data[4],rw,clk,out1010_5);
binarycell cell_1011_5(dOut[11],data[4],rw,clk,out1011_5);
binarycell cell_1100_5(dOut[12],data[4],rw,clk,out1100_5);
binarycell cell_1101_5(dOut[13],data[4],rw,clk,out1101_5);
binarycell cell_1110_5(dOut[14],data[4],rw,clk,out1110_5);
binarycell cell_1111_5(dOut[15],data[4],rw,clk,out1111_5);
```

```
binarycell cell_0000_6(dOut[0],data[5],rw,clk,out0000_6);
binarycell cell_0001_6(dOut[1],data[5],rw,clk,out0001_6);
binarycell cell_0010_6(dOut[2],data[5],rw,clk,out0010_6);
binarycell cell_0011_6(dOut[3],data[5],rw,clk,out0011_6);
binarycell cell_0100_6(dOut[4],data[5],rw,clk,out0100_6);
binarycell cell_0101_6(dOut[5],data[5],rw,clk,out0101_6);
binarycell cell_0110_6(dOut[6],data[5],rw,clk,out0110_6);
binarycell cell_0111_6(dOut[7],data[5],rw,clk,out0111_6);
binarycell cell_1000_6(dOut[8],data[5],rw,clk,out1000_6);
binarycell cell_1001_6(dOut[9],data[5],rw,clk,out1001_6);
binarycell cell_1010_6(dOut[10],data[5],rw,clk,out1010_6);
binarycell cell_1011_6(dOut[11],data[5],rw,clk,out1011_6);
binarycell cell_1100_6(dOut[12],data[5],rw,clk,out1100_6);
```

```
binarycell cell_1101_6(dOut[13],data[5],rw,clk,out1101_6);
binarycell cell_1110_6(dOut[14],data[5],rw,clk,out1110_6);
binarycell cell_1111_6(dOut[15],data[5],rw,clk,out1111_6);
```

```
binarycell cell_0000_7(dOut[0],data[6],rw,clk,out0000_7);
binarycell cell_0001_7(dOut[1],data[6],rw,clk,out0001_7);
binarycell cell_0010_7(dOut[2],data[6],rw,clk,out0010_7);
binarycell cell_0011_7(dOut[3],data[6],rw,clk,out0011_7);
binarycell cell_0100_7(dOut[4],data[6],rw,clk,out0100_7);
binarycell cell_0101_7(dOut[5],data[6],rw,clk,out0101_7);
binarycell cell_0110_7(dOut[6],data[6],rw,clk,out0110_7);
binarycell cell_0111_7(dOut[7],data[6],rw,clk,out0111_7);
binarycell cell_1000_7(dOut[8],data[6],rw,clk,out1000_7);
binarycell cell_1001_7(dOut[9],data[6],rw,clk,out1001_7);
binarycell cell_1010_7(dOut[10],data[6],rw,clk,out1010_7);
binarycell cell_1011_7(dOut[11],data[6],rw,clk,out1011_7);
binarycell cell_1100_7(dOut[12],data[6],rw,clk,out1100_7);
binarycell cell_1101_7(dOut[13],data[6],rw,clk,out1101_7);
binarycell cell_1110_7(dOut[14],data[6],rw,clk,out1110_7);
binarycell cell_1111_7(dOut[15],data[6],rw,clk,out1111_7);
```

```
binarycell cell_0000_8(dOut[0],data[7],rw,clk,out0000_8);
binarycell cell_0001_8(dOut[1],data[7],rw,clk,out0001_8);
binarycell cell_0010_8(dOut[2],data[7],rw,clk,out0010_8);
binarycell cell_0011_8(dOut[3],data[7],rw,clk,out0011_8);
binarycell cell_0100_8(dOut[4],data[7],rw,clk,out0100_8);
binarycell cell_0101_8(dOut[5],data[7],rw,clk,out0101_8);
binarycell cell_0110_8(dOut[6],data[7],rw,clk,out0110_8);
binarycell cell_0111_8(dOut[7],data[7],rw,clk,out0111_8);
binarycell cell_1000_8(dOut[8],data[7],rw,clk,out1000_8);
binarycell cell_1001_8(dOut[9],data[7],rw,clk,out1001_8);
binarycell cell_1010_8(dOut[10],data[7],rw,clk,out1010_8);
binarycell cell_1011_8(dOut[11],data[7],rw,clk,out1011_8);
binarycell cell_1100_8(dOut[12],data[7],rw,clk,out1100_8);
binarycell cell_1101_8(dOut[13],data[7],rw,clk,out1101_8);
binarycell cell_1110_8(dOut[14],data[7],rw,clk,out1110_8);
binarycell cell_1111_8(dOut[15],data[7],rw,clk,out1111_8);
```

```
assign out[0] = out0000_1 || out0001_1 || out0010_1 || out0011_1 || out0100_1 || out0101_1 || out0110_1 || out0111_1
|| out1000_1 || out1001_1 || out1010_1 || out1011_1 || out1100_1 || out1101_1 || out1110_1 || out1111_1;
assign out[1] = out0000_2 || out0001_2 || out0010_2 || out0011_2 || out0100_2 || out0101_2 || out0110_2 || out0111_2
|| out1000_2 || out1001_2 || out1010_2 || out1011_2 || out1100_2 || out1101_2 || out1110_2 || out1111_2;
assign out[2] = out0000_3 || out0001_3 || out0010_3 || out0011_3 || out0100_3 || out0101_3 || out0110_3 || out0111_3
|| out1000_3 || out1001_3 || out1010_3 || out1011_3 || out1100_3 || out1101_3 || out1110_3 || out1111_3;
assign out[3] = out0000_4 || out0001_4 || out0010_4 || out0011_4 || out0100_4 || out0101_4 || out0110_4 || out0111_4
|| out1000_4 || out1001_4 || out1010_4 || out1011_4 || out1100_4 || out1101_4 || out1110_4 || out1111_4;
assign out[4] = out0000_5 || out0001_5 || out0010_5 || out0011_5 || out0100_5 || out0101_5 || out0110_5 || out0111_5
|| out1000_5 || out1001_5 || out1010_5 || out1011_5 || out1100_5 || out1101_5 || out1110_5 || out1111_5;
assign out[5] = out0000_6 || out0001_6 || out0010_6 || out0011_6 || out0100_6 || out0101_6 || out0110_6 || out0111_6
|| out1000_6 || out1001_6 || out1010_6 || out1011_6 || out1100_6 || out1101_6 || out1110_6 || out1111_6;
assign out[6] = out0000_7 || out0001_7 || out0010_7 || out0011_7 || out0100_7 || out0101_7 || out0110_7 || out0111_7
|| out1000_7 || out1001_7 || out1010_7 || out1011_7 || out1100_7 || out1101_7 || out1110_7 || out1111_7;
assign out[7] = out0000_8 || out0001_8 || out0010_8 || out0011_8 || out0100_8 || out0101_8 || out0110_8 || out0111_8
|| out1000_8 || out1001_8 || out1010_8 || out1011_8 || out1100_8 || out1101_8 || out1110_8 || out1111_8;
```

```
endmodule
```

```
//-----
```

```
module ram(data, rw, clk, out, addr, EN);
```

```
input [7:0] addr;
```

```
input rw, clk, EN;
```

```
input[7:0] data;
```

```
output[7:0] out;
```

```
wire [7:0] out1, out2,out3,out4,out5,out6,out7,out8,out9,out10,out11,out12,out13,out14,out15,out16;
```

```
wire [15:0] dOut;
```

```
wire [15:0] d1_Out;
```

```
wire [15:0] d2_Out;
```

```
wire [15:0] d3_Out;
```

```
wire [15:0] d4_Out;
```

```
wire [15:0] d5_Out;
```

```
wire [15:0] d6_Out;
```

```
wire [15:0] d7_Out;
```

```
wire [15:0] d8_Out;
```

```
wire [15:0] d9_Out;
```

```
wire [15:0] d10_Out;
```

```
wire [15:0] d11_Out;
```

```
wire [15:0] d12_Out;
```

```
wire [15:0] d13_Out;
```

```
wire [15:0] d14_Out;
```

```
wire [15:0] d15_Out;
```

```
wire [15:0] d16_Out;
```

```
decoder_4to16 decoder(addr[7], addr[6], addr[5], addr[4], EN, dOut);
```

```
decoder_4to16 decoder1(addr[3], addr[2], addr[1], addr[0], dOut[0], d1_Out);
```

```
decoder_4to16 decoder2(addr[3], addr[2], addr[1], addr[0], dOut[1], d2_Out);
```

```
decoder_4to16 decoder3(addr[3], addr[2], addr[1], addr[0], dOut[2], d3_Out);
```

```
decoder_4to16 decoder4(addr[3], addr[2], addr[1], addr[0], dOut[3], d4_Out);
```

```
decoder_4to16 decoder5(addr[3], addr[2], addr[1], addr[0], dOut[4], d5_Out);
```

```
decoder_4to16 decoder6(addr[3], addr[2], addr[1], addr[0], dOut[5], d6_Out);
```

```
decoder_4to16 decoder7(addr[3], addr[2], addr[1], addr[0], dOut[6], d7_Out);
```

```
decoder_4to16 decoder8(addr[3], addr[2], addr[1], addr[0], dOut[7], d8_Out);
```

```
decoder_4to16 decoder9(addr[3], addr[2], addr[1], addr[0], dOut[8], d9_Out);
```

```
decoder_4to16 decoder10(addr[3], addr[2], addr[1], addr[0], dOut[9], d10_Out);
```

```
decoder_4to16 decoder11(addr[3], addr[2], addr[1], addr[0], dOut[10],d11_Out);
```

```
decoder_4to16 decoder12(addr[3], addr[2], addr[1], addr[0], dOut[11],d12_Out);
```

```
decoder_4to16 decoder13(addr[3], addr[2], addr[1], addr[0], dOut[12],d13_Out);
```

```
decoder_4to16 decoder14(addr[3], addr[2], addr[1], addr[0], dOut[13],d14_Out);
```

```
decoder_4to16 decoder15(addr[3], addr[2], addr[1], addr[0], dOut[14],d15_Out);
```

```
decoder_4to16 decoder16(addr[3], addr[2], addr[1], addr[0], dOut[15],d16_Out);
```

```
RamPart h1(d1_Out, data, rw, clk, out1);
```

```
RamPart h2(d2_Out, data, rw, clk, out2);
```

```
RamPart h3(d3_Out, data, rw, clk, out3);
```

```
RamPart h4(d4_Out, data, rw, clk, out4);
```

```
RamPart h5(d5_Out, data, rw, clk, out5);
```

```
RamPart h6(d6_Out, data, rw, clk, out6);
```

```
RamPart h7(d7_Out, data, rw, clk, out7);
```

```
RamPart h8(d8_Out, data, rw, clk, out8);
```

```

RamPart h9(d9_Out, data, rw, clk, out9);
RamPart h10(d10_Out, data, rw, clk, out10);
RamPart h11(d11_Out, data, rw, clk, out11);
RamPart h12(d12_Out, data, rw, clk, out12);
RamPart h13(d13_Out, data, rw, clk, out13);
RamPart h14(d14_Out, data, rw, clk, out14);
RamPart h15(d15_Out, data, rw, clk, out15);
RamPart h16(d16_Out, data, rw, clk, out16);

assign out = out1 | out2 | out3 | out4 | out5 | out6 | out7 | out8 | out9 | out10 | out11 | out12 | out13 | out14 | out15 |
out16;

endmodule

```

ROM:

```

module rom(addr,out);

input[11:0] addr;
output [11:0] out;
reg[11:0] out;

always@ (*) begin

case(addr)

12'b000000000000 : out= 12'b010000011010;
12'b000000000001 : out= 12'b111111111111;
12'b000000000010 : out= 12'b001001010000;
12'b000000000011 : out= 12'b100011111111;
12'b000000000100 : out= 12'b000100100000;
12'b000000000101 : out= 12'b011101001011;
12'b000000000110 : out= 12'b111110100010;
12'b000000000111 : out= 12'b110011111111;
12'b000000001000 : out= 12'b101110100010;
12'b000000001001 : out= 12'b100111111111;
12'b000000001010 : out= 12'b111100001000;
12'b000000001011 : out= 12'b010000000010;
12'b000000001100 : out= 12'b111100001111;
12'b000000001101 : out= 12'b110000001000;
12'b000000001110 : out= 12'b111000001111;
12'b000000001111 : out= 12'b010100000011;
12'b000000010000 : out= 12'b001101111111;
12'b000000010001 : out= 12'b011000000100;
12'b000000010010 : out= 12'b111101100001;
12'b000000010011 : out= 12'b010000000111;
12'b000000010100 : out= 12'b101001100001;
12'b000000010101 : out= 12'b110100001111;
12'b000000010110 : out= 12'b000000110000;

```

```
// all operations were used
```

```
//-----
```

```
12'b0000000010111 : out= 12'b0000000010111;  
12'b0000000011000 : out= 12'b0000000011000;  
12'b0000000011001 : out= 12'b0000000011001;  
12'b0000000011010 : out= 12'b0000000011010;  
12'b0000000011011 : out= 12'b0000000011011;  
12'b0000000011100 : out= 12'b0000000011100;  
12'b0000000011101 : out= 12'b0000000011101;  
12'b0000000011110 : out= 12'b0000000011110;  
12'b0000000011111 : out= 12'b0000000011111;  
12'b0000000100000 : out= 12'b0000000100000;  
12'b0000000100001 : out= 12'b0000000100001;  
12'b0000000100010 : out= 12'b0000000100010;  
12'b0000000100011 : out= 12'b0000000100011;  
12'b0000000100100 : out= 12'b0000000100100;  
12'b0000000100101 : out= 12'b0000000100101;  
12'b0000000100110 : out= 12'b0000000100110;  
12'b0000000100111 : out= 12'b0000000100111;  
12'b0000000101000 : out= 12'b0000000101000;  
12'b0000000101001 : out= 12'b0000000101001;  
12'b0000000101010 : out= 12'b0000000101010;  
12'b0000000101011 : out= 12'b0000000101011;  
12'b0000000101100 : out= 12'b0000000101100;  
12'b0000000101101 : out= 12'b0000000101101;  
12'b0000000101110 : out= 12'b0000000101110;  
12'b0000000101111 : out= 12'b0000000101111;  
12'b0000000110000 : out= 12'b0000000110000;  
12'b0000000110001 : out= 12'b0000000110001;  
12'b0000000110010 : out= 12'b0000000110010;  
12'b0000000110011 : out= 12'b0000000110011;  
12'b0000000110100 : out= 12'b0000000110100;  
12'b0000000110101 : out= 12'b0000000110101;  
12'b0000000110110 : out= 12'b0000000110110;  
12'b0000000110111 : out= 12'b0000000110111;  
12'b0000000111000 : out= 12'b0000000111000;  
12'b0000000111001 : out= 12'b0000000111001;  
12'b0000000111010 : out= 12'b0000000111010;  
12'b0000000111011 : out= 12'b0000000111011;  
12'b0000000111100 : out= 12'b0000000111100;  
12'b0000000111101 : out= 12'b0000000111101;  
12'b0000000111110 : out= 12'b0000000111110;  
12'b0000000111111 : out= 12'b0000000111111;  
12'b0000001000000 : out= 12'b0000001000000;  
12'b0000001000001 : out= 12'b0000001000001;  
12'b0000001000010 : out= 12'b0000001000010;  
12'b0000001000011 : out= 12'b0000001000011;  
12'b0000001000100 : out= 12'b0000001000100;  
12'b0000001000101 : out= 12'b0000001000101;  
12'b0000001000110 : out= 12'b0000001000110;  
12'b0000001000111 : out= 12'b0000001000111;  
12'b0000001001000 : out= 12'b0000001001000;  
12'b0000001001001 : out= 12'b0000001001001;  
12'b0000001001010 : out= 12'b0000001001010;  
12'b0000001001011 : out= 12'b0000001001011;  
12'b0000001001100 : out= 12'b0000001001100;
```


[illegible]

[illegible]

12'b000010111101 : out= 12'b000010111101;
12'b000010111110 : out= 12'b000010111110;
12'b000010111111 : out= 12'b000010111111;
12'b000011000000 : out= 12'b000011000000;
12'b000011000001 : out= 12'b000011000001;
12'b000011000010 : out= 12'b000011000010;
12'b000011000011 : out= 12'b000011000011;
12'b000011000100 : out= 12'b000011000100;
12'b000011000101 : out= 12'b000011000101;
12'b000011000110 : out= 12'b000011000110;
12'b000011000111 : out= 12'b000011000111;
12'b000011001000 : out= 12'b000011001000;
12'b000011001001 : out= 12'b000011001001;
12'b000011001010 : out= 12'b000011001010;
12'b000011001011 : out= 12'b000011001011;
12'b000011001100 : out= 12'b000011001100;
12'b000011001101 : out= 12'b000011001101;
12'b000011001110 : out= 12'b000011001110;
12'b000011001111 : out= 12'b000011001111;
12'b000011010000 : out= 12'b000011010000;
12'b000011010001 : out= 12'b000011010001;
12'b000011010010 : out= 12'b000011010010;
12'b000011010011 : out= 12'b000011010011;
12'b000011010100 : out= 12'b000011010100;
12'b000011010101 : out= 12'b000011010101;
12'b000011010110 : out= 12'b000011010110;
12'b000011010111 : out= 12'b000011010111;
12'b000011011000 : out= 12'b000011011000;
12'b000011011001 : out= 12'b000011011001;
12'b000011011010 : out= 12'b000011011010;
12'b000011011011 : out= 12'b000011011011;
12'b000011011100 : out= 12'b000011011100;
12'b000011011101 : out= 12'b000011011101;
12'b000011011110 : out= 12'b000011011110;
12'b000011011111 : out= 12'b000011011111;
12'b000011100000 : out= 12'b000011100000;
12'b000011100001 : out= 12'b000011100001;
12'b000011100010 : out= 12'b000011100010;
12'b000011100011 : out= 12'b000011100011;
12'b000011100100 : out= 12'b000011100100;
12'b000011100101 : out= 12'b000011100101;
12'b000011100110 : out= 12'b000011100110;
12'b000011100111 : out= 12'b000011100111;
12'b000011101000 : out= 12'b000011101000;
12'b000011101001 : out= 12'b000011101001;
12'b000011101010 : out= 12'b000011101010;
12'b000011101011 : out= 12'b000011101011;
12'b000011101100 : out= 12'b000011101100;
12'b000011101101 : out= 12'b000011101101;
12'b000011101110 : out= 12'b000011101110;
12'b000011101111 : out= 12'b000011101111;
12'b000011110000 : out= 12'b000011110000;
12'b000011110001 : out= 12'b000011110001;
12'b000011110010 : out= 12'b000011110010;
12'b000011110011 : out= 12'b000011110011;
12'b000011110100 : out= 12'b000011110100;

12'b000011110101 : out= 12'b000011110101;
12'b000011110110 : out= 12'b000011110110;
12'b000011110111 : out= 12'b000011110111;
12'b000011111000 : out= 12'b000011111000;
12'b000011111001 : out= 12'b000011111001;
12'b000011111010 : out= 12'b000011111010;
12'b000011111011 : out= 12'b000011111011;
12'b000011111100 : out= 12'b000011111100;
12'b000011111101 : out= 12'b000011111101;
12'b000011111110 : out= 12'b000011111110;
12'b000011111111 : out= 12'b000011111111;
12'b000100000000 : out= 12'b000100000000;
12'b000100000001 : out= 12'b000100000001;
12'b000100000010 : out= 12'b000100000010;
12'b000100000011 : out= 12'b000100000011;
12'b000100000100 : out= 12'b000100000100;
12'b000100000101 : out= 12'b000100000101;
12'b000100000110 : out= 12'b000100000110;
12'b000100000111 : out= 12'b000100000111;
12'b000100001000 : out= 12'b000100001000;
12'b000100001001 : out= 12'b000100001001;
12'b000100001010 : out= 12'b000100001010;
12'b000100001011 : out= 12'b000100001011;
12'b000100001100 : out= 12'b000100001100;
12'b000100001101 : out= 12'b000100001101;
12'b000100001110 : out= 12'b000100001110;
12'b000100001111 : out= 12'b000100001111;
12'b000100010000 : out= 12'b000100010000;
12'b000100010001 : out= 12'b000100010001;
12'b000100010010 : out= 12'b000100010010;
12'b000100010011 : out= 12'b000100010011;
12'b000100010100 : out= 12'b000100010100;
12'b000100010101 : out= 12'b000100010101;
12'b000100010110 : out= 12'b000100010110;
12'b000100010111 : out= 12'b000100010111;
12'b000100011000 : out= 12'b000100011000;
12'b000100011001 : out= 12'b000100011001;
12'b000100011010 : out= 12'b000100011010;
12'b000100011011 : out= 12'b000100011011;
12'b000100011100 : out= 12'b000100011100;
12'b000100011101 : out= 12'b000100011101;
12'b000100011110 : out= 12'b000100011110;
12'b000100011111 : out= 12'b000100011111;
12'b000100100000 : out= 12'b000100100000;
12'b000100100001 : out= 12'b000100100001;
12'b000100100010 : out= 12'b000100100010;
12'b000100100011 : out= 12'b000100100011;
12'b000100100100 : out= 12'b000100100100;
12'b000100100101 : out= 12'b000100100101;
12'b000100100110 : out= 12'b000100100110;
12'b000100100111 : out= 12'b000100100111;
12'b000100101000 : out= 12'b000100101000;
12'b000100101001 : out= 12'b000100101001;
12'b000100101010 : out= 12'b000100101010;
12'b000100101011 : out= 12'b000100101011;
12'b000100101100 : out= 12'b000100101100;

[illegible]

12'b000101100101 : out= 12'b000101100101;
12'b000101100110 : out= 12'b000101100110;
12'b000101100111 : out= 12'b000101100111;
12'b000101101000 : out= 12'b000101101000;
12'b000101101001 : out= 12'b000101101001;
12'b000101101010 : out= 12'b000101101010;
12'b000101101011 : out= 12'b000101101011;
12'b000101101100 : out= 12'b000101101100;
12'b000101101101 : out= 12'b000101101101;
12'b000101101110 : out= 12'b000101101110;
12'b000101101111 : out= 12'b000101101111;
12'b000101110000 : out= 12'b000101110000;
12'b000101110001 : out= 12'b000101110001;
12'b000101110010 : out= 12'b000101110010;
12'b000101110011 : out= 12'b000101110011;
12'b000101110100 : out= 12'b000101110100;
12'b000101110101 : out= 12'b000101110101;
12'b000101110110 : out= 12'b000101110110;
12'b000101110111 : out= 12'b000101110111;
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[illegible]

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[illegible]

[illegible]

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[illegible]

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[illegible]

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[illegible]

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12'b111110111001 : out= 12'b111110111001;
12'b111110111010 : out= 12'b111110111010;
12'b111110111011 : out= 12'b111110111011;
12'b111110111100 : out= 12'b111110111100;
12'b111110111101 : out= 12'b111110111101;
12'b111110111110 : out= 12'b111110111110;
12'b111110111111 : out= 12'b111110111111;
12'b111111000000 : out= 12'b111111000000;
12'b111111000001 : out= 12'b111111000001;
12'b111111000010 : out= 12'b111111000010;
12'b111111000011 : out= 12'b111111000011;
12'b111111000100 : out= 12'b111111000100;
12'b111111000101 : out= 12'b111111000101;
12'b111111000110 : out= 12'b111111000110;
12'b111111000111 : out= 12'b111111000111;
12'b111111001000 : out= 12'b111111001000;
12'b111111001001 : out= 12'b111111001001;
12'b111111001010 : out= 12'b111111001010;
12'b111111001011 : out= 12'b111111001011;
12'b111111001100 : out= 12'b111111001100;
12'b111111001101 : out= 12'b111111001101;
12'b111111001110 : out= 12'b111111001110;
12'b111111001111 : out= 12'b111111001111;
12'b111111010000 : out= 12'b111111010000;
12'b111111010001 : out= 12'b111111010001;
12'b111111010010 : out= 12'b111111010010;
12'b111111010011 : out= 12'b111111010011;
12'b111111010100 : out= 12'b111111010100;

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12'b111111010101 : out= 12'b111111010101;
12'b111111010110 : out= 12'b111111010110;
12'b111111010111 : out= 12'b111111010111;
12'b111111011000 : out= 12'b111111011000;
12'b111111011001 : out= 12'b111111011001;
12'b111111011010 : out= 12'b111111011010;
12'b111111011011 : out= 12'b111111011011;
12'b111111011100 : out= 12'b111111011100;
12'b111111011101 : out= 12'b111111011101;
12'b111111011110 : out= 12'b111111011110;
12'b111111011111 : out= 12'b111111011111;
12'b111111100000 : out= 12'b111111100000;
12'b111111100001 : out= 12'b111111100001;
12'b111111100010 : out= 12'b111111100010;
12'b111111100011 : out= 12'b111111100011;
12'b111111100100 : out= 12'b111111100100;
12'b111111100101 : out= 12'b111111100101;
12'b111111100110 : out= 12'b111111100110;
12'b111111100111 : out= 12'b111111100111;
12'b111111101000 : out= 12'b111111101000;
12'b111111101001 : out= 12'b111111101001;
12'b111111101010 : out= 12'b111111101010;
12'b111111101011 : out= 12'b111111101011;
12'b111111101100 : out= 12'b111111101100;
12'b111111101101 : out= 12'b111111101101;
12'b111111101110 : out= 12'b111111101110;
12'b111111101111 : out= 12'b111111101111;
12'b111111110000 : out= 12'b111111110000;
12'b111111110001 : out= 12'b111111110001;
12'b111111110010 : out= 12'b111111110010;
12'b111111110011 : out= 12'b111111110011;
12'b111111110100 : out= 12'b111111110100;
12'b111111110101 : out= 12'b111111110101;
12'b111111110110 : out= 12'b111111110110;
12'b111111110111 : out= 12'b111111110111;
12'b111111111000 : out= 12'b111111111000;
12'b111111111001 : out= 12'b111111111001;
12'b111111111010 : out= 12'b111111111010;
12'b111111111011 : out= 12'b111111111011;
12'b111111111100 : out= 12'b111111111100;
12'b111111111101 : out= 12'b111111111101;
12'b111111111110 : out= 12'b111111111110;
12'b111111111111 : out= 12'b111111111111;

endcase
end
endmodule

```

RTL:

Finally our RTL View (in closed shape) are presented below:

