Spring 2018

İSTANBUL BİLGİ UNIVERSITY
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EEEN 222 Digital Systems Design
Homework 02

Due: Midterm

Problem 1)
Convert each of the following Boolean expressions to product of sums form (POS) by employing the distributive law appropriately:

a. $x + yz' + x'z$

b. $abc'd + b'cd + ad'$

Problem 2)
Show that a set A containing only the gate @ described by the truth table is said to be a complete set. In other words, justify that any Boolean function can be implemented using only the gate @.

x	y	x@y
0	0	1
0	1	0
1	0	1
1	1	1

Problem 3)
Consider the following Boolean function:

$$F(A, B, C) = \sum m(1,3,6,7)$$

Simplify the Boolean function in **sum of products form** and **product of sums form** by means of a three variable Karnaugh map.

Problem 4)
Consider the following Boolean function with don't care conditions:

$$F(A, B, C, D) = \sum m(1,3,4,6,9,11)$$
$$d(A, B, C, D) = \sum m(0,2,5,10,12,14)$$

Simplify the Boolean function in **sum of products form** by means of a four variable Karnaugh map.

Problem 5)
Design a combinational logic circuit to detect an error in the representation of a decimal digit in BCD. In other words, write an equation with value 1 when the inputs are any of the six unused bit combinations in the BCD code, and value 0, otherwise.

a. Give a simplified expression of the error detector function in sum of products form.
b. Draw the 2-level NAND gate implementation of the corresponding logic circuit.
c. Give a simplified expression of the error detector function in product of sums form.
d. Draw the 2-level NOR gate implementation of the corresponding logic circuit.

Problem 6)
A combinational circuit is specified by the following three Boolean functions:

$$f = (b + c)' + a'b'c'$$
$$g = (a + c)' + ab'$$
$$h = bc' + (a + b')'$$

Design the circuit with a decoder of appropriate size and external gates if necessary.

Problem 7)

Implement the following Boolean functions using the indicated multiplexers.

a) $F(A, B, C) = A'C + B'C' + AC'$ with a 4-to-1 line multiplexer and external gates if necessary.
b) $F(A, B, C, D) = \sum(0,1,5,9,10,15)$ with a 4-to-1 line multiplexer and external gates if necessary.
c) $F(A, B, C, D) = \sum(1,3,4,11,12,13,14,15)$ with an 8-to-1 line multiplexer and external gates if necessary.