Selected Problems – VII

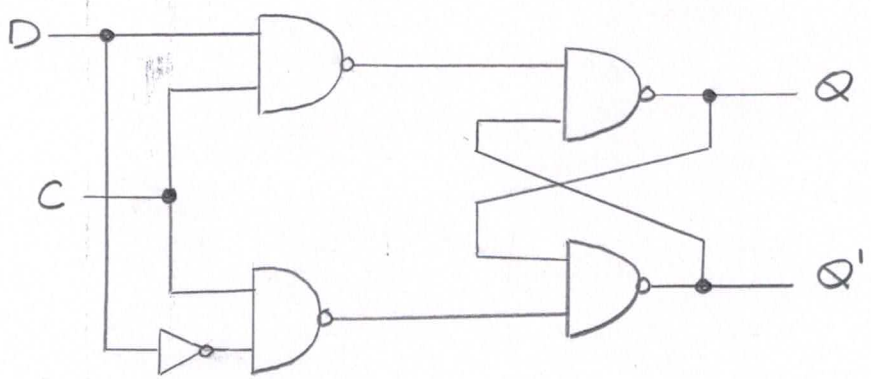
Problem 1) Consider the following ways for obtaining a D latch, and in each case draw the logic diagram and verify the circuit operation:

a. Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed

b. Use NOR gates for all four gates. Inverters may be needed.

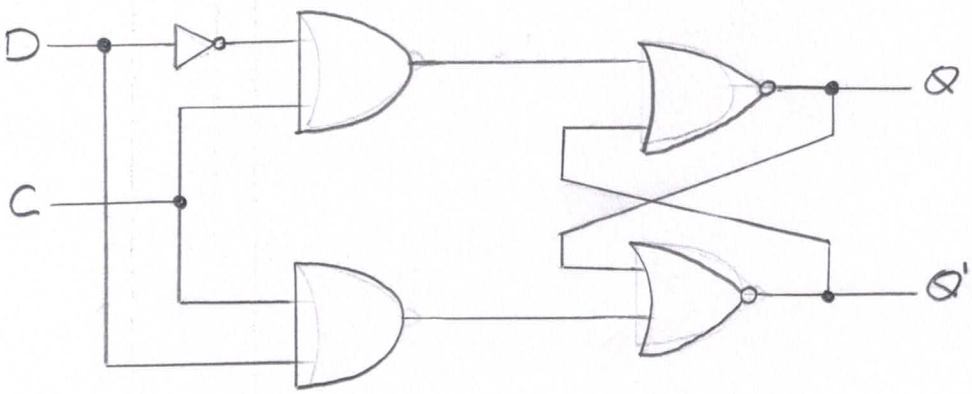
c. Use four NAND gates only (without an inverter).

Solution. We have a D latch constructed by four NAND gates plus an inverter



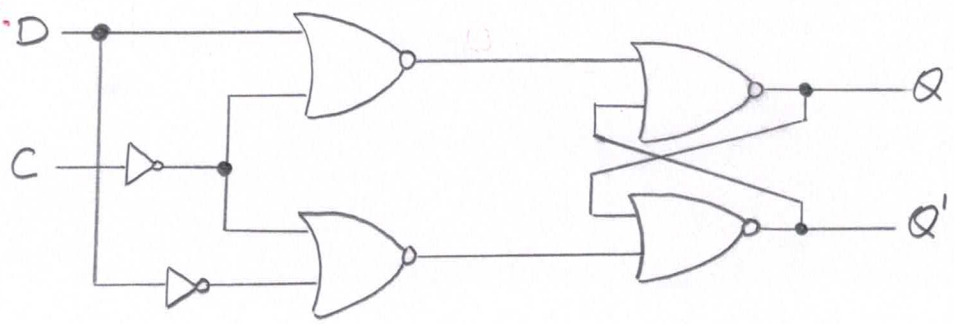
C	D	Q(t+1)
0	X	No change
1	0	0 (Reset)
1	1	1 (Set)

a.



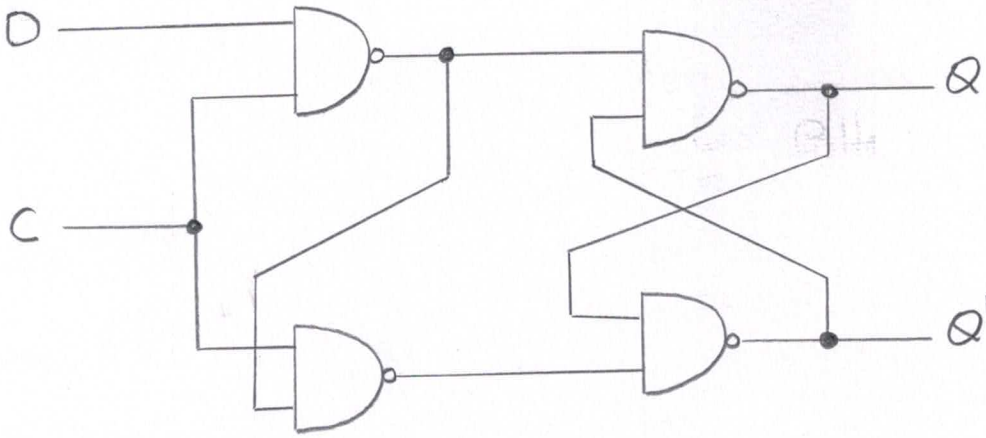
C	D	Q(t+1)
0	X	No change
1	0	0 (Reset)
1	1	1 (Set)

b.



C	D	Q(t+1)
0	X	No change
1	0	0 (Reset)
1	1	1 (Set)

c.



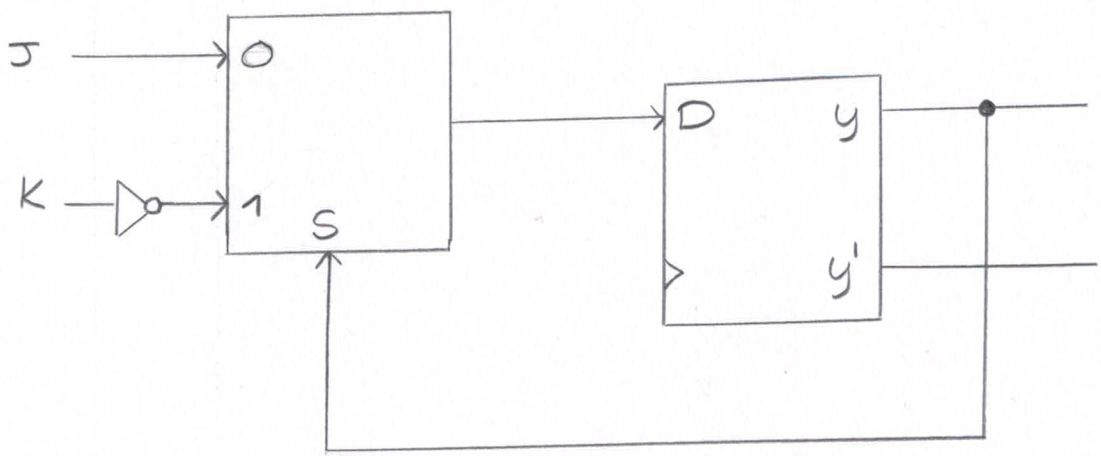
C	D	Q(t+1)
0	x	No change
1	0	0 (Reset)
1	1	1 (Set)

Problem 2) Construct a JK flip-flop using a D flip-flop, a 2-to-1-line multiplexer and an inverter.

Solution. Note that for a JK flip-flop, we have

$$Y = Jy' + K'y$$

-now choosing y as the select input of the 2-to-1-line multiplexer, and J as the 0-input and K' as the 1-input of the multiplexer gives



Problem 3) A PN flip-flop has four operations, clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

a. Tabulate the characteristic table.

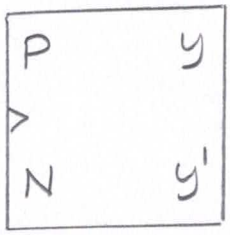
b. Derive the characteristic equation.

c. Tabulate the excitation table.

d. Show how the PN flip-flop can be converted to a D flip-flop.

Solution.

c.



P	N	Y	
0	0	0	Clear to 0
0	1	y	No change
1	0	y'	Complement
1	1	1	Set to 1

b.

y \ PN	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$Y = Py' + Ny + P'Ny$ "characteristic equation"

c.

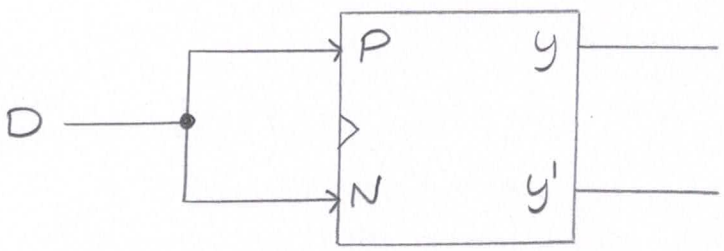
y \ Y	00	01	11	10
	0,d	1,d	d,1	d,0

"excitation table"

P,N

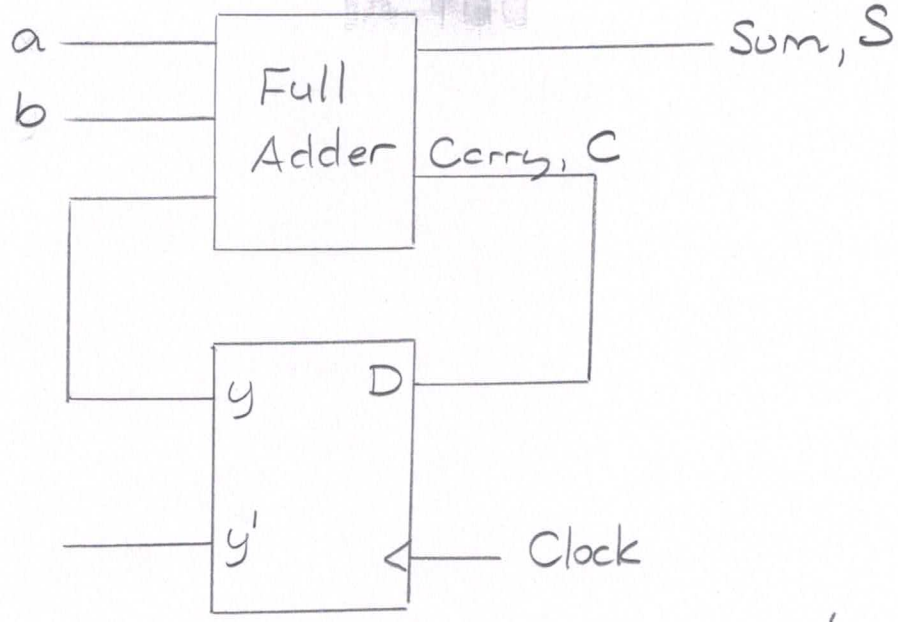
$0\{{0\atop 0}\ {1\atop 0}\}d \quad 1\{{1\atop 1}\ {1\atop 0}\}d \quad d\{{0\atop 1}\ {1\atop 1}\}1 \quad d\{{0\atop 1}\ {0\atop 0}\}0$

d. We simply drive P and N inputs of the PN flip-flop with the D input as follows



D	P	N	Y	
0	0	0		Clear to 0
1	1	1		Set to 1

Problem 4) Consider the following sequential circuit shown as



a. Derive the state table of the sequential circuit.
b. Draw the state diagram of the sequential circuit

Solution. We have

$$S = a \oplus b \oplus y \quad \text{"output eqn."}$$

$$C = ab + (a \oplus b)y \quad \text{"flip-flop input eqn."}$$

Hence;

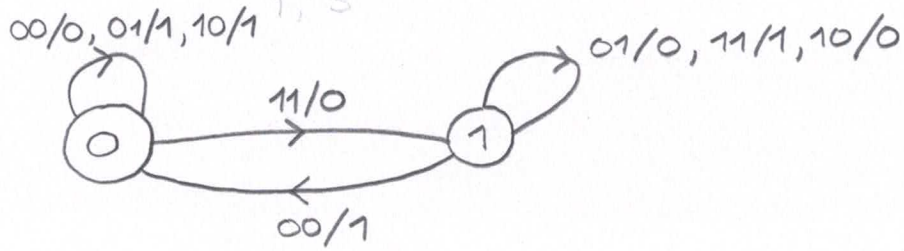
$$Y = D = ab + (a \oplus b)y$$

a.

y \ ab	00	01	11	10
0	0,0	0,1	1,0	0,1
1	0,1	1,0	1,1	1,0

Y, S

b.



Problem 5) A sequential circuit with two D flip-flops, two inputs x and y, and one output z is specified by the following next state and output equations

$$A(t+1) = x'y + xB$$

$$B(t+1) = x'A + xB$$

$$z = A$$

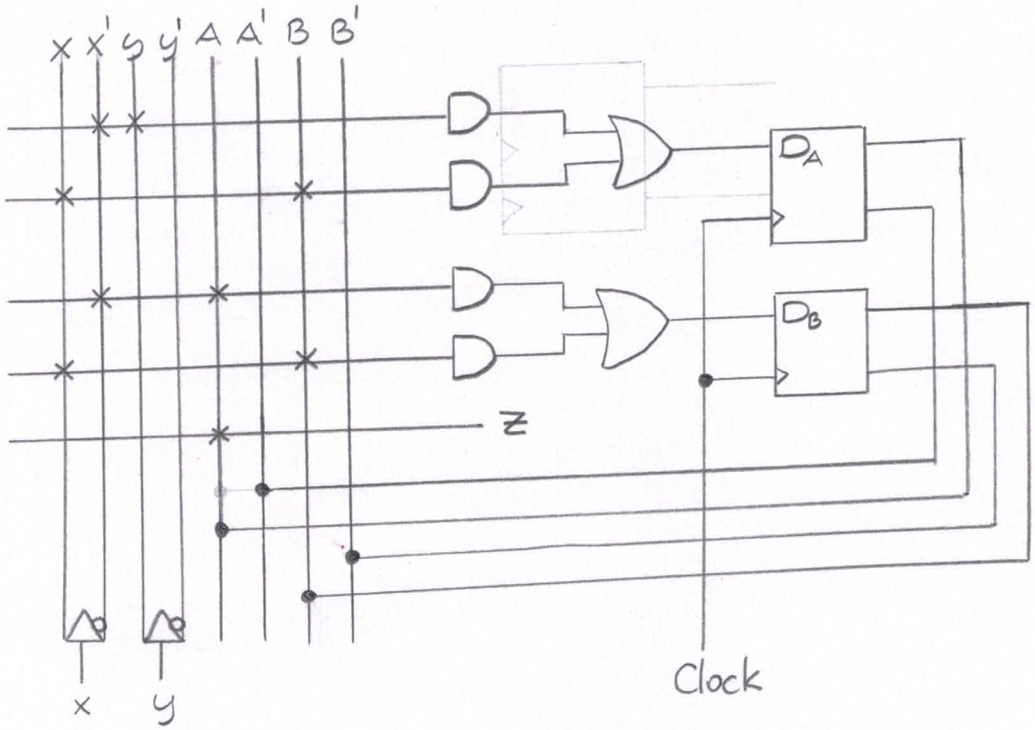
a. Draw the logic diagram of the circuit.

b. List the state table for the sequential circuit.

c. Draw the corresponding state diagram.

Solution.

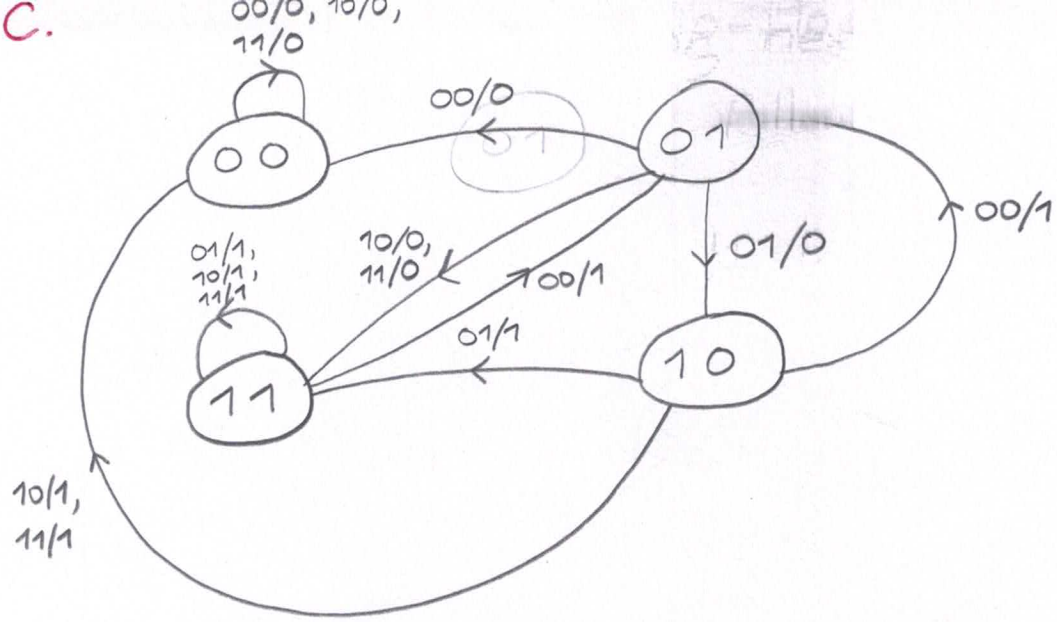
a.



b.

AB \ xy	00	01	10	11
00	00,0	10,0	00,0	00,0
01	00,0	10,0	11,0	11,0
10	01,1	11,1	00,1	00,1
11	01,1	11,1	11,1	11,1

C.


00/0, 10/0,
11/0
00/0
01
00/1
01/0
10/0,
11/0
00/1
01/1,
10/1,
11/1
01/1
00
11
10
10/1,
11/1