EEEN 222
Digital Systems Design, Spring 2018
(6 ECTS)

Instructor Information:

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Laboratory Teaching Assistants: Gökhan Gümüş, Hilmi Artun Oyman, Sami Utku Çelikok

Course description:

EEEN 222 is a one semester 6 ECTS course that meets for 3 hours of lecture and 2 hours of lab or tutorial sessions per week. This course covers the history and evolution of the computer and show how the shape of the computers we use today is a product of that evolution. Students will learn enough about Boolean logic and logical circuits to understand in principle how the processor of a modern computer works and be able to sketch the design of a simple computer.

Course objectives:

By the end of the course, students are supposed to be equipped with a balanced treatment of logic design, digital system design and computer design basics. In particular, they learn enough about Boolean logic and logical circuits to understand in principle how the processor of a modern computer works, and penetrate into the design of digital systems.

Course Learning Outcomes:

Following the successful completion of this course work, students will be able to,

1. Explain the general boolean algebra and how to use primitive logic gates for the implementation of logic circuits.
2. Identify the minterms and maxterms of a Boolean function.

3. Describe the operation of sequential circuit elements through state tables and state diagrams.
4. Use combinational logic circuits such as ROM, PLA, PAL for the purpose of storing binary information.
5. Present fuse diagrams or programming tables for the programmable logic devices.

Prerequisites: None

Text Books:

Logic and Computer Design Fundamentals,
M. Morris Mano and Charles R. Kime,
Publisher: Pearson, ISBN: 0-13-1911651

Requirements

1. Students must attend at least 70 % of the lectures, labs and tutorial sessions.
2. Students who miss a lecture or lab are completely responsible for obtaining the material they missed.
3. No make-up exams or labs will be given.
4. Excused absences must be documented and their legitimacy is determined by the instructor
5. Late assignments will be reduced 20 % of its total points for each day late, not more than 3 days
6. Adherence to the University Academic Integrity policy is expected.

Exams and Grading:

Evaluation Type	Number		Percentage
Midterm	1		30
Final Comprehensive Exam	1		50
Homeworks/ Labs	6/3		20
TOTAL			**100**

Tentative Lecture Schedule

Date	Subject
Week 1	Binary arithmetic, Arithmetic operations, Decimal codes, Alphanumeric and ASCII codes
Week 2	Boolean Logic, Logic gates, Boolean algebra, Standard forms
Week 3	Minterms, maxterms, SOP, POS forms,
Week 4	Karnaugh maps, map simplifications, digital logic gates
Week 5	Decoders, Encoders, Multiplexers, Demultiplexers
Week 6	Programmable logic devices, ROM, PLA, PAL
Week 7	Binary full and half adders, Binary ripple carry adder
Week 8	MIDTERM EXAM
Week 9	Sequential circuits, Information storage, Synchronous sequential circuit, SR and D latches
Week 10	Master-Slave flip-flops, Edge-Triggered flip-flops, Standard graphics symbols
Week 11	Characteristic tables, Sequential circuit analysis
Week 12	Input equations, State-tables
Week 13	Mealy and Moore model, State diagrams
Week 14	Sequential circuit design
Week 15	Sequential circuit examples, counters
Week 16	FINAL EXAM