Selected Problems – X

Problem 1) Design a synchronous counter that goes through the sequences

1 3 5 7 4 2 0 6 and repect

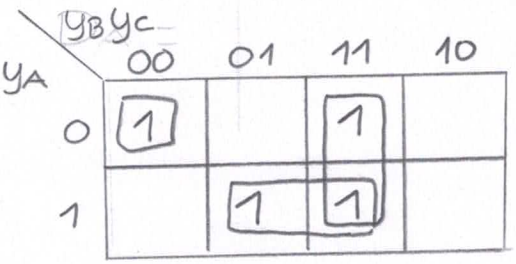
using one D, one SR, and one JK type flip-flops.

Solution. We first derive the extended state table for the counter as follows

y_A	y_B	y_C	Y_A	Y_B	Y_C	D_A	S_B	R_B	J_C	K_C
0	0	0	1	1	0	1	1	0	0	d
0	0	1	0	1	1	0	1	0	d	0
0	1	0	0	0	0	0	0	1	0	d
0	1	1	1	0	1	1	0	1	d	0
1	0	0	0	1	0	0	1	0	0	d
1	0	1	1	1	1	1	1	0	d	0
1	1	0	0	0	1	0	0	1	0	d
1	1	1	1	0	0	1	0	1	d	0

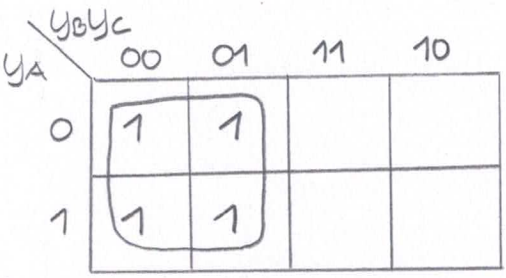
– we find that

D_A:



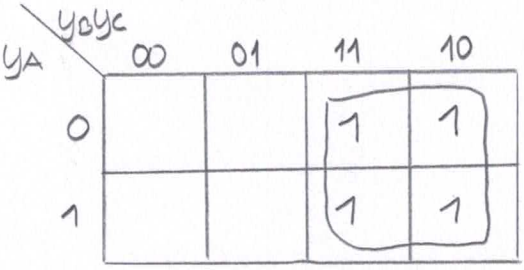
$$D_A = y_A y_C + y_B y_C + y'_A y'_B y'_C$$

S_B:



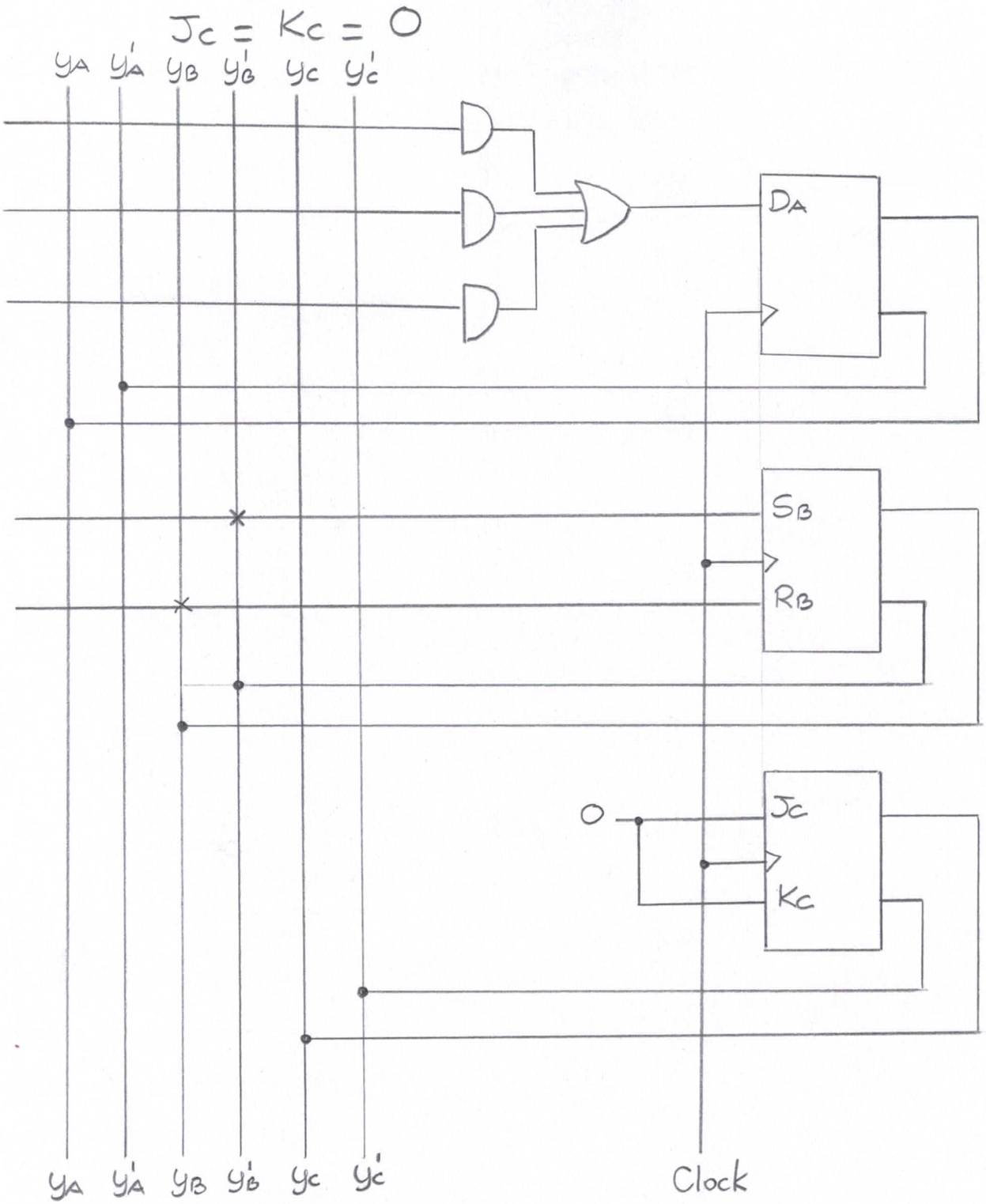
$$S_B = y'_B$$

R_B:



$$R_B = y_B$$

-and we notice that



Problem 2) Design a synchronous counter using one SR flip-flop, one T type flip-flop and one JK type flip-flop denoted by A, B, C, respectively and a single input x such that when x=0 the circuit counts from 0 to 2 to 4 to 6 and back to 0 and when x=1, it counts from 1 to 3 to 5 to 7 and back to 1.

a. Derive the state table of the sequential circuit. PS 10.2

b. Derive the state diagram of the sequential circuit.

c. Draw the logic circuit diagram for the sequential logic circuit.

Solution.

a.

x	y_A	y_B	y_C	Y_A	Y_B	Y_C	S_A	R_A	T_B	J_C	K_C
0	0	0	0	0	1	0	0	d	1	0	d
1	0	0	1	0	1	1	0	d	1	d	0
0	0	1	0	1	0	0	1	0	1	0	d
1	0	1	1	1	0	1	1	0	1	d	0
0	1	0	0	1	1	0	d	0	1	0	d
1	1	0	1	1	1	1	d	0	1	d	0
0	1	1	0	0	0	0	0	1	1	0	d
1	1	1	1	0	0	1	0	1	1	d	0

- we find that

$T_B = 1$ and $J_C = K_C = 0$

S_A:

xy_A \ y_By_C	00	01	11	10
00		d	d	1
01	d	d	d	
11	d	d		d
10	d		1	d

$S_A = y'_A y_B$

xy_A \ y_By_C	00	01	11	10
00	d	d	d	
01		d	d	1
11	d		1	d
10	d	d		d

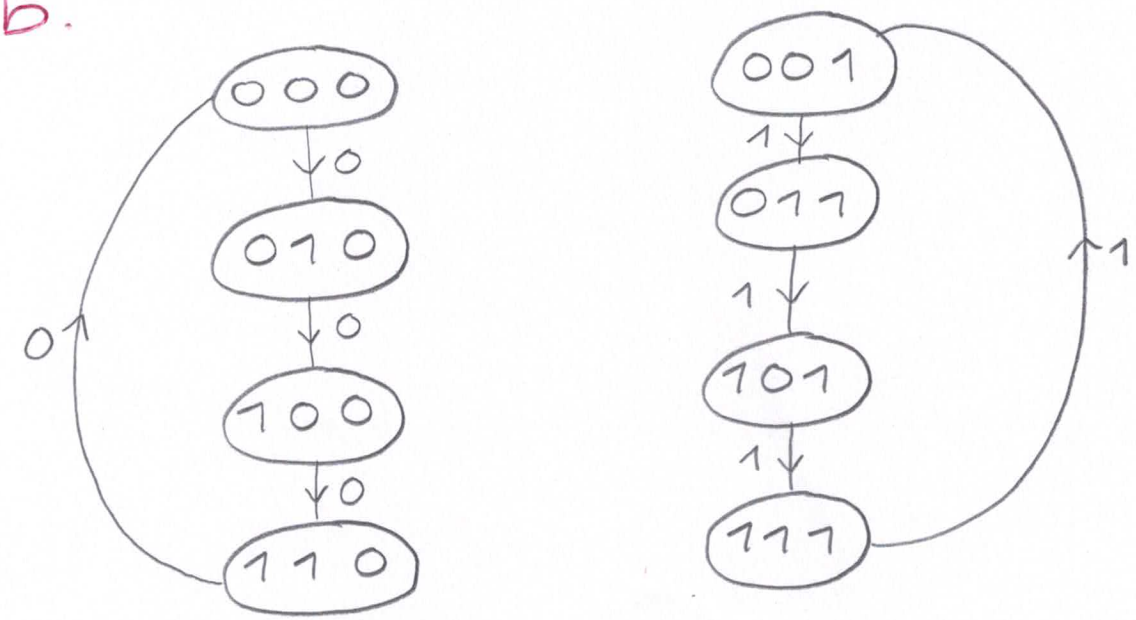
$R_A = y_A y_B$

Note that ;

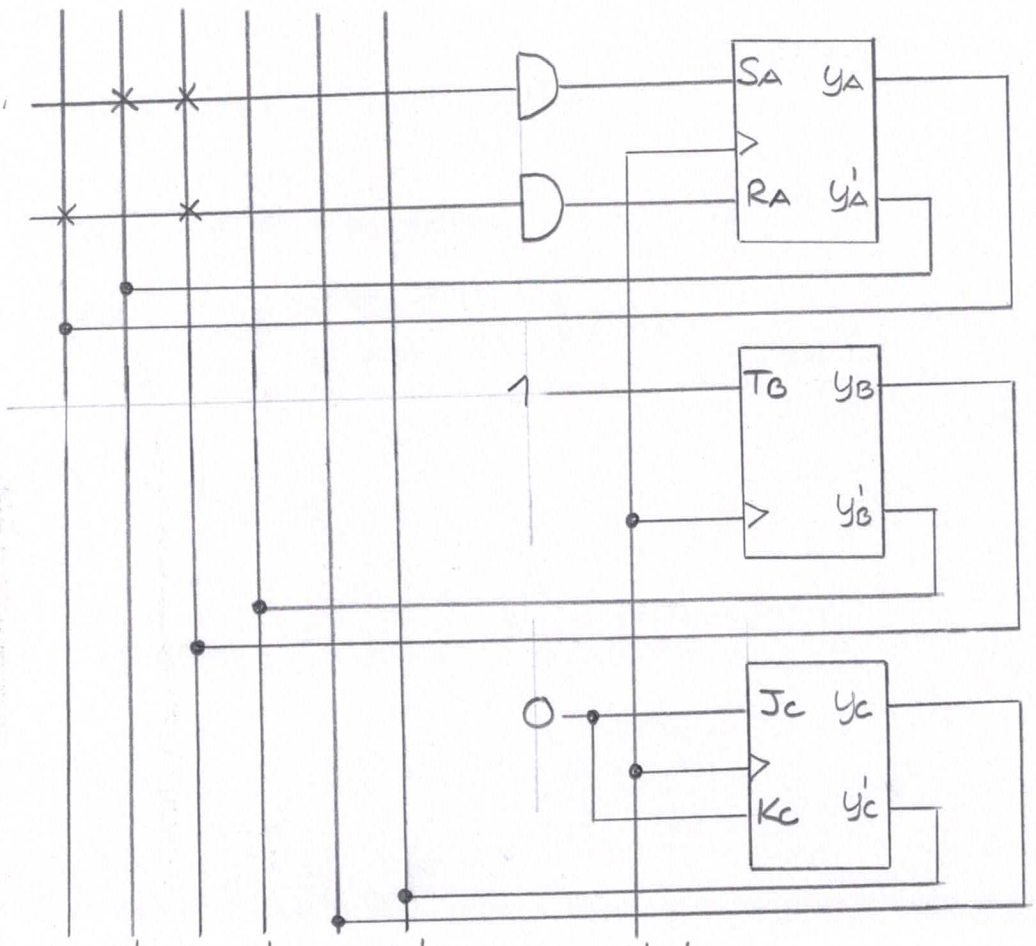
-we assumed that for $x=0$, the inputs 1, 3, 5, 7 do NOT occur and for $x=1$, the inputs 0, 2, 4, 6 do NOT occur

(( ) thus allowing to consider these situations as don't cares

b.



c.



Problem 3) Given the NEW flip-flop described by the following Karnaugh map

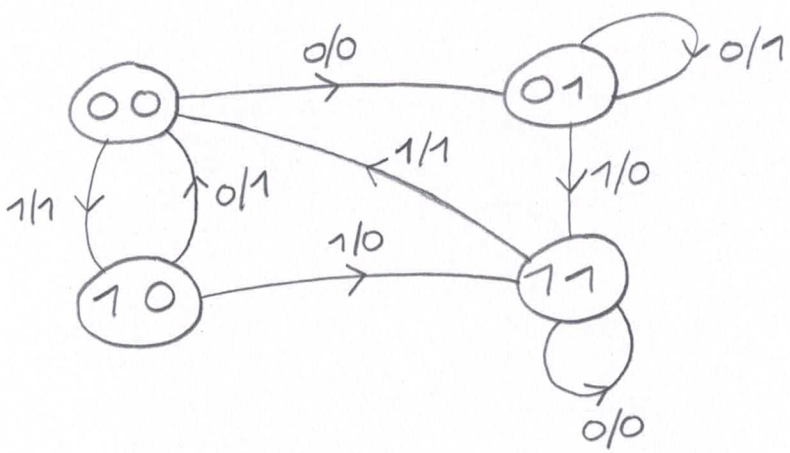
Q(t) \ xy	00	01	11	10
0	1	1		
1		1	1	

Q(t+1)

where x and y are flip-flop inputs, Q(t) is the present state and Q(t+1) is the next state.

a. Find the excitation table of the NEW flip-flop.

b. Using this NEW flip-flop, realize the sequential circuit with the state diagram shown as



Solution.

a. The excitation table is obtained as follows

Q(t) Q(t+1)	00	01	11	10
	1, d	0, d	d, 1	d, 0

b. We tabulate the state table as follows:

E	A	B	A(t+1)	B(t+1)	x_A	y_A	x_B	y_B	z
0	0	0	0	1	1	d	0	d	0
1	0	0	1	0	0	d	1	d	1
0	0	1	0	1	1	d	d	1	1
1	0	1	1	1	0	d	d	1	0
0	1	0	0	0	d	0	1	d	1
1	1	0	1	1	d	1	0	d	0
0	1	1	1	1	d	1	d	1	0
1	1	1	0	0	d	0	d	0	1

X_A :

E \ AB	00	01	11	10
0	1	1	d	d
1	·	·	d	d

$X_A = E'$

y_A :

E \ AB	00	01	11	10
0	d	d	1	·
1	d	d	·	1

$y_A = E'B + EB'$

$= E \oplus B$

X_B :

E \ AB	00	01	11	10
0	·	d	d	1
1	1	d	d	·

$X_B = E'A + EA'$

$= E \oplus A$

y_B :

E \ AB	00	01	11	10
0	d	1	1	d
1	d	1	·	d

$y_B = E' + A'$

Z :

E \ AB	00	01	11	10
0		1		1
1	1	1	1	

$Z = EA'B' + E'A'B + EAB + E'AB'$