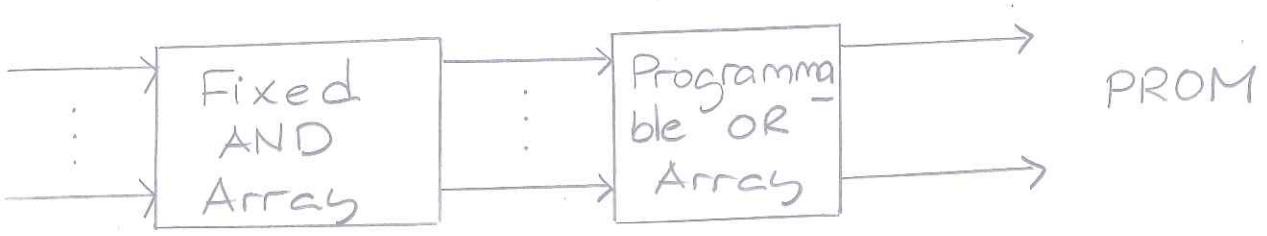
Programmable Logic Devices (PLD)

- Programmable logic devices are AND-OR logic circuits
  - ↳ which can be programmed by the user
- we consider three main types of PLDs:
  1. Read Only Memory (ROM)
  2. Programmable Logic Array (PLA)
  3. Programmable Array Logic (PAL)

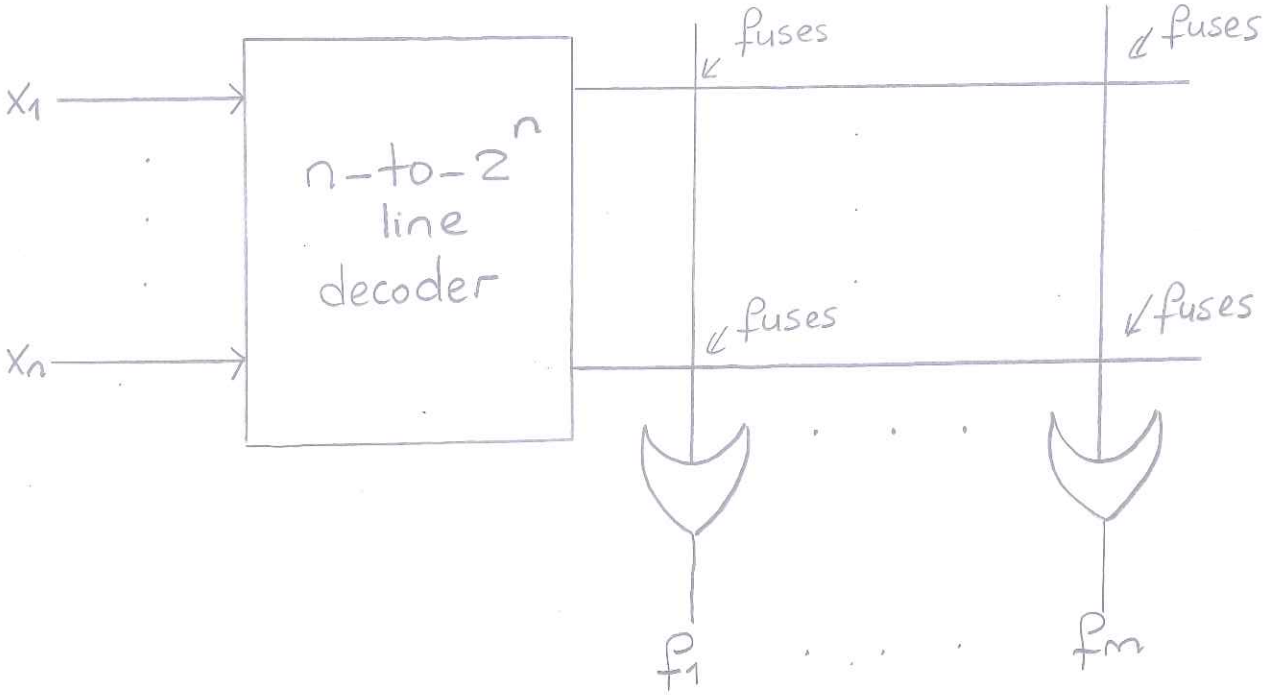
Read Only Memory (ROM)

- there exist various types of ROMs such as
  - PROM (Programmable ROM)
  - EPROM (Electrically PROM)
  - EEPROM (Electrically Erasable PROM)
- the general structure is given as follows

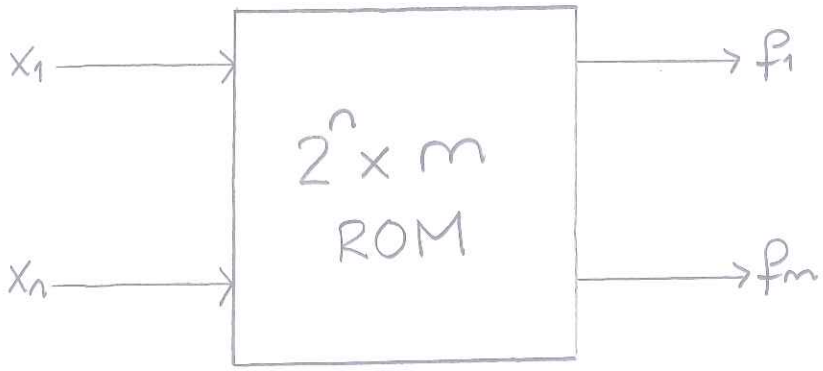


- the ROM circuit is a combinational circuit
  - ↳ that implements m Boolean functions of n variables in sum of minterms form

- the circuit is composed of an n-input decoder and m OR gates



- and equivalently represented as follows



Note that ;

- if the input sequence is $(x_1 \cdots x_n)$, then the binary information of m bits, namely, $(f_1 \cdots f_m)$ is stored at address $(x_1 \cdots x_n)$

↳ justifying why it is referred as "Read Only Memory"

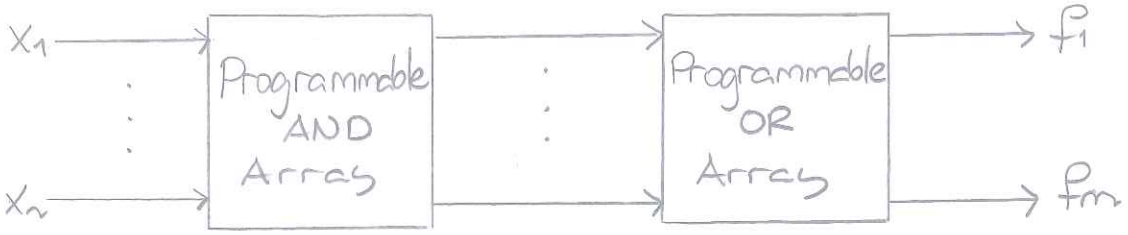
However;

- keep in mind that this is a combinational logic circuit

  ↳ thus every combinational logic circuit can be interpreted as a ROM circuit

Programmable Logic Array (PLA)

- the general structure can be given by



- a typical PLA circuit involves 16 inputs, 48 AND gates, and 8 outputs

Note that;

- a PROM with 16 inputs has 2^{16} AND gates

  ↳ while PLA has only 48 AND gates

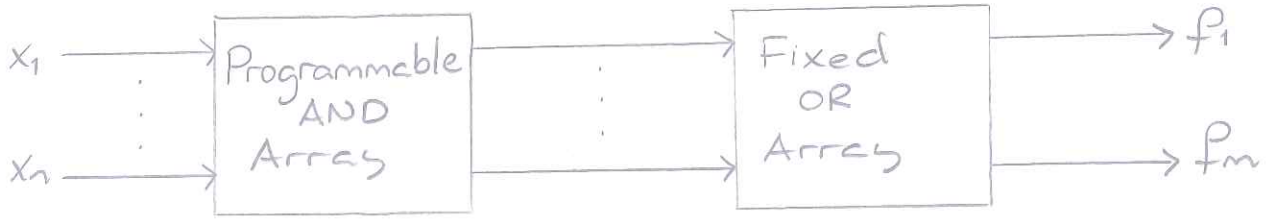
Hence;

- a PROM with 16 inputs and 8 outputs is capable of storing 2^{16} times 8 bits of binary information
- so does a PLA of the same size

  ↳ but with significantly less number of AND gates.

Programmable Array Logic (PAL)

- the general structure can be shown as



- since only the AND gates are programmable
  - ↳ it is not as flexible as PLA

Note that;

- ROM, PLA and PAL devices can be mask programmable or field programmable

mask programming

- the customer provides a program table to the manufacturer
  - ↳ which is used by the vendor to produce a custom-made PLD that has the internal logic specified by the customer

field programming

- it uses a field-programmable logic array
  - ↳ which can be programmed by the user with a commercial hardware programming unit

Boolean functions and PLDs

- multiple number of Boolean functions can be implemented using ROM, PLA, or PAL
- simply because PLDs generate either entire minterms or several product terms
  - (1) which are ORed and obtained as outputs
- we need to handle each PLD in a different way

Namely,

ROM: All minterms are available. form
Obtain the sum of minterms for each Boolean function.

PLA: AND terms are in limited number.
Minimize the Boolean functions such that common product terms are obtained

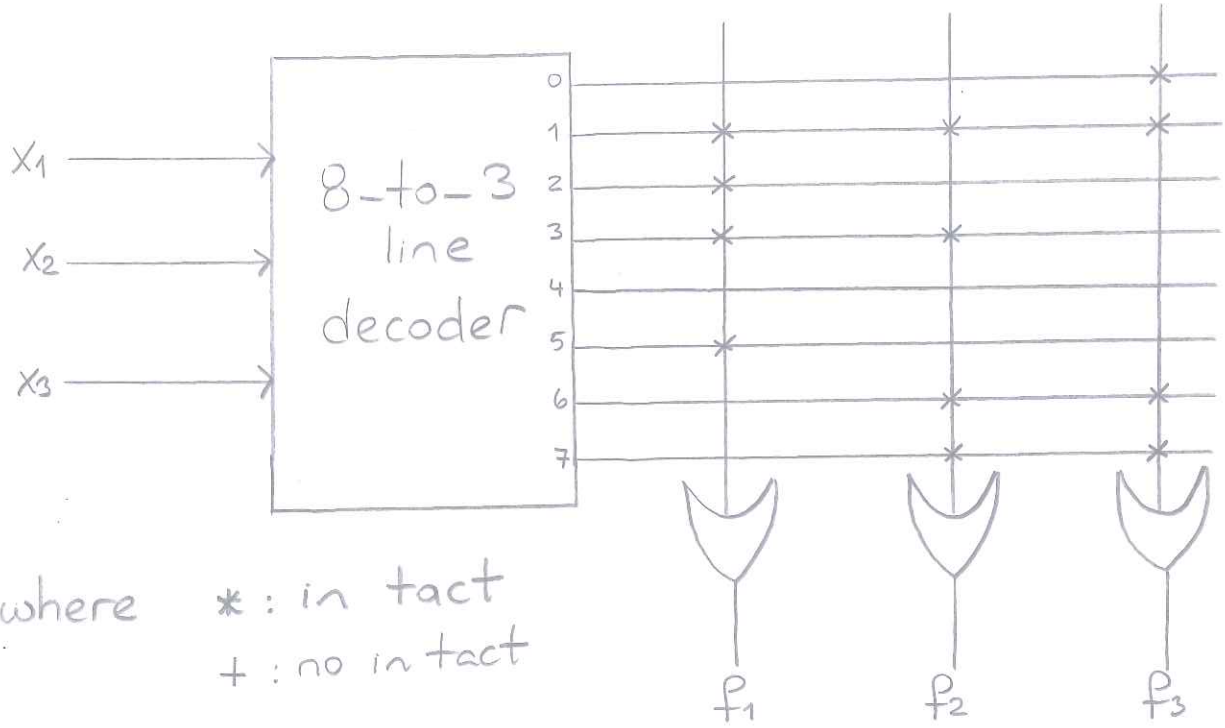
PAL: Minimize the Boolean functions individually such that each function is implemented with at most a certain number of AND gates

example. Consider the following Boolean functions

$$f_1(x_1, x_2, x_3) = \Sigma m(1,2,3,5)$$
$$f_2(x_1, x_2, x_3) = \Sigma m(1,3,6,7)$$
$$f_3(x_1, x_2, x_3) = \Sigma m(0,1,6,7)$$

Implement f_1, f_2, f_3 using an appropriate size ROM.

- we need to employ an 8 × 3 ROM



where * : in tact
+ : no in tact

- we find that at the following addresses,

x_1	x_2	x_3	f_1	f_2	f_3
0	1	1	1	1	0
1	0	1	1	0	0
1	1	0	0	1	1

addresses — information stored

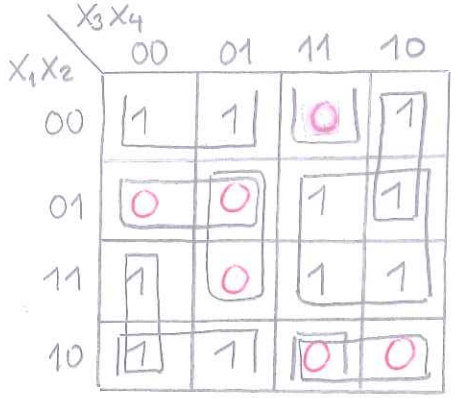
the corresponding 3 bits of data are stored

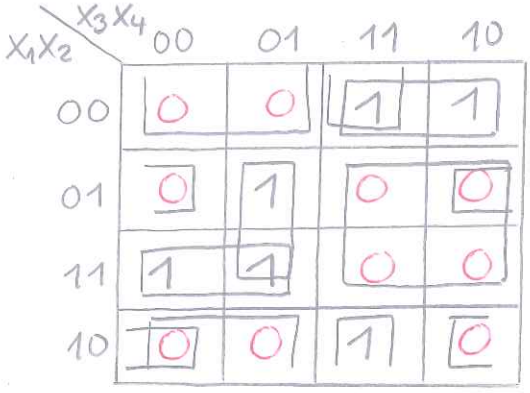
example. Consider the following Boolean functions

$$f_1(x_1, x_2, x_3, x_4) = \Sigma m(0, 1, 2, 6, 7, 8, 9, 12, 14, 15)$$

$$f_2(x_1, x_2, x_3, x_4) = \Sigma m(2, 3, 5, 11, 12, 13)$$

- we minimize both $\{f_1, f_1'\}$ and $\{f_2, f_2'\}$





$$f_1 = x_2x_3 + x_2'x_3' + x_1'x_3x_4' + x_1x_3'x_4'$$

$$f_2 = x_1'x_2'x_3 + x_2'x_3x_4 + x_1x_2x_3' + x_2x_3'x_4$$

$$f_1' = x_1'x_2x_3' + x_2x_3'x_4 + x_2'x_3x_4 + x_1x_2'x_3$$

$$f_2' = x_2'x_3' + x_2x_3 + x_1'x_2x_4' + x_1x_2'x_4'$$

- we can see that f_1 and f_2' have the greatest number of common terms
- the PLA implementation table is given by

Product terms	x_1	x_2	x_3	x_4	f_1	f_2'
1	–	1	1	–	1	1
2	–	0	0	–	1	1
3	0	–	1	0	1	–
4	1	–	0	0	1	–
5	0	1	–	0	–	1
6	1	0	–	0	–	1

- then the PLA has 4 inputs, 6 AND gates, and 2 outputs