**Problem 1)** Design a combinational circuit with three inputs x, y, and z, and three outputs A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is three less than the input.

a. Derive the truth table of the circuit.

b. Minimize the output Boolean functions.

c. Implement the circuit using an appropriate size decoder and external OR gates.

**Solution.**

a.

| x | y | z | A | B | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

b.

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | 1 | 1 |
| 1 | | | 1 | |

$A = x'y + yz$

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 1 | | |
| 1 | | 1 | | 1 |

$B = x'y' + y'z + xyz'$

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | 1 | 1 | |
| 1 | 1 | | | 1 |

$C = x'z + xz'$

c. We have

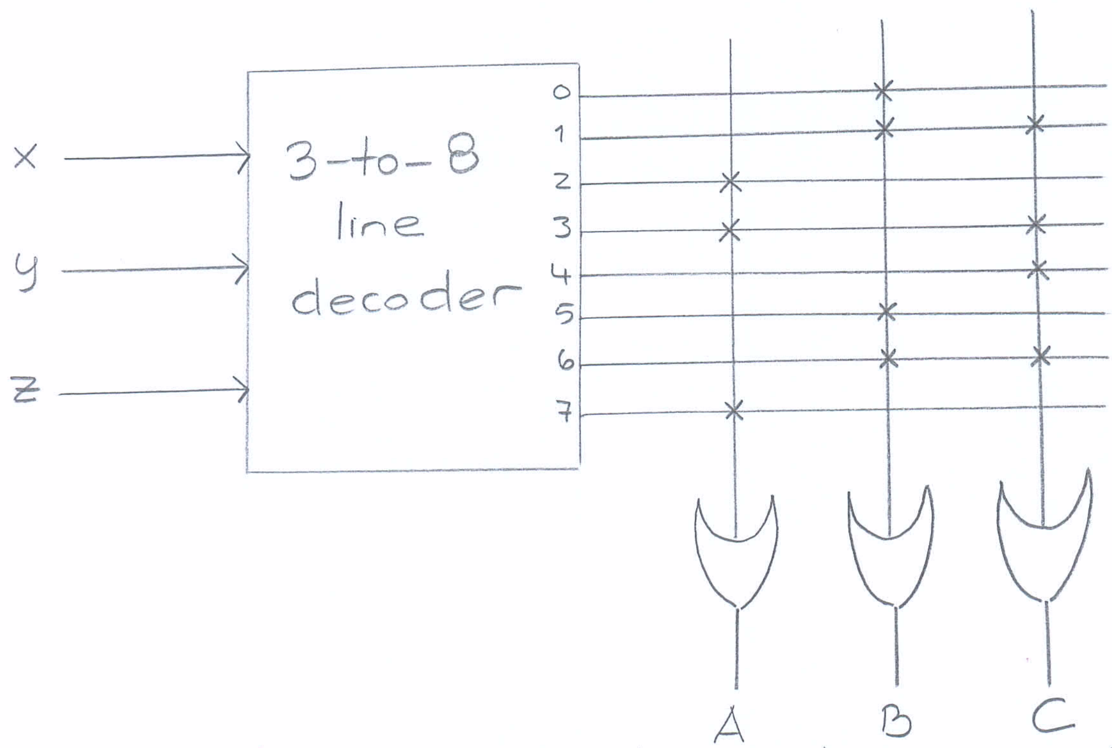
$$A(x,y,z) = \Sigma m(2,3,7)$$

$$B(x,y,z) = \Sigma m(0,1,5,6)$$

$$C(x,y,z) = \Sigma m(1,3,4,6)$$

- we have 3 inputs and 3 outputs

↳ thus, a 3-to-8 line decoder is needed




Problem 2) Draw the logic diagram of a 2-to-4 line decoder using :

a. AND gates only,

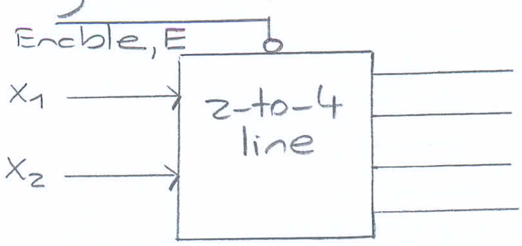
b. NAND gates only,

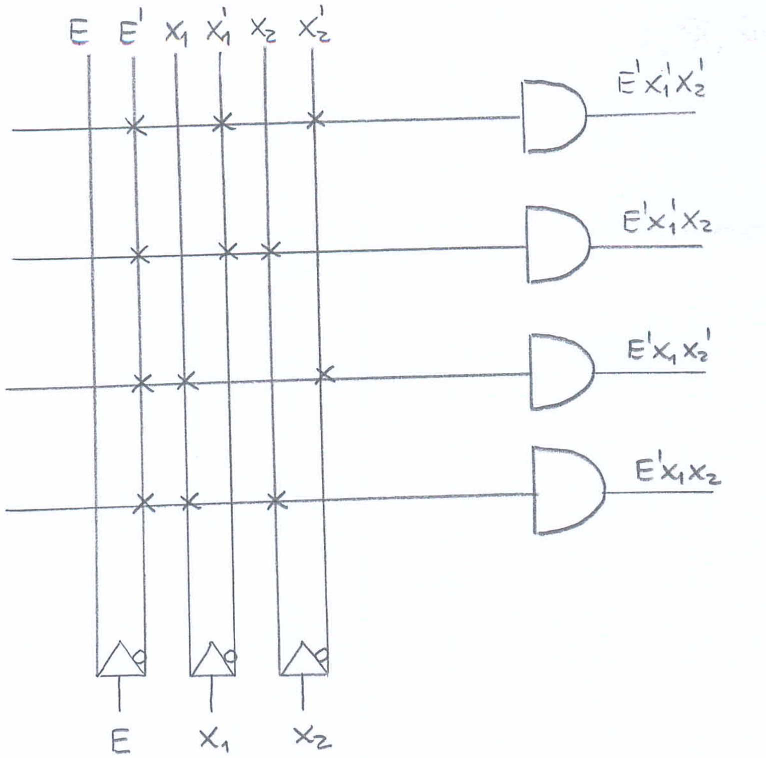
c. NOR gates only.

Include also an enable input.

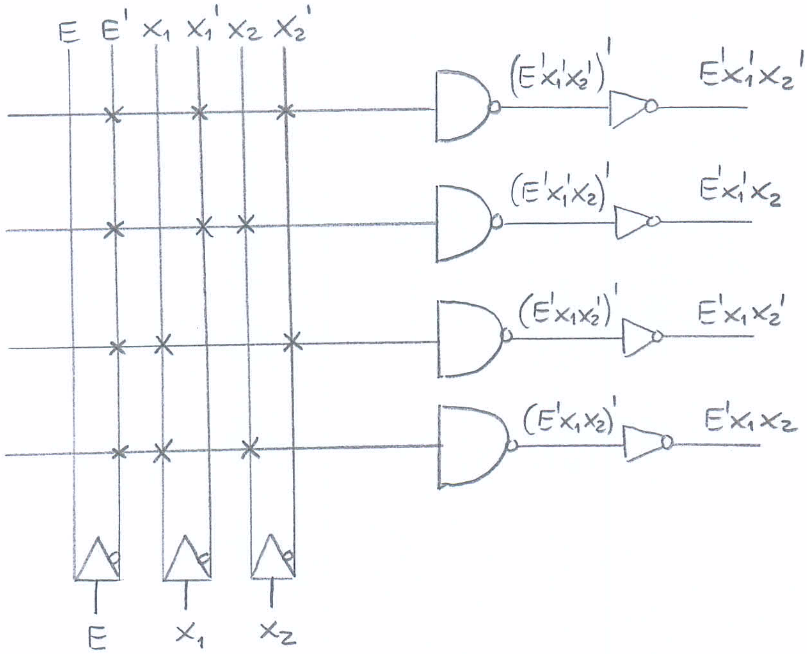
Solution.

a. The block diagram of a 2-to-4 line decoder with enable input:

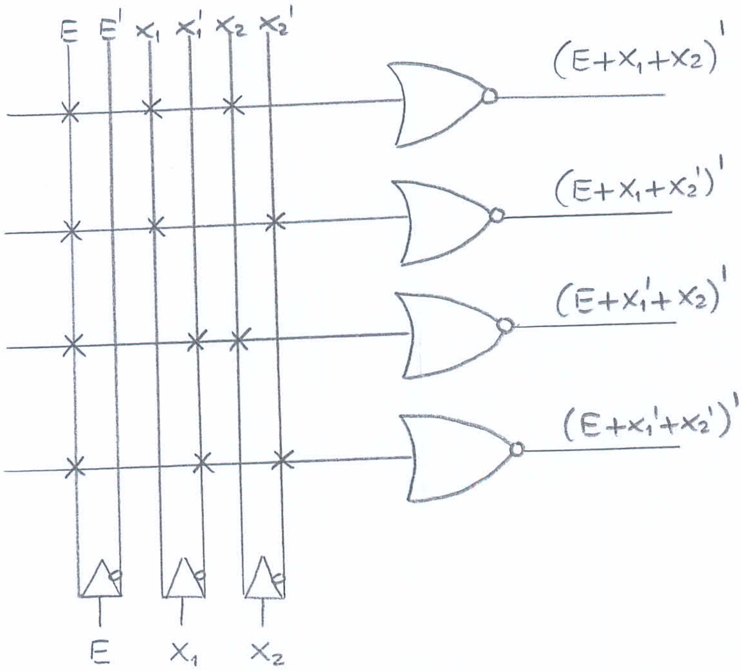



E E' X1 X1' X2 X2'
E'X1'X2'
E'X1'X2
E'X1X2'
E'X1X2
E X1 X2

b.


E E' X1 X1' X2 X2'
(E'X1'X2')'
E'X1'X2'
(E'X1'X2)'
E'X1'X2
(E'X1X2')'
E'X1X2'
(E'X1X2)'
E'X1X2
E X1 X2

c.


E E' X1 X1' X2 X2'
(E+X1+X2)'
(E+X1+X2')'
(E+X1'+X2)'
(E+X1'+X2')'
E X1 X2

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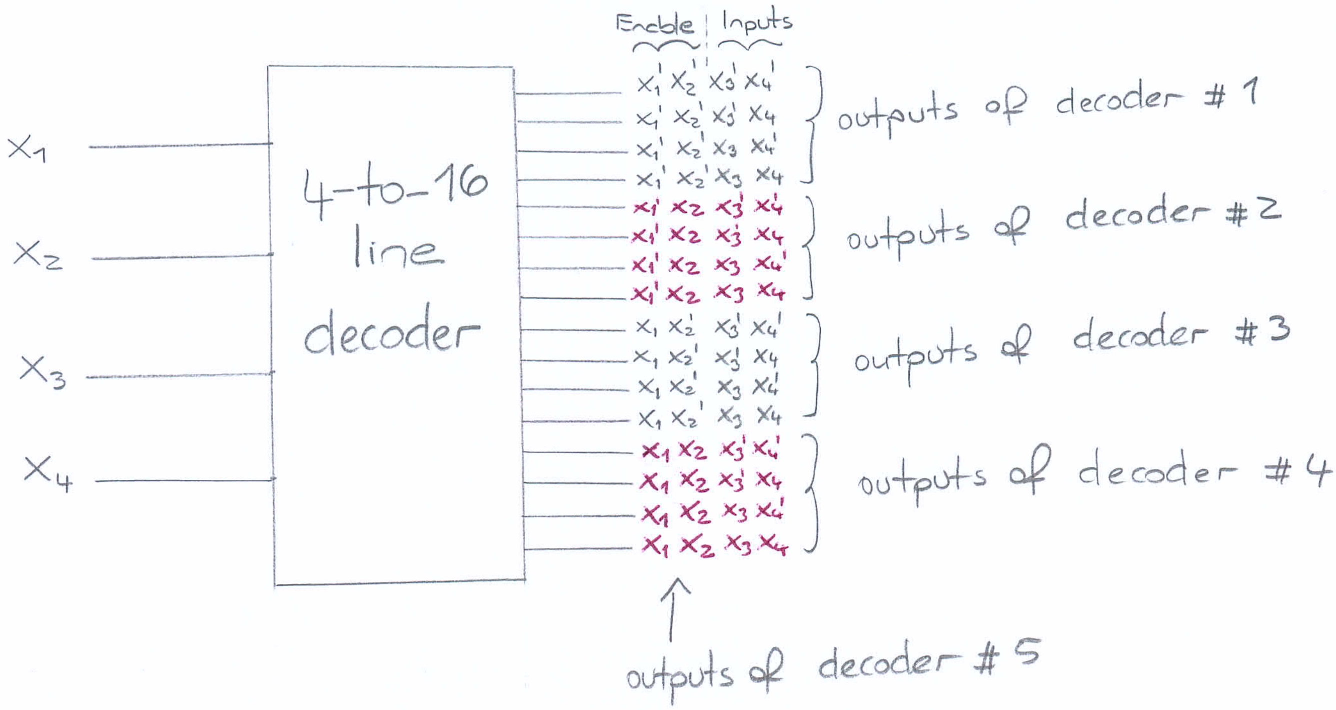
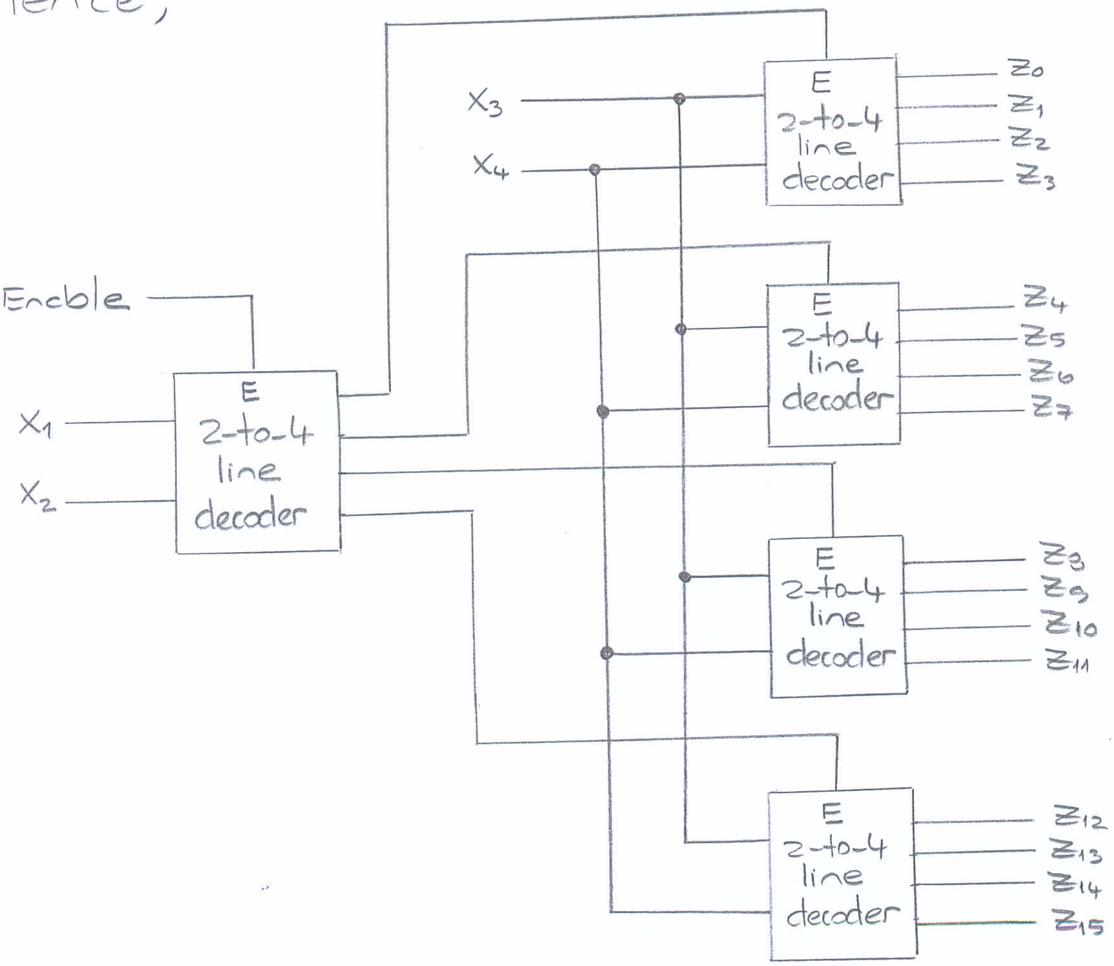
Problem 3) Construct a 4-to-16 line decoder with five 2-to-4 line decoders with enable. Use block diagram for the components.

Solution. We have




Hence;



**Problem 4)** Implement the following Boolean functions using the indicated multiplexers.

a. $F(A,B,C,D) = \sum m(0,2,5,7,11,14)$ with a 8-to-1 line multiplexer and external gates if necessary.

b. $G(A,B,C,D) = \prod M(3,8,12)$ with a 4-to-1 line multiplexer and external gates if necessary.

**Solution.**

a.

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | | | 1 |
| 01 | | 1 | 1 | |
| 11 | | | | 1 |
| 10 | | | 1 | |

$$F = A'B'D' + A'BD + ABCD' + AB'CD$$

- we shall select A, B, D as control inputs of the 3-to-8 line decoder

That is ;

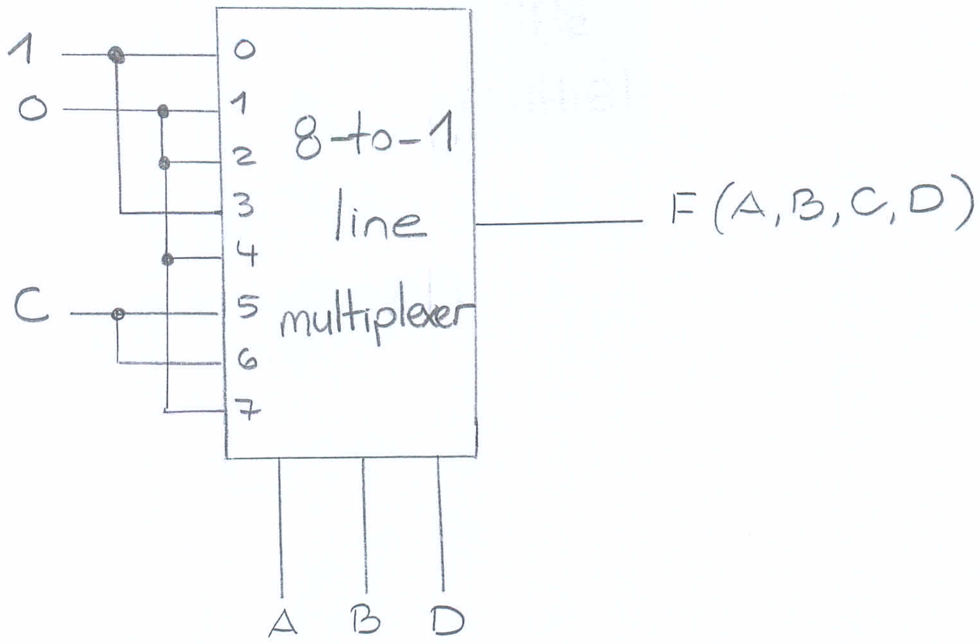
$$F = (A'B'D')\cdot 1 + (A'BD)\cdot 1 + (ABD')\cdot C + (AB'D)\cdot C$$

$$= m_0 \cdot 1 + m_3 \cdot 1 + m_6 \cdot C + m_5 \cdot C$$

$$+ m_1 \cdot 0 + m_2 \cdot 0 + m_4 \cdot 0 + m_7 \cdot 0$$

$$= \sum_{i=0}^{7} m_i I_i$$

where $I_0 = I_3 = 1$, $I_1 = I_2 = I_4 = I_7 = 0$ and $I_5 = I_6 = C$




b.

$$G(A,B,C,D) = \Sigma m(0,1,2,4,5,6,7,9,10,11,13,14,15)$$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | | 1 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | | 1 | 1 | 1 |
| 10 | | 1 | 1 | 1 |

$$G = C'D + CD' + A'C'D' + BCD + ACD$$

Note that;

- as we shall choose C and D as the control inputs of the 4-to-1 line multiplexer

↳ in the Karnaugh map, our concern is NOT to consider the largest groupings always but keep track of the group of 1's involving C and D in its product expression

- That is why we take groups of two 1's in the K-map

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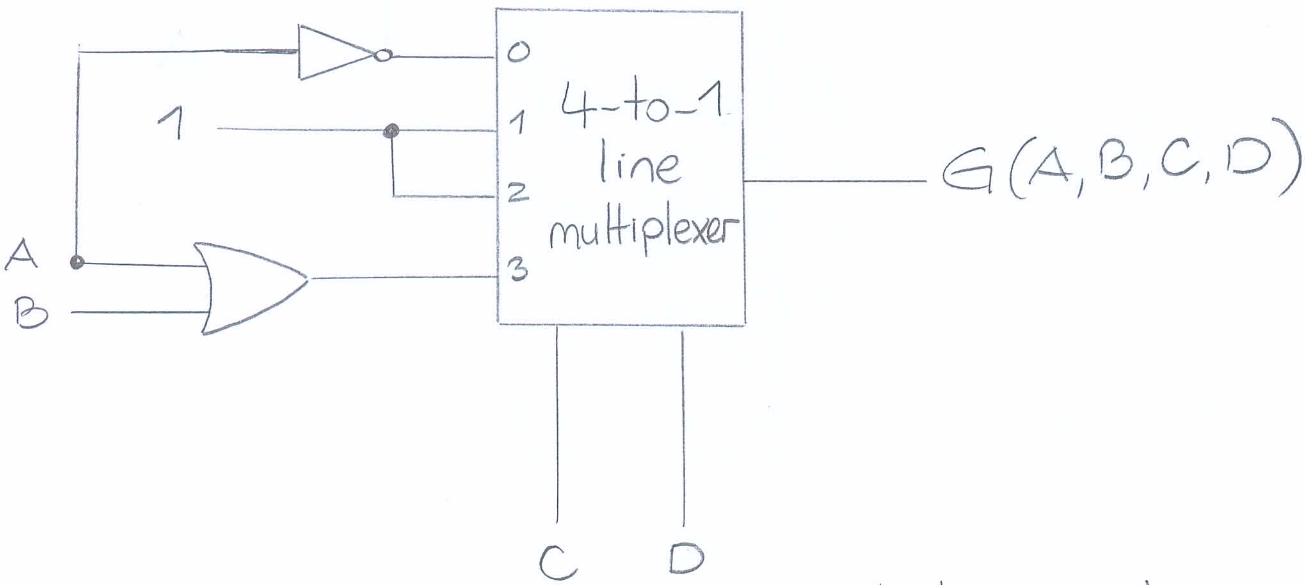
Hence;

$$G = (C'D')A' + (C'D)\cdot 1 + (CD')\cdot 1 + (CD)(A+B)$$

$$= m_0 \cdot A' + m_1 \cdot 1 + m_2 \cdot 1 + m_3 \cdot (A+B)$$

$$= \sum_{i=0}^{3} m_i I_i$$

where $I_0 = A'$ , $I_1 = I_2 = 1$ , $I_3 = A + B$




Problem 5) An $8\times 1$ multiplexer has inputs A, B, and C connected to the selection inputs. The data inputs $I_0$ through $I_7$ are as follows:

$$I_1 = I_2 = 0 , \quad I_3 = I_7 = 1 , \quad I_4 = I_5 = D ,$$

and

$$I_0 = I_6 = D'$$

Determine the Boolean function that the multiplexer implements.

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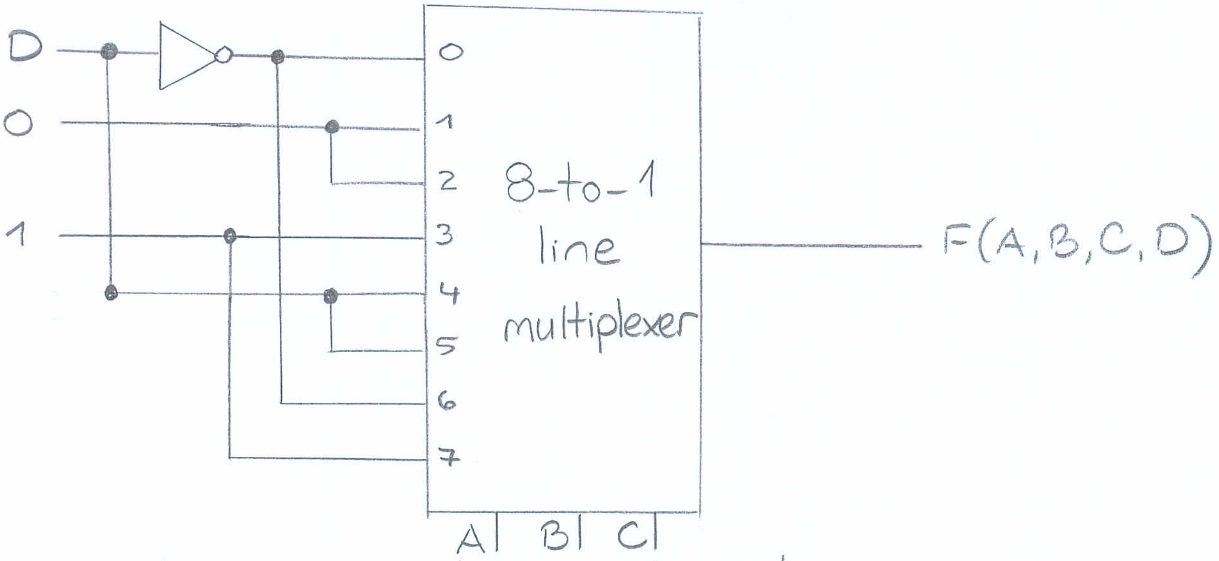
**Solution.** We shall draw the circuit diagram:




– as the circuit is already given, we shall obtain the Boolean function

(i) by using the output description of the multiplexer

$$F(A,B,C,D) = \sum_{i=0}^{7} m_i I_i$$

$$= m_0 \cdot D' + m_1 \cdot 0 + m_2 \cdot 0 + m_3 \cdot 1$$
$$+ m_4 \cdot D + m_5 \cdot D + m_6 \cdot D' + m_7 \cdot 1$$

$$= (A'B'C') \cdot D' + (A'BC) \cdot 1 + (AB'C') \cdot D$$
$$+ (AB'C) \cdot D + (ABC') \cdot D' + (ABC) \cdot 1$$

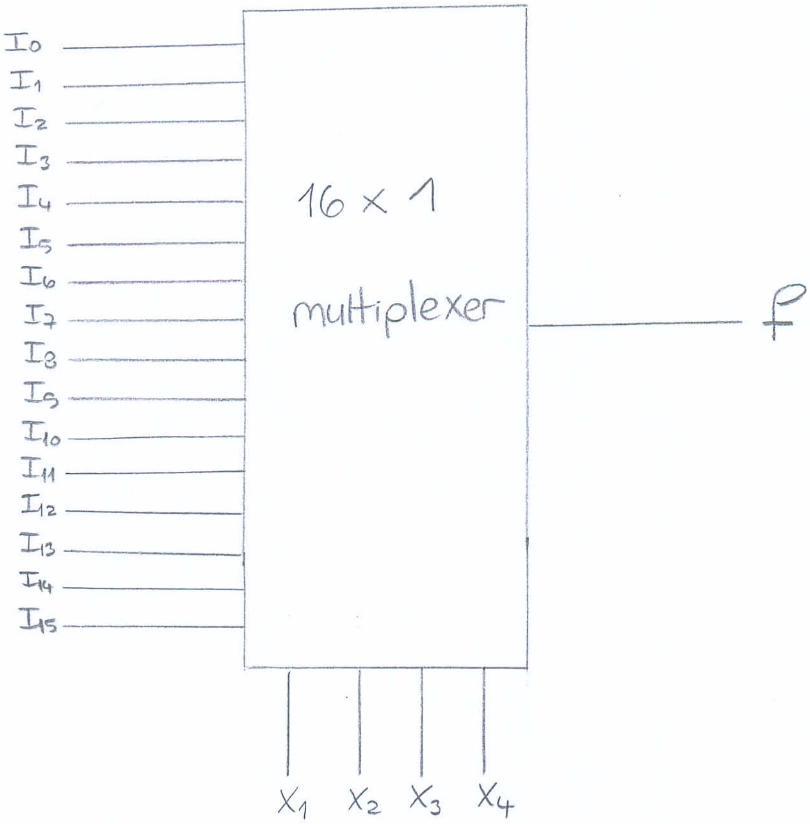
| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | | | |
| 01 | | | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | | 1 | 1 | |

Hence;

$$F(A,B,C,D) = \sum m(0,6,7,9,11,12,13,14,15)$$

Problem 6) Construct a 16 x 1 multiplexer with two 8x1 multiplexers and one 2x1 multiplexer. Use block diagrams.

Solution. We wish to obtain




- we have

$$f(x_1,x_2,x_3,x_4) = \sum_{i=0}^{15} m_i I_i$$

$$\begin{aligned}
&= x_1'x_2'x_3'x_4' I_0 + x_1'x_2'x_3'x_4 I_1 + x_1'x_2'x_3x_4' I_2 + x_1'x_2'x_3x_4 I_3 \\
&+ x_1'x_2x_3'x_4' I_4 + x_1'x_2x_3'x_4 I_5 + x_1'x_2x_3x_4' I_6 + x_1'x_2x_3x_4 I_7 \\
&+ x_1x_2'x_3'x_4' I_8 + x_1x_2'x_3'x_4 I_9 + x_1x_2'x_3x_4' I_{10} + x_1x_2'x_3x_4 I_{11} \\
&+ x_1x_2x_3'x_4' I_{12} + x_1x_2x_3'x_4 I_{13} + x_1x_2x_3x_4' I_{14} + x_1x_2x_3x_4 I_{15}
\end{aligned}$$

$$\begin{aligned}
= x_1' \Big( &x_2'x_3'x_4' I_0 + x_2'x_3'x_4 I_1 + x_2'x_3x_4' I_2 + x_2'x_3x_4 I_3 \\
&+ x_2x_3'x_4' I_4 + x_2x_3'x_4 I_5 + x_2x_3x_4' I_6 + x_2x_3x_4 I_7 \Big) \\
+ x_1 \Big( &x_2'x_3'x_4' I_8 + x_2'x_3'x_4 I_9 + x_2'x_3x_4' I_{10} + x_2'x_3x_4 I_{11} \\
&+ x_2x_3'x_4' I_{12} + x_2x_3'x_4 I_{13} + x_2x_3x_4' I_{14} + x_2x_3x_4 I_{15} \Big)
\end{aligned}$$

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$$= x_1' (m_0 I_0 + m_1 I_1 + m_2 I_2 + m_3 I_3 + m_4 I_4 + m_5 I_5 + m_6 I_6 + m_7 I_7)$$

$$+ x_1 (m_0 I_8 + m_1 I_9 + m_2 I_{10} + m_3 I_{11} + m_4 I_{12} + m_5 I_{13} + m_6 I_{14} + m_7 I_{15})$$

where $m_i$, $i = 0, 1, \ldots, 7$ are minterms wrt the variables $x_2, x_3, x_4$

Moreover;

$$f(x_1, x_2, x_3, x_4) = x_1' \sum_{i=0}^{7} m_i I_i + x_1 \sum_{i=0}^{7} m_i I_{i+8}$$

$$= \hat{m}_0 \underbrace{\left( \sum_{i=0}^{7} m_i I_i \right)}_{\text{generated by an } 8\times 1 \text{ multiplexer}} + \hat{m}_1 \underbrace{\left( \sum_{i=0}^{7} m_i I_{i+8} \right)}_{\text{generated by an } 8\times 1 \text{ multiplexer}}$$

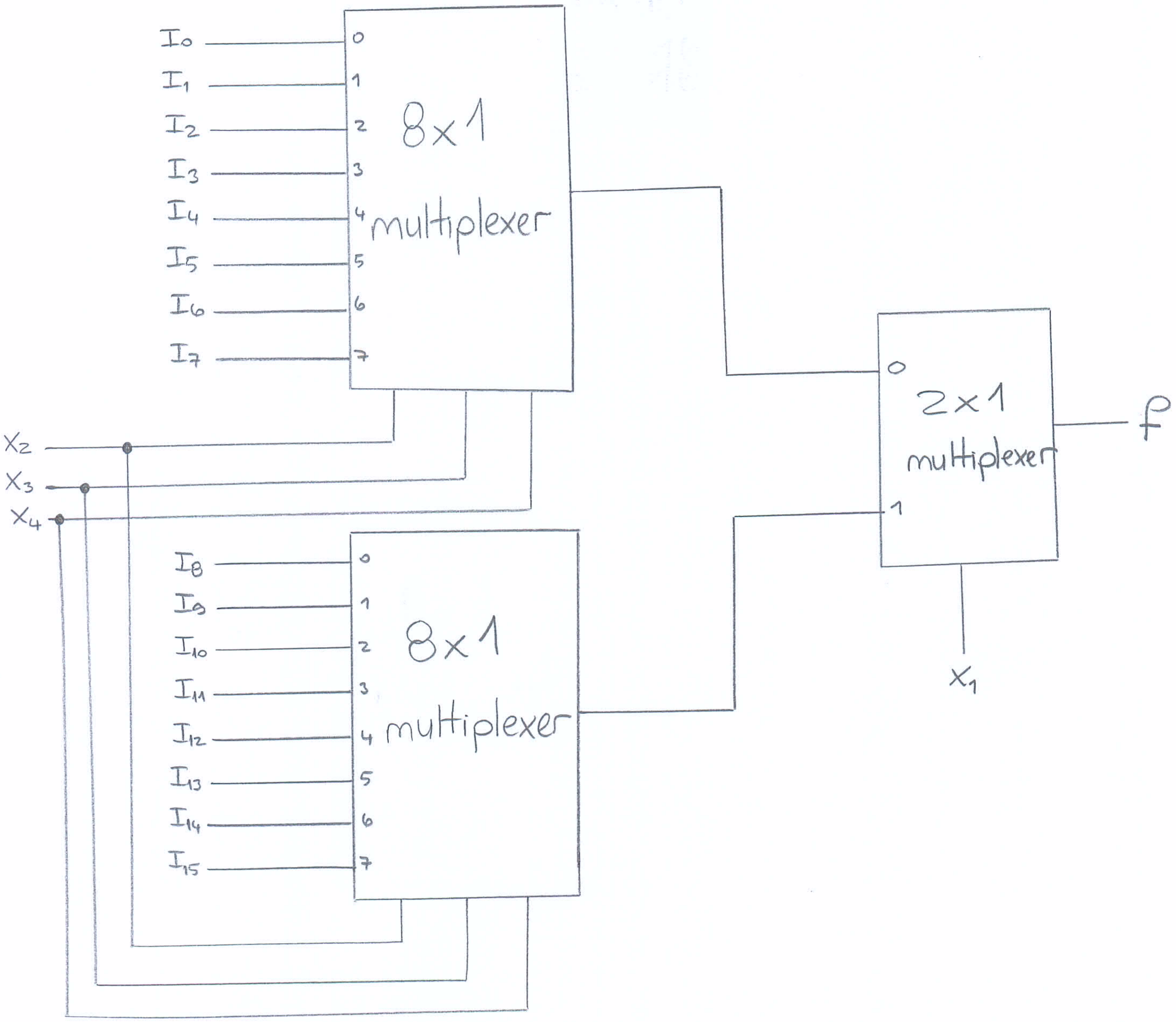
$$= \hat{m}_0 \hat{I}_0 + \hat{m}_1 \hat{I}_1$$

where $\hat{m}_0$, $\hat{m}_1$ are the minterms wrt the variable $x_1$ and

$$\hat{I}_0 = \sum_{i=0}^{7} m_i I_i \quad , \quad \hat{I}_1 = \sum_{i=0}^{7} m_i I_{i+8}$$

As a result;

$$f(x_1, x_2, x_3, x_4) = \underbrace{\sum_{j=0}^{1} \hat{m}_j \hat{I}_j}_{\text{generated by a } 2\times 1 \text{ multiplexer}}$$


I0
I1
I2
I3
I4
I5
I6
I7
0
1
2
3
4
5
6
7
8x1
multiplexer
X2
X3
X4
I8
I9
I10
I11
I12
I13
I14
I15
0
1
2
3
4
5
6
7
8x1
multiplexer
0
1
2x1
multiplexer
f
X1