Problem 1) Using half adders and/or full adders

a. Design a four-bit combinational circuit incrementer (a circuit that adds 1 to a four-bit binary number)

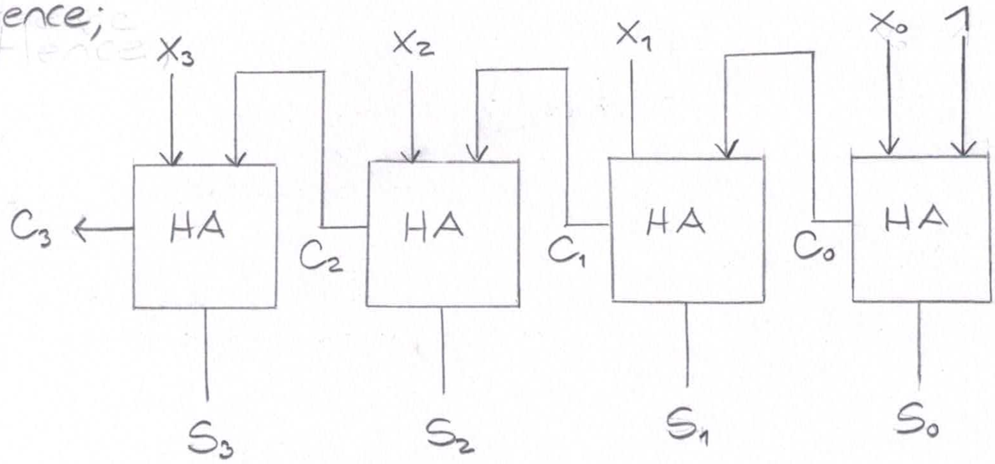
b. Design a four-bit combinational circuit decrementer (a circuit that subtracts 1 from a four-bit binary number)

Solution.

a. We consider

$$\begin{array}{cccccc} & & X_3 & X_2 & X_1 & X_0 \\ & + & 0 & 0 & 0 & 1 \\ \hline C_3 & & S_3 & S_2 & S_1 & S_0 \end{array}$$

Hence;



b. We consider

$$\begin{array}{ccccc} & X_3 & X_2 & X_1 & X_0 \\ - & 0 & 0 & 0 & 1 \\ \hline \end{array}$$

- now employing the technique of 2's complement, we shall redefine subtraction as follows

$$\begin{array}{cl} & X_3 \quad X_2 \quad X_1 \quad X_0 \\ + & \text{2's complement of } (0001) \\ \hline \end{array}$$

- and we calculate

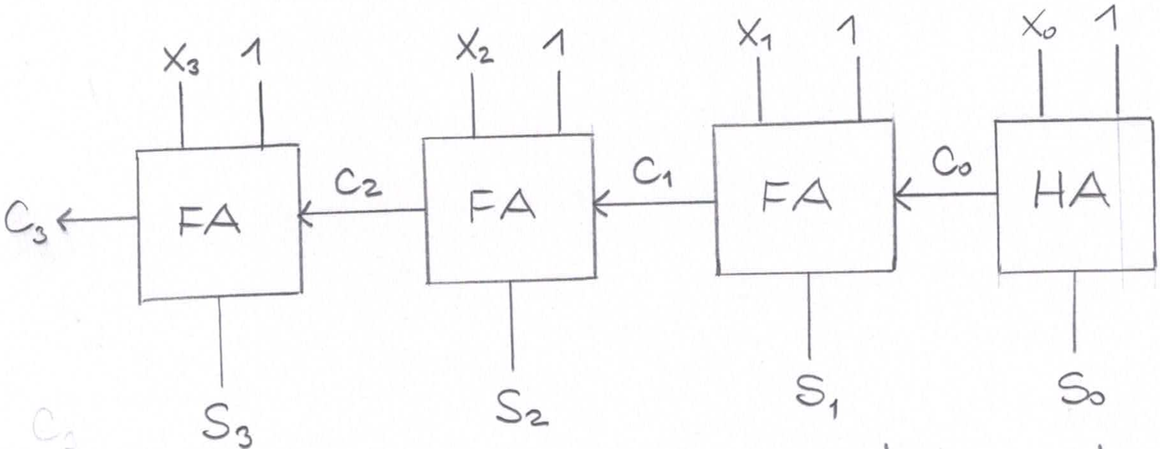
2's complement of 0001 = 1's complement of 0001 + 0001

= 1110 + 0001

= 1111

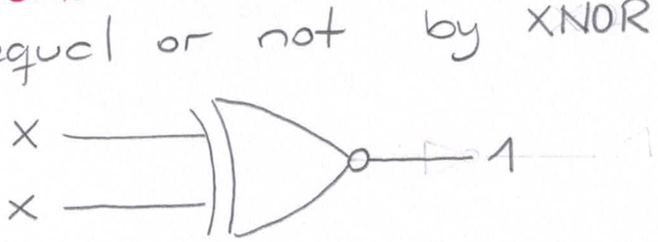
Therefore;

$$\begin{array}{cccc} X_3 & X_2 & X_1 & X_0 \\ 0 & 0 & 0 & 1 \\ \hline \end{array} \; - \quad \equiv \quad \begin{array}{ccccc} & X_3 & X_2 & X_1 & X_0 \\ + & 1 & 1 & 1 & 1 \\ \hline C_3 & S_3 & S_2 & S_1 & S_0 \end{array}$$



Problem 2) Design a combinational circuit that compares two four-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

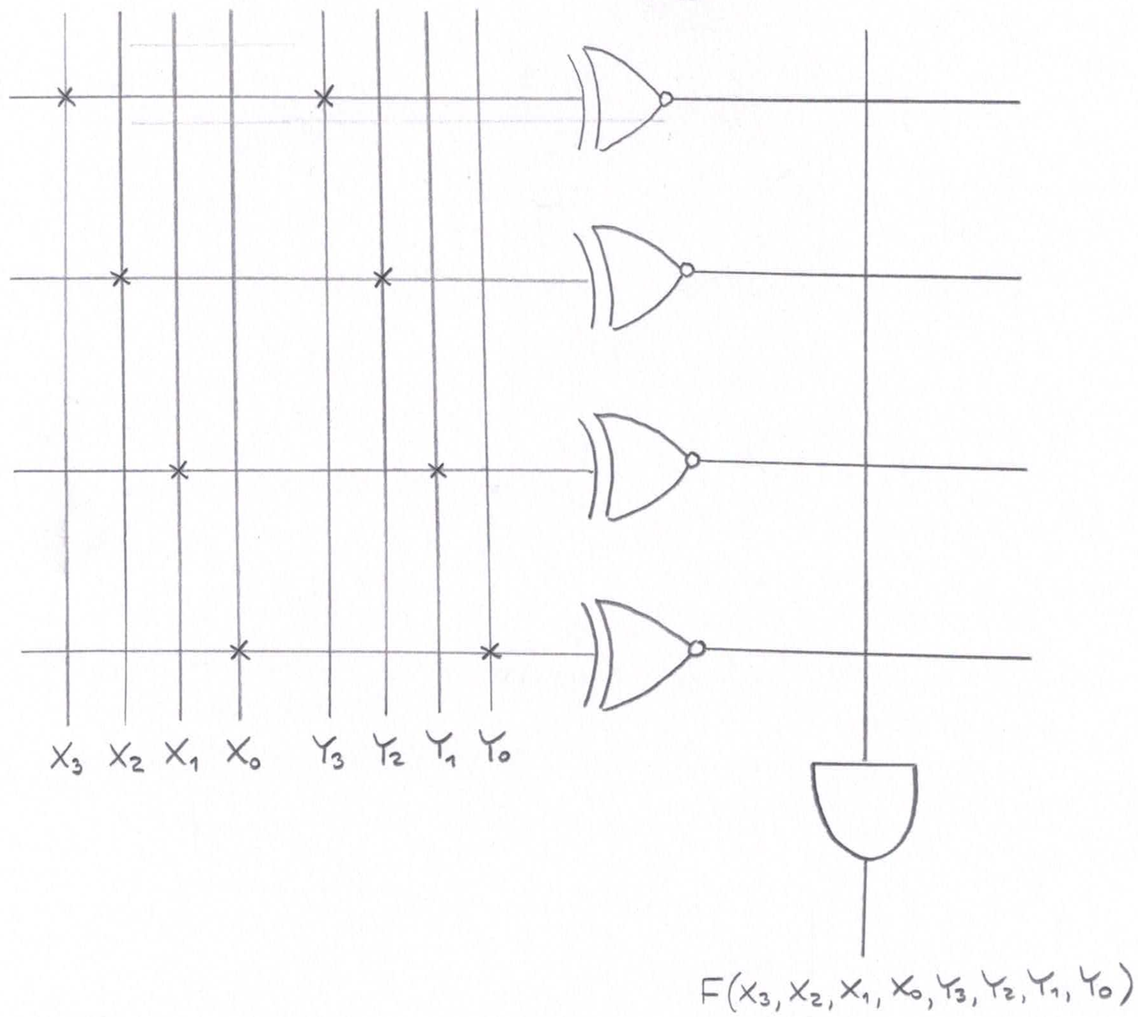
Solution. Note that we shall check if two single bits are equal or not by XNOR'ing them, that is



Therefore;

- we shall XNOR each bit of the four-bit number with the corresponding bit of the other four-bit number and then AND all four results

– we consider to compare $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$



$$F(X_3,\dots,X_0,Y_3,\dots,Y_0) = (X_0 \oplus Y_0)' \cdot (X_1 \oplus Y_1)' \cdot (X_2 \oplus Y_2)' \cdot (X_3 \oplus Y_3)'$$

Problem 3) Design a four-input priority encoder with inputs D_0, D_1, D_2, and D_3 such that input D_0 has the highest priority and input D_3 has the lowest priority.

Solution. We shall list the truth table of the priority encoder as follows

D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	d	d	0
1	d	d	d	0	0	1
0	1	d	d	0	1	1
0	0	1	d	1	0	1
0	0	0	1	1	1	1

where V denotes the valid bit indicator that is set to 1 when one or more inputs are equal to 1.

$D_0D_1 \backslash D_2D_3$	00	01	11	10
00	d	1	1	1
01				
11				
10				

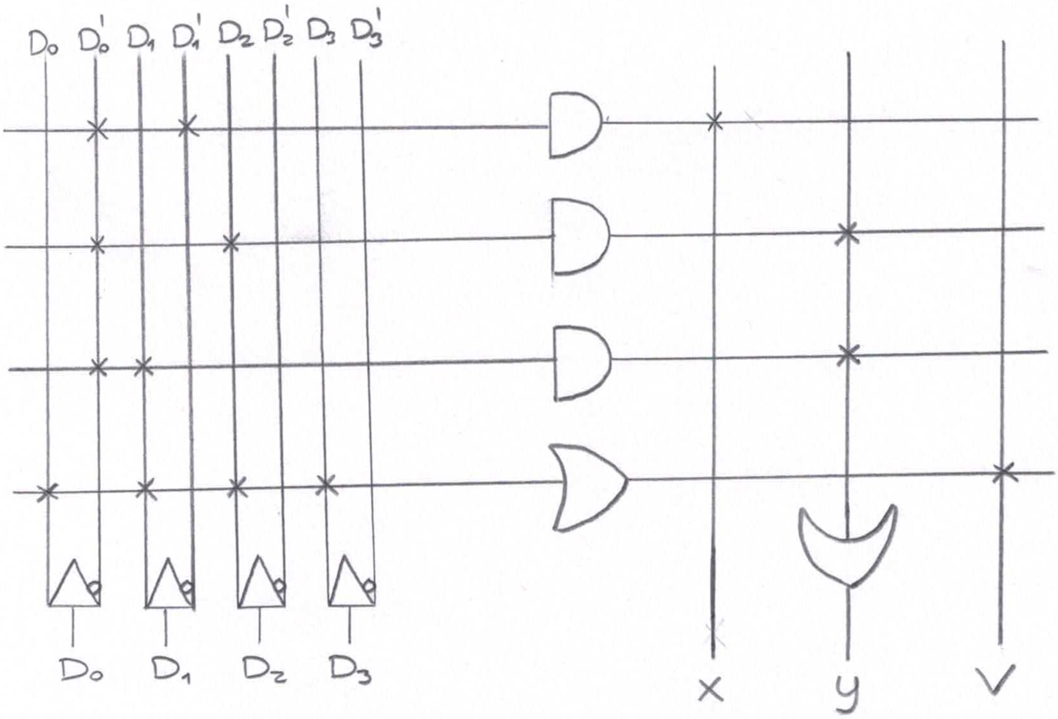
$x = D_0' D_1'$

$D_0D_1 \backslash D_2D_3$	00	01	11	10
00	d	1		
01	1	1	1	1
11				
10				

$y = D_0' D_2 + D_0' D_1$

and

$$V = D_0 + D_1 + D_2 + D_3$$



Problem 4) Implement a full adder with two 4-to-1-line multiplexers.

Solution. We know that

$$S = X \oplus Y \oplus C_{in}$$
$$= (X'Y + XY')' C_{in} + (X'Y + XY') C_{in}'$$
$$= X'Y' C_{in} + XY C_{in} + X'Y C_{in}' + XY' C_{in}'$$

and

$$C = (X \oplus Y)\, C_{in} + XY$$

$$= (X'Y + XY')\, C_{in} + XY$$

$$= X'YC_{in} + XY'C_{in} + XY$$

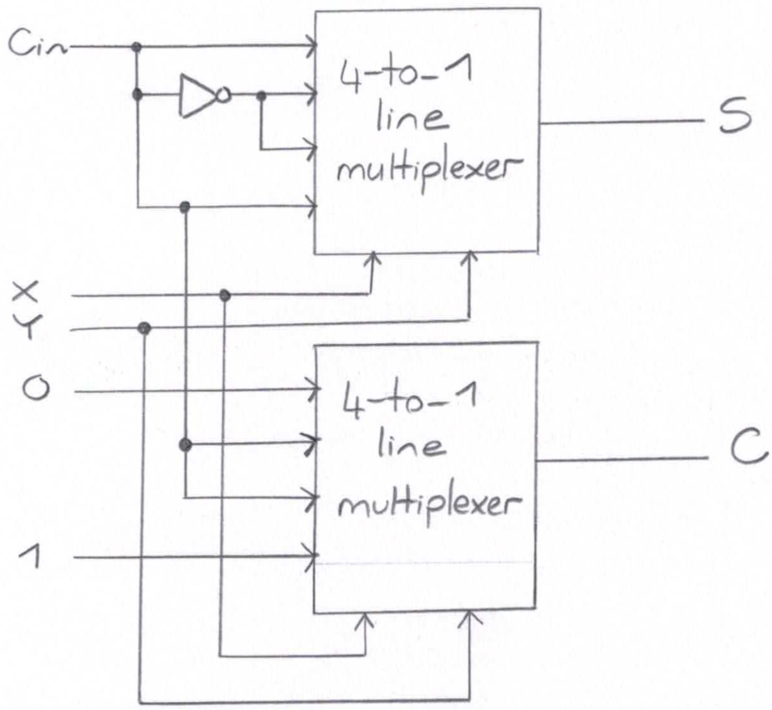
-we shall select inputs X and Y as the control inputs of the 4-to-1-line multiplexers

Therefore;

$$S = m_0 \cdot C_{in} + m_3 \cdot C_{in} + m_1 \cdot C_{in}' + m_2 \cdot C_{in}'$$

$$C = m_1 \cdot C_{in} + m_2 \cdot C_{in} + m_3 \cdot 1 + m_0 \cdot 0$$

where m_i's, $i = 0,1,2,3$ are the minterms wrt the variables X and Y



Problem 5) Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the number of product terms.

$$A(x,y,z) = \sum m(1,2,4,6)$$

$$B(x,y,z) = \sum m(0,1,6,7)$$

$$C(x,y,z) = \sum m(2,6)$$

$$D(x,y,z) = \sum m(1,2,3,5,7)$$

Solution.

$x \backslash yz$	00	01	11	10
0	0	1	0	1
1	1	0	0	1

$x \backslash yz$	00	01	11	10
0	1	1	0	0
1	0	0	1	1

$A(x,y,z) = yz' + xz' + x'y'z$

$A'(x,y,z) = x'y'z' + xz + yz$

$B(x,y,z) = x'y' + xy$

$B'(x,y,z) = x'y + xy'$

$x \backslash yz$	00	01	11	10
0	0	0	0	1
1	0	0	0	1

$x \backslash yz$	00	01	11	10
0	0	1	1	1
1	0	1	1	0

$C(x,y,z) = yz'$

$C'(x,y,z) = z + xy' + x'y'z'$

$D(x,y,z) = x'y + z$

$D'(x,y,z) = xz' + x'y'z'$

- we find that we need to utilize 6 product terms to implement these functions

Remark. The set of (A', B', C', D) can also be considered as only 6 terms are required.

Product terms	x	y	z	(T) A	(C) B	(T) C	(T) D
yz'	–	1	0	1	–	1	–
xz'	1	–	0	1	–	–	–
$x'y$	0	1	–	–	1	–	1
xy'	1	0	–	–	1	–	–
z	–	–	1	–	–	–	1
$x'y'z$	0	0	1	1	–	–	–

PLA programming table

Problem 6) Using an appropriate size ROM, design a combinational circuit that squares a 3-bit number

Solution. The largest 3-bit number is 7 and its square is 49 which needs at least 6 bits to represent in binary form. Let us now tabulate the truth table

A	B	C	S_5	S_4	S_3	S_2	S_1	S_0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

- we find that $S_1 = 0$ for all ccses

Hence;

- we require an 8×5 ROM

$$S_0 = \Sigma m(1,3,5,7)$$

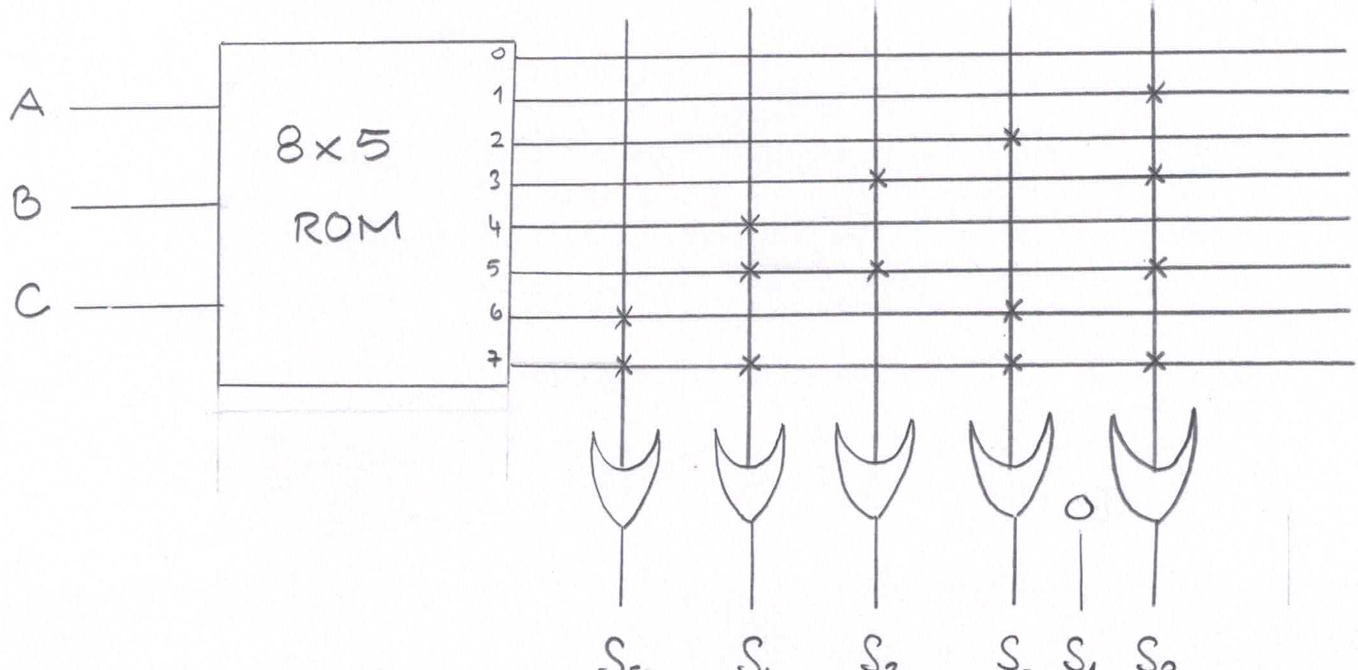
$$S_1 = 0$$

$$S_2 = \Sigma m(2,6,7)$$

$$S_3 = \Sigma m(3,5)$$

$$S_4 = \Sigma m(4,5,7)$$

$$S_5 = \Sigma m(6,7)$$



Problem 7) The following is a truth table of a three-input, four-output combinational circuit:

x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

Tabulate the PAL programming table for the circuit and mark the fuse map in the logic circuit diagram of the PAL.

Solution. We have

$$A(x,y,z) = \Sigma m(1,2,4,6)$$
$$B(x,y,z) = \Sigma m(0,1,3,6,7)$$
$$C(x,y,z) = \Sigma m(1,2,4,6,7)$$
$$D(x,y,z) = \Sigma m(1,2,3,5,7)$$

x \ yz	00	01	11	10
0		1		1
1	1			1

$A(x,y,z) = yz' + x'y'z + xy'z'$

x \ yz	00	01	11	10
0	1	1	1	
1			1	1

$B(x,y,z) = x'y' + yz + xy$

x \ yz	00	01	11	10
0		1		1
1	1		1	1

$C(x,y,z) = yz' + x'y'z + xy'z'$
$+ xy$
$= A + xy$

x \ yz	00	01	11	10
0		1	1	1
1		1	1	

$D(x,y,z) = z + x'y$

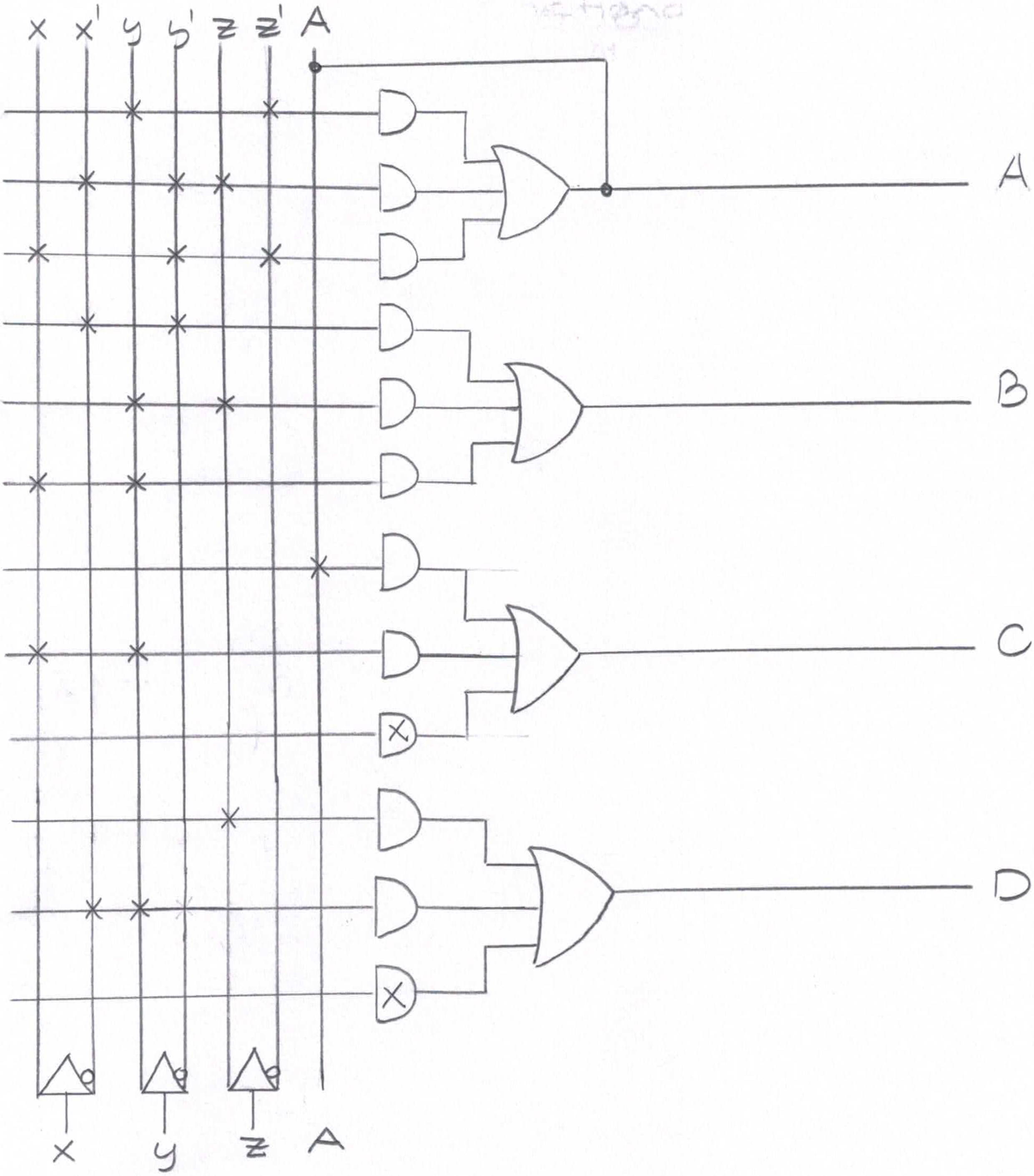
- it appears that A can be used to express the Boolean function, C

↳ thus, the function output of A can be sent as an additional input in the feedback path

Hence;

- we are able to implement each Boolean function with AT MOST 3 product terms

Product term	Inputs x y z A	Outputs
1	- 1 0 -	
2	0 0 1 -	$A = yz' + x'y'z + xy'z'$
3	1 0 0 -	
1	0 0 - -	
2	- 1 1 -	$B = x'y' + yz + xy$
3	1 1 - -	
1	- - - 1	
2	1 1 - -	$C = A + xy$
3	0 - - -	
1	- - 1 -	
2	0 1 - -	$D = z + x'y$
3	0 - - -	



PAL circuit diagram