Modulo-2 counter

- if the output at time instant of i is

$$n_i = y_{n-1}\, y_{n-2} \cdots y_1\, y_0$$

- then the output at time instant of $i+1$ is

$$n_{i+1} = y_{n-1}\, y_{n-2} \cdots y_1\, y_0 + 1$$

$$\equiv Y_{n-1}\, Y_{n-2} \cdots Y_1\, Y_0$$

- it is easily seen that

$$Y_0 = y_0 \oplus 1 = y_0'$$

$$Y_1 = y_1 \oplus y_0$$

$$\vdots$$

$$Y_i = y_i \oplus y_{i-1}\, y_{i-2} \cdots y_1\, y_0$$

In other words;

- if the outputs $y_0, \ldots, y_{n-1}$ are all 1, then

$$Y_i = y_i'$$

otherwise,

$$Y_i = y_i$$

In a similar manner;

- for a down counter

$$Y_{n-1}\, Y_{n-2} \cdots Y_1\, Y_0 = y_{n-1}\, y_{n-2} \cdots y_1\, y_0 - 1$$

- and we have

$$Y_0 = y_0 \oplus 1 = y_0'$$

$$Y_1 = y_1 \oplus y_0'$$

$$\vdots$$

$$Y_i = y_i \oplus y_{i-1}' y_{i-2}' \cdots y_1' y_0'$$

Namely,

- if the outputs $y_0, \ldots, y_{n-1}$ are all zero then

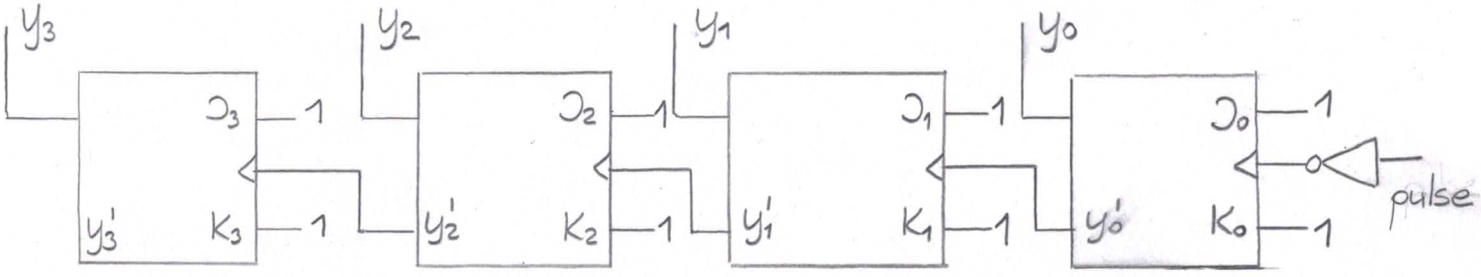
$$Y_i = y_i'$$

otherwise

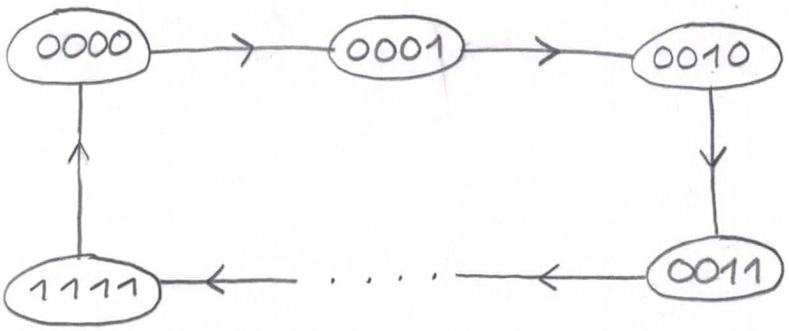
$$Y_i = y_i$$

Asynchronous counters

- let us consider a modulo-2^4 asynchronous counter example



- the corresponding state diagram is obtained as



Note that;

- when the output y_{i-1} has a transition of $1 \to 0$, the output y_i changes its state, i.e.

$y_i \to y_i'$

- for the transitions of

$0 \to 0$
$0 \to 1$
$1 \to 1$

$\Rightarrow$ y_i keeps its state as the corresponding FF is not triggerred

Maximum count rate

- when the asynchronous sequential counter is in $111\ldots11$, let a pulse signal is received

  ↳ then the flip-flops change their state in an orderly fashion

- Therefore, if a single flip-flop requires a propagation time of t_{PF}

  ↳ then there exists a need of nt_{PF} time for n flip-flops to change state

- Moreover, if we wish to have t_{read} seconds for the number to be displayed

↳ then the pulse signal period must satisfy

$$T_{pmin} \geq n T_{PF} + t_{read}$$

Hence;

- the count rate can be found as follows

$$f_{max} \leq \frac{1}{n T_{PF} + t_{read}}$$

In general;

- up counters are used as frequency dividers
- if the timing diagrams of outputs are drawn,

↳ then it can be seen that

$$T_i = 2^{i+1} T_d$$

where

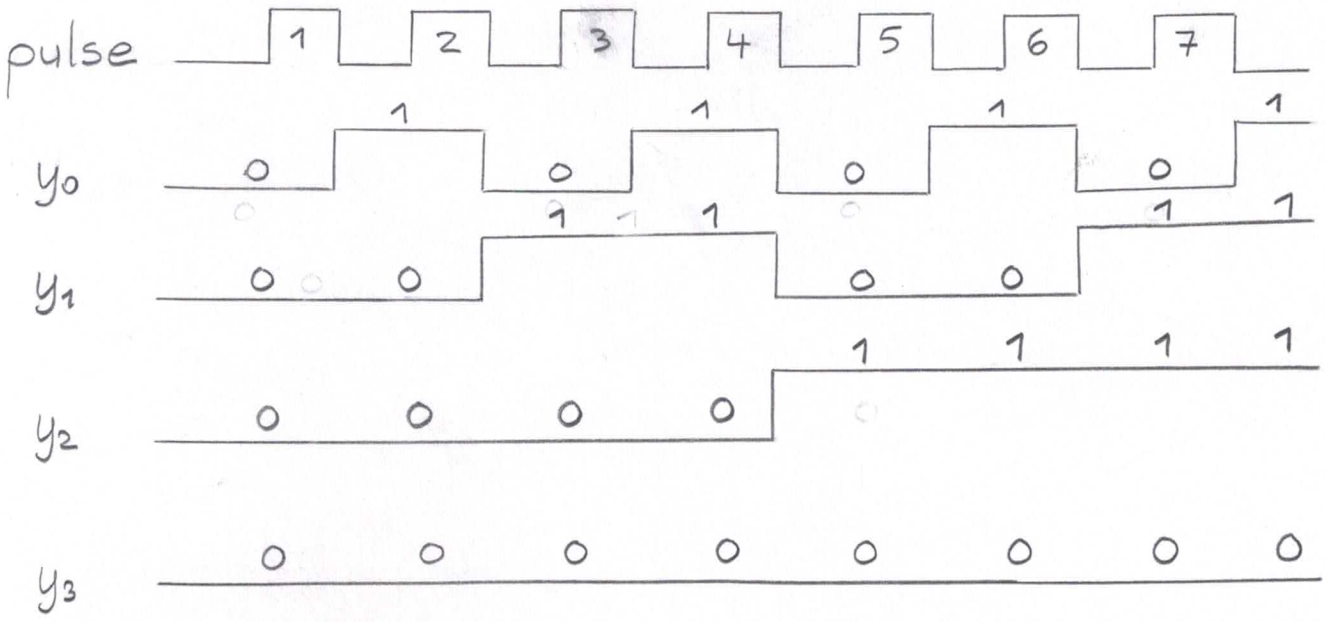
T_i : period of output y_i

T_p : period of pulse signal

Therefore;

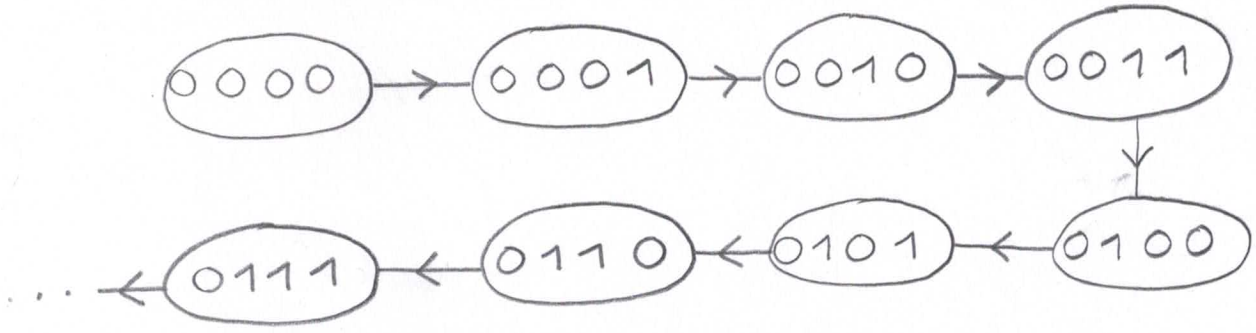
$$f_i = f_p / 2^{i+1}$$

Timing diagram of Modulo-2^4 asynchronous counter



Hence;

- we have



Remark. The asynchronous counter can be reset to 0 by applying a pulse of 1 or 0 (depending on the type of flip-flops used) to the "clear" inputs of flip-flops.

- The main advantage of asynchronous counters is the simplicity of their structure

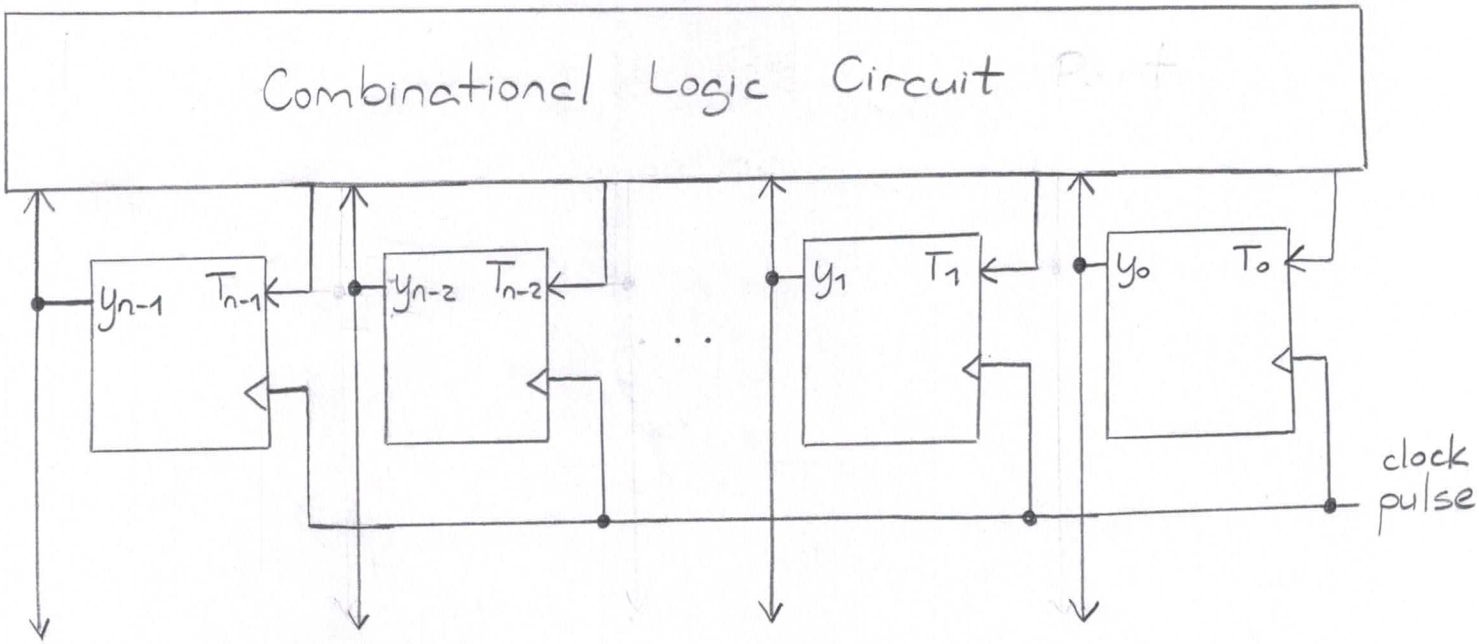
However;

- they operate more slowly compared to their synchronous counterparts
- there may exist "hazard" in the circuit

Definition. If an output in a logic circuit which should not change, has a change of $1 \to 0 \to 1$ or $0 \to 1 \to 0$ within a short time when the inputs are subject to change, it is said that there exist "static hazard" in the circuit. Moreover, if $0 \to 1$ transition occurs as $0 \to 1 \to 0 \to 1$ or $1 \to 0$ transition transition occurs as $1 \to 0 \to 1 \to 0$, it is said that there exist "dynamic hazard" in the circuit.

Synchronous sequential counters

- The pulse signal to be counted is applied to the clock inputs of all flip-flops
  - ↳ in a synchronous sequential counter
- the general structure of a synchronous sequential counter which is implemented by T type ff's
  - ↳ can be given by the following diagram



-the synchronous sequential counter counts as

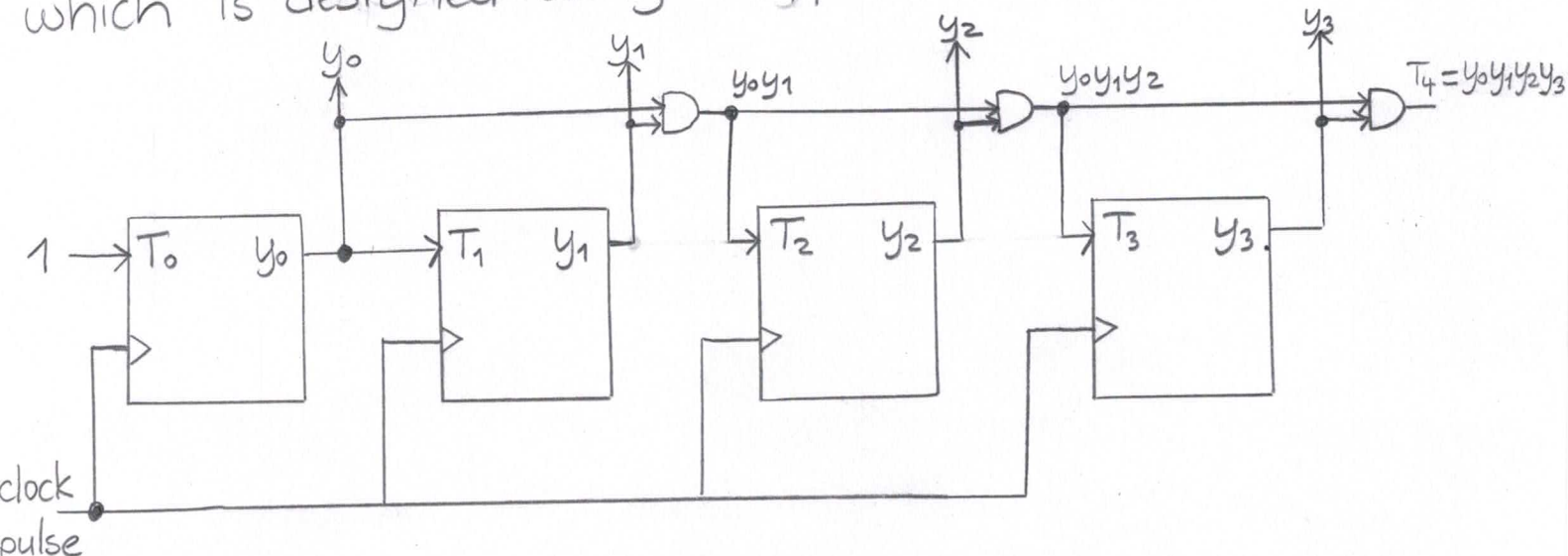
$$n_1 \rightarrow n_2 \rightarrow \cdots \rightarrow n_{k-1} \rightarrow n_k$$

where n_i, $i=1,\cdots,k$, is any number satisfying

$$0 \leq n_i \leq 2^n - 1$$

An example: Modulo-2^4 counter

-the circuit diagram of a modulo-2^4 counter which is designed using T ff's is shown as follows



-the describing function for a T type ff is

$$Y = y \oplus T$$

Hence;

$$T_i = y_i \oplus Y_i \,,\; y_i \oplus y_i = 0 \Rightarrow T_i = y_{i-1} y_{i-2} \cdots y_2 y_1$$

Maximum count rate

- If the clock pulse is received when the counter output is

$$y_3 y_2 y_1 y_0 = 1110$$

- then after t_{PF} sec., the 1st ff is trigerred and $y_0 = 1$ is achieved and

↳ received by the 1st AND gate

- let t_{AND} represent propagation delay of AND gate

- then after $(t_{PF} + t_{AND})$ sec., the 1st AND gate output becomes 1

- and after $(t_{PF} + 2t_{AND})$ sec., the 2nd AND gate output becomes 1

Therefore;

- in a modulo-2^n counter, the last AND gate output becomes 1

  ↳ after $t_{PF} + (n-2)t_{AND}$

- then if $t_{read} = 0$, we need to have

$$t_{pmin} \geq t_{PF} + (n-2)t_{AND}$$

$$\Rightarrow f_{max} \leq \frac{1}{t_{PF} + (n-2)t_{AND}}$$