Selected Problems – IX

Problem 1) Design a sequential circuit with two JK flip-flops A and B and two inputs E and F. If $E=0$, the circuit remains in the same state regardless of the value of F. When $E=1$ and $F=1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E=1$ and $F=0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

Solution. We have the following extended state table as

inputs E	F	present states y_A	y_B	next states Y_A	Y_B	flip-flop inputs J_A	K_A	J_B	K_B
0	d	0	0	0	0	0	d	0	d
0	d	0	1	0	1	0	d	d	0
0	d	1	0	1	0	d	0	0	d
0	d	1	1	1	1	d	0	d	0
1	1	0	0	0	1	0	d	1	d
1	1	0	1	1	0	1	d	d	1
1	1	1	0	1	1	d	0	1	d
1	1	1	1	0	0	d	1	d	1
1	0	0	0	1	1	1	d	1	d
1	0	0	1	0	0	0	d	d	1
1	0	1	0	0	1	d	1	1	d
1	0	1	1	1	0	d	0	1	d

J_A :

E \ Fy_B	00	01	11	10
0		d	d	
1	$\boxed{1}$		$\boxed{1}$	

$$J_A = EF'y_B' + EFy_B$$
$$= E(F \oplus y_B)'$$

K_A :

$E \backslash F y_B$	00	01	11	10
0	.	d	d	.
1	1	.	1	.

$$K_A = EF'y_B' + EFy_B$$
$$= E(F \oplus y_B)'$$

J_B :

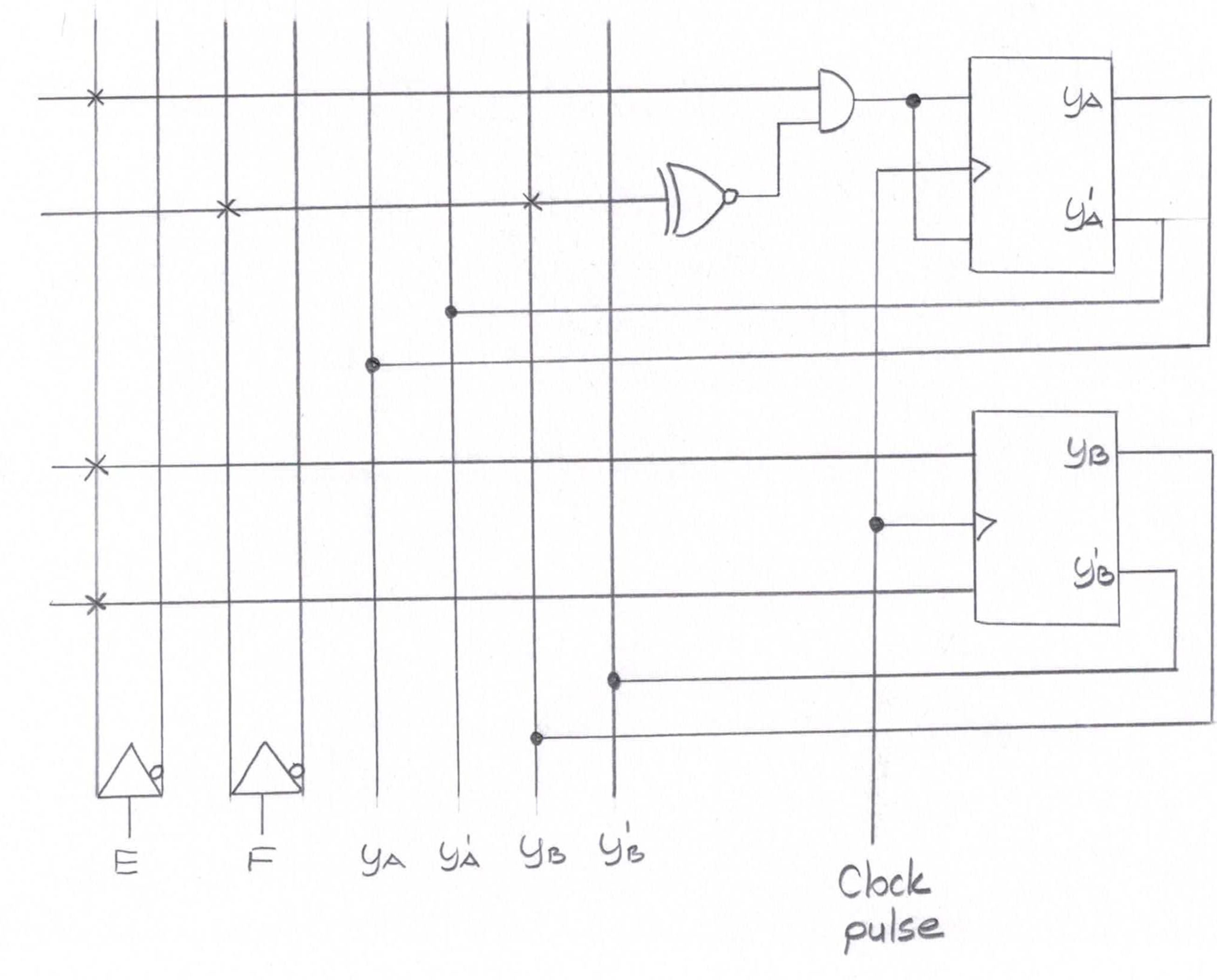
$E \backslash F y_A$	00	01	11	10
0	.	.	.	.
1	1	1	1	1

$$J_B = E$$

$E \backslash F y_A$	00	01	11	10
0	.	.	.	.
1	1	d	1	1

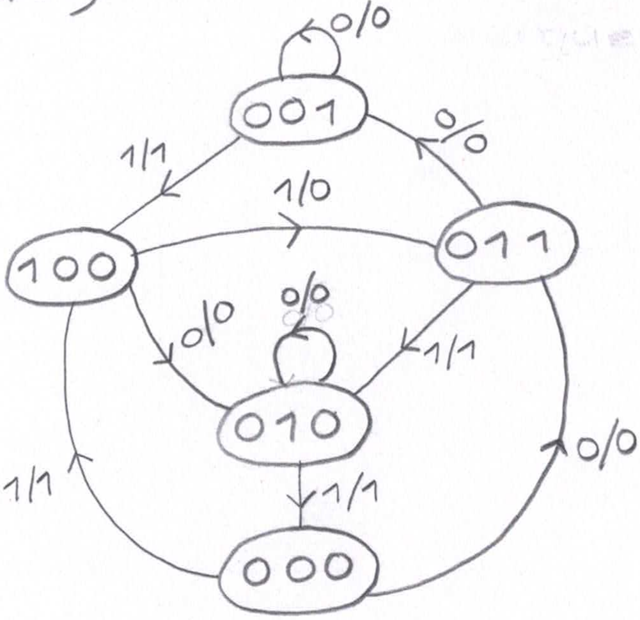
$$K_B = E$$

and the circuit diagram can be drawn as



PS 9.2

Problem 2) A sequential circuit has three flip-flops A, B, and C ; one input x and one output y. The state diagram is shown as



The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

a. Use D flip-flops in the design.

b. Use JK flip-flops in the design.

Solution.

a. We construct the extended state table as

x	y_A	y_B	y_C	Y_A	Y_B	Y_C	D_A	D_B	D_C	Z
0	0	0	0	0	1	1	0	1	1	0
1	0	0	0	1	0	0	1	0	0	1
0	0	0	1	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1	0	0	1
0	0	1	0	0	1	0	0	1	0	0
1	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	1	0	0	1	0
1	0	1	1	0	1	0	0	1	0	1
0	1	0	0	0	1	0	0	1	0	0
1	1	0	0	0	1	1	0	1	1	0

- we treat the unused states 101, 110, 111 as don't

D_A :

$xy_A \backslash y_By_C$	00	01	11	10
00				
01		d	d	d
11		d	d	d
10	1	1		

$$D_A = x y_A' y_B'$$

D_B :

$xy_A \backslash y_By_C$	00	01	11	10
00	1			1
01	1	d	d	d
11	1	d	d	d
10			1	

$$D_B = x'y_C' + y_A + x y_B y_C$$

D_C:

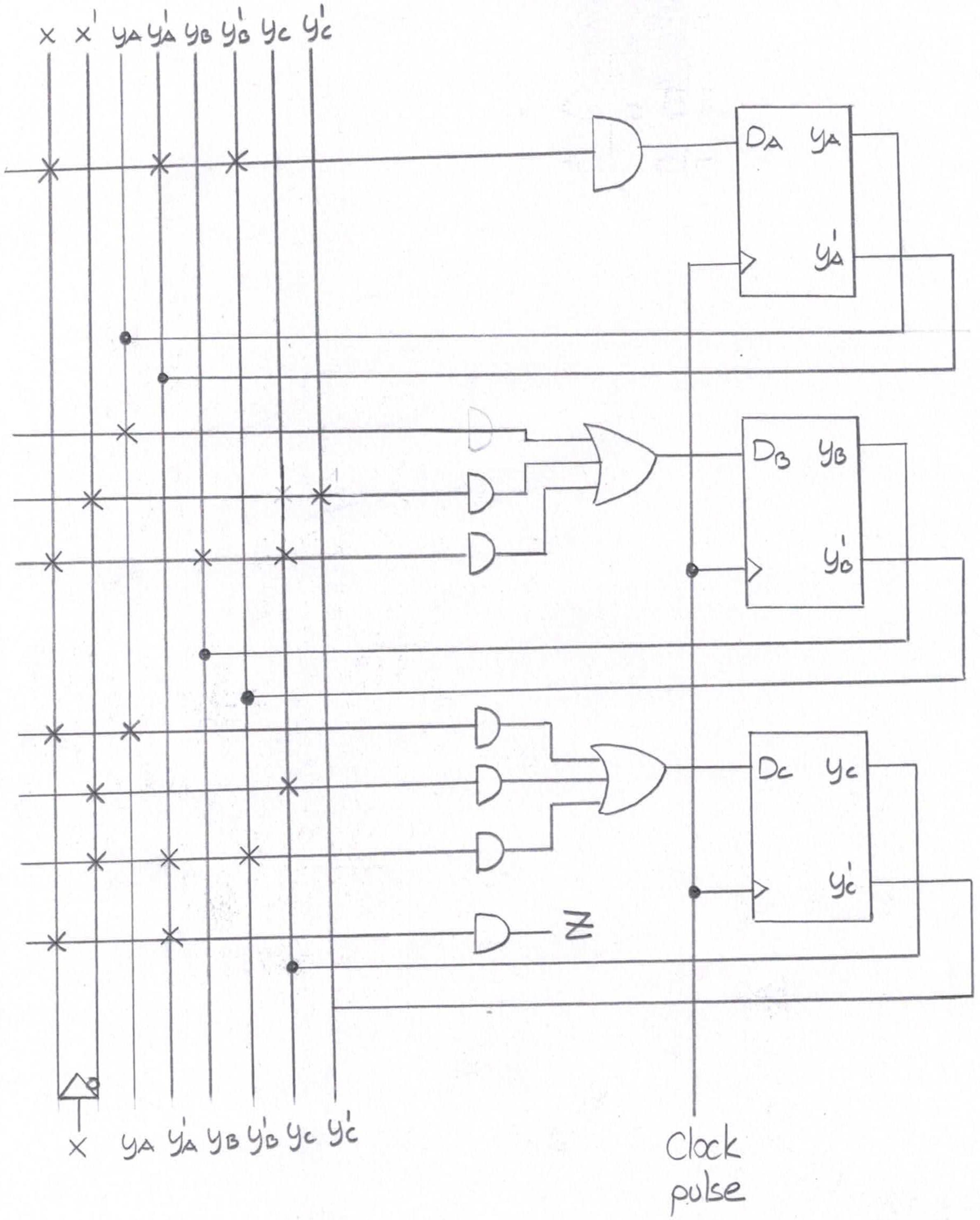
$xy_A \backslash y_By_C$	00	01	11	10
00	1	1	1	
01		d	d	d
11	1	d	d	d
10				

$$D_C = x y_A + x' y_C + x' y_A' y_B'$$

Z :

$xy_A \backslash y_By_C$	00	01	11	10
00				
01		d	d	d
11		d	d	d
10	1	1	1	1

$$Z = x y_A'$$



Now ;
- we check if the sequential circuit is locked or not
- when the state machine goes to the unused states

x	y_A	y_B	y_C	Y_A	Y_B	Y_C
0	1	0	1	0	1	1
1	1	0	1	0	1	1
0	1	1	0	0	1	0
1	1	1	0	0	1	1
0	1	1	1	0	1	1
1	1	1	1	0	1	1

$\Rightarrow$ it returns to one of the used states

Hence ;

- the state machine is NOT a locked type,

that is ;

(i) it is self-correcting

b. We again construct the extended state table

x	y_A	y_B	y_C	Y_A	Y_B	Y_C	J_A	K_A	J_B	K_B	J_C	K_C	Z
0	0	0	0	0	1	1	0	d	1	d	1	d	0
1	0	0	0	1	0	0	1	d	0	d	0	d	1
0	0	0	1	0	0	1	0	d	0	d	d	0	0
1	0	0	1	1	0	0	1	d	0	d	d	1	1
0	0	1	0	0	1	0	0	d	d	0	0	d	0
1	0	1	0	0	0	0	0	d	d	1	0	d	1
0	0	1	1	0	0	1	0	d	d	1	d	0	0
1	0	1	1	0	1	0	0	d	d	0	d	1	1
0	1	0	0	0	1	0	d	1	1	d	0	d	0
1	1	0	0	0	1	1	d	1	1	d	1	d	0

J_A, K_A

$xy_A \backslash y_By_C$	00	01	11	10
00	.	.	.	d
01	d	d	d	d
11	d	d	d	d
10	1	1	.	.

$J_A = x y_B'$, $K_A = 1$

$xy_A \backslash y_By_C$	00	01	11	10
00	1	.	d	d
01	1	d	d	d
11	1	d	d	d
10	.	.	d	d

$J_B = y_A + x'y_C'$

$xy_A \backslash y_By_C$	00	01	11	10
00	d	d	1	·
01	d	d	d	d
11	d	d	d	d
10	d	d	·	1

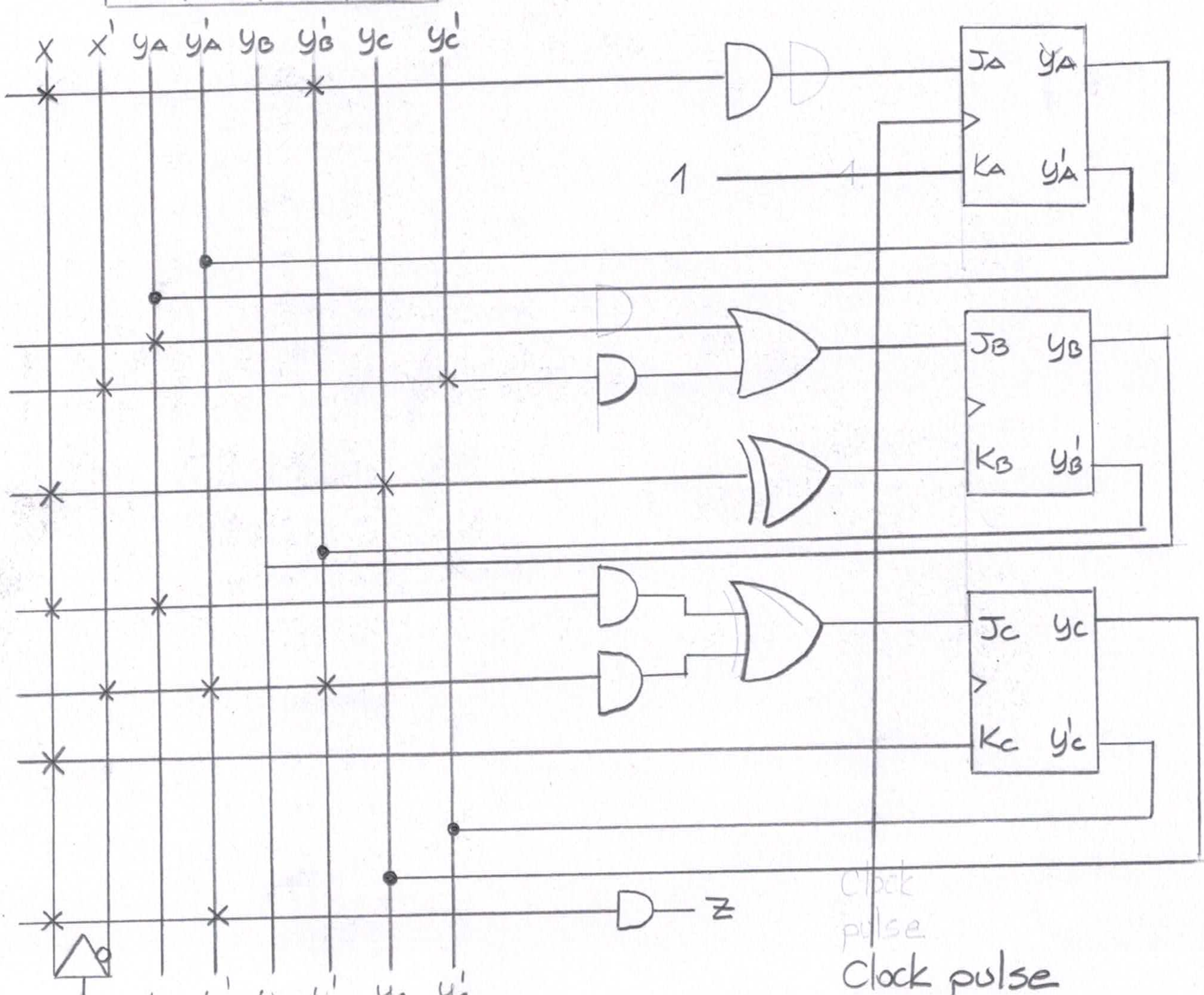
$$K_B = x'y_C + xy_C'$$
$$= x \oplus y_C$$

$xy_A \backslash y_By_C$	00	01	11	10
00	1	d	d	·
01	·	d	d	d
11	1	d	d	d
10	·	d	d	·

$$J_C = xy_A + x'y_A'y_B'$$

$xy_A \backslash y_By_C$	00	01	11	10
00	d	·	·	d
01	d	d	d	d
11	d	d	d	d
10	d	1	1	d

$$K_C = x$$



Now ;

-we check if the sequential circuit is locked or not

-when the state machine goes to the unused

states

X	y_A	y_B	y_C	Y_A	Y_B	Y_C
0	1	0	1	0	1	0
1	1	0	1	0	1	0
0	1	1	0	0	1	0
1	1	1	0	0	0	1
0	1	1	1	0	0	0
1	1	1	1	0	1	0

$\Downarrow$

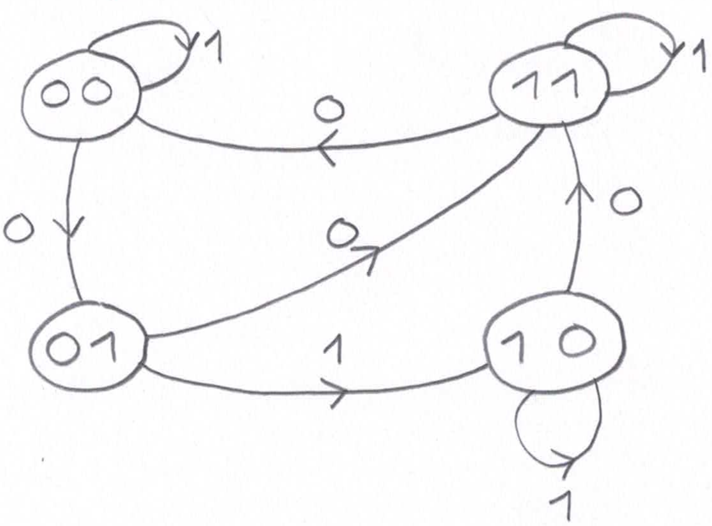
it returns to one of the used states

Therefore ;

-the state machine is NOT a locked type

↳ that is, it is self-correcting

Problem 3) Consider the following state-diagram



Design the sequential circuit specified by the state diagram depicted above using T type flip-flops.

Solution. We construct the extended state table

x	y_A	y_B	Y_A	Y_B	T_A	T_B
0	0	0	0	1	0	1
1	0	0	0	0	0	0
0	0	1	1	1	1	0
1	0	1	1	0	1	1
0	1	0	1	1	0	1
1	1	0	1	0	0	0
0	1	1	0	0	1	1
1	1	1	1	1	0	0

$x \backslash y_Ay_B$	00	01	11	10
0		1	1	
1		1		

$$T_A = x'y_B + y_A'y_B$$

$x \backslash y_Ay_B$	00	01	11	10
0	1		1	1
1		1		

$$T_B = x'y_B' + x'y_A + xy_A'y_B$$