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1.Project description

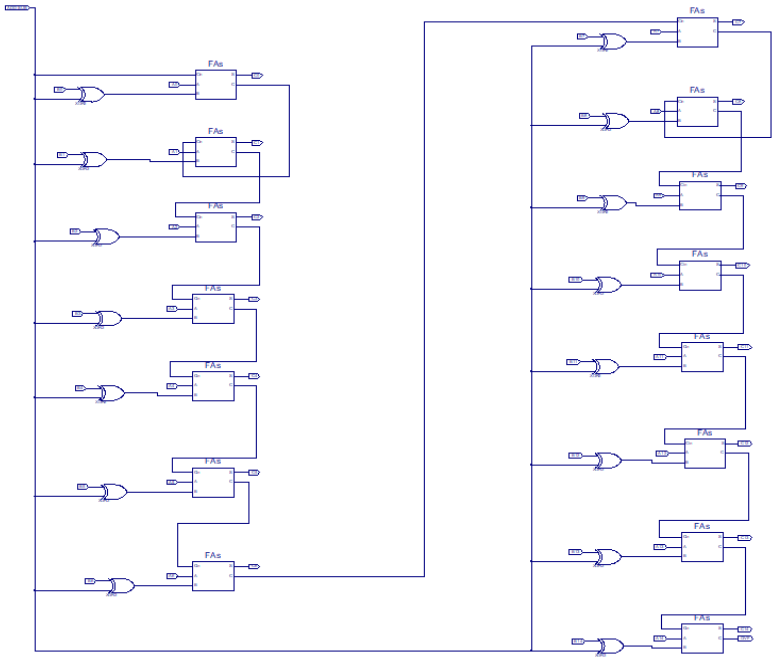
I have created 2 schemas;

Firstly, I created 15-bits ripple carry adder/ subtractor. I created a subchema named as FAs to make a symbol of 1-bit FullAdder. Then duplicated it 15 times in my main schema named as asdasd(sorry for the name but I created 10 schemas so i run out of names, because there was an error in Isim. TA helped me and the solution was the Run as Administrator ISE DESIGN, so that was very sad). Then, I added add/sub functionality with XORs that controls both c0 and B values, and checked it by Isim.

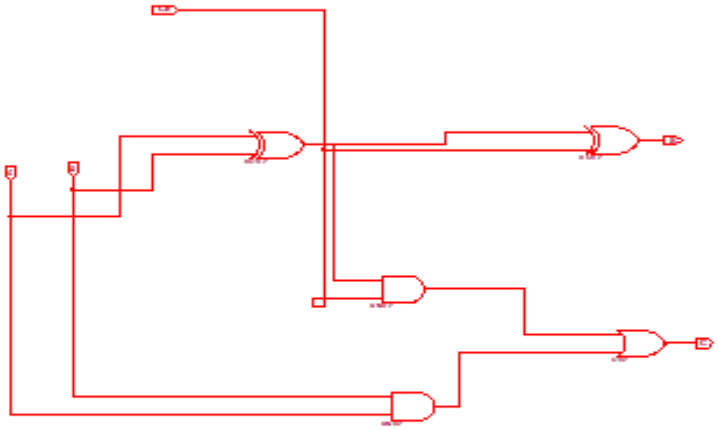
Secondly, 15-bit hybrid adder/subtractor by five 3-bits carry lookahead adders. I created a schema (CLAs) of CLA to use as a symbol. Then duplicated it in main schema (CLAsche). Then I added add/sub functionality with XORs that controls both c0 and B values. After the CLA I found sums and checked it in Isim.

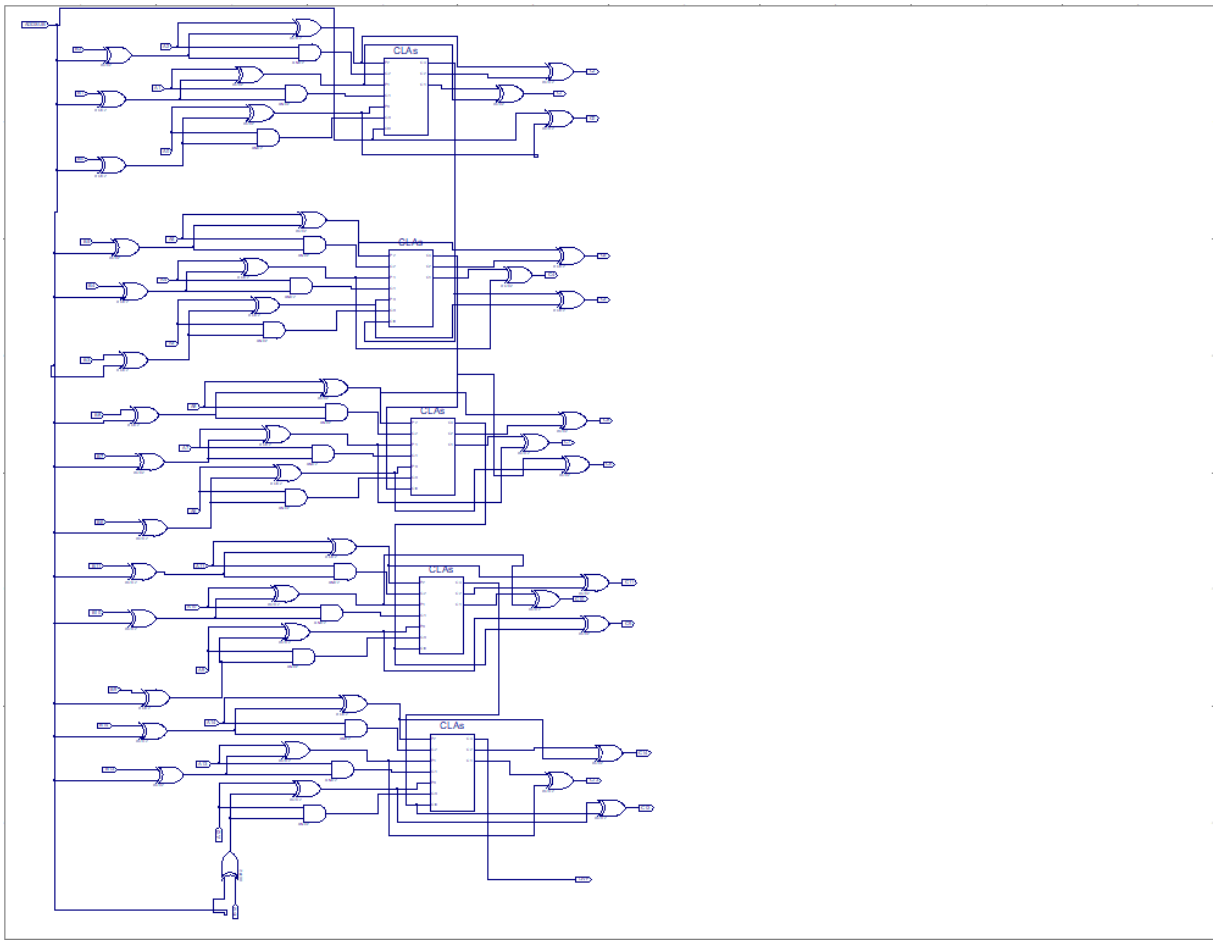
2-) First design

2-1) Sche



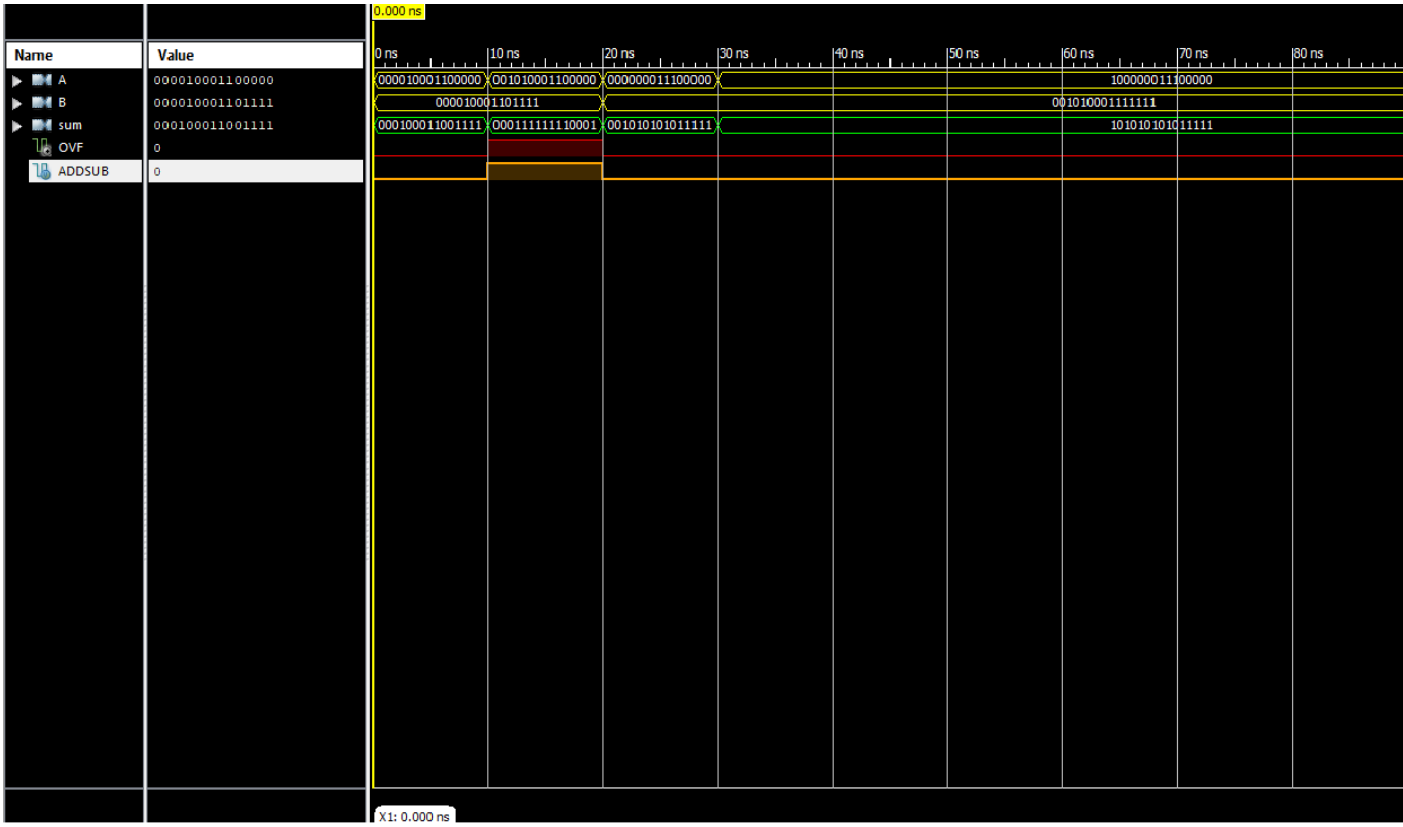
15 times repeated FAs with add/sub controller





SYMBOL OF FA

2-2) Simulation



These are the simulation results and the decimal number are as below;

1-) A(1120) + B(1135) = C(2255) Addition 0/ no over flow 0

2- A(5216) - B (1135) = C(4081) subtraction 1/ there is overflow 1

3-) A(224) + B(5247) = C(5471) Addition 0/ no over flow 0

4-) A(-16160) + B(5183) = C(-10913) Addition 0(A is negative, b is positive) / no overflow 0

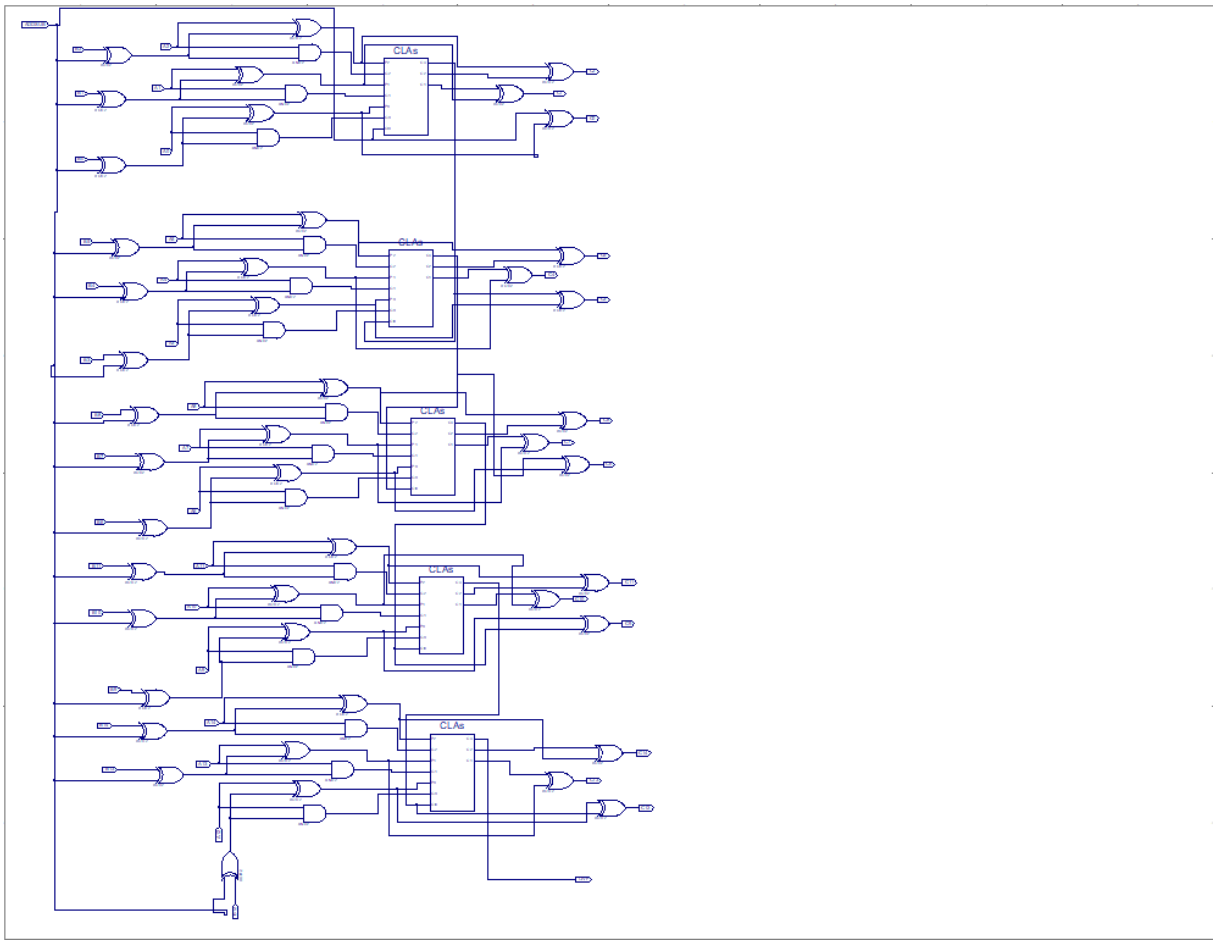
2-3) Implementation Results

time delay 41.941 ns,

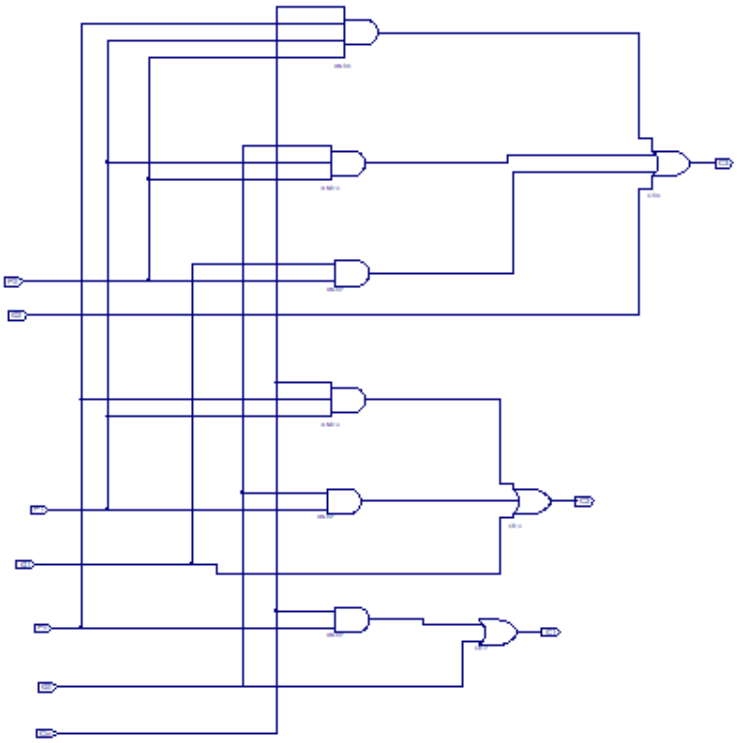
Number of 4 input LUTs: 54

3-) SECOND DESIGN

3-1)SCHEMATICS

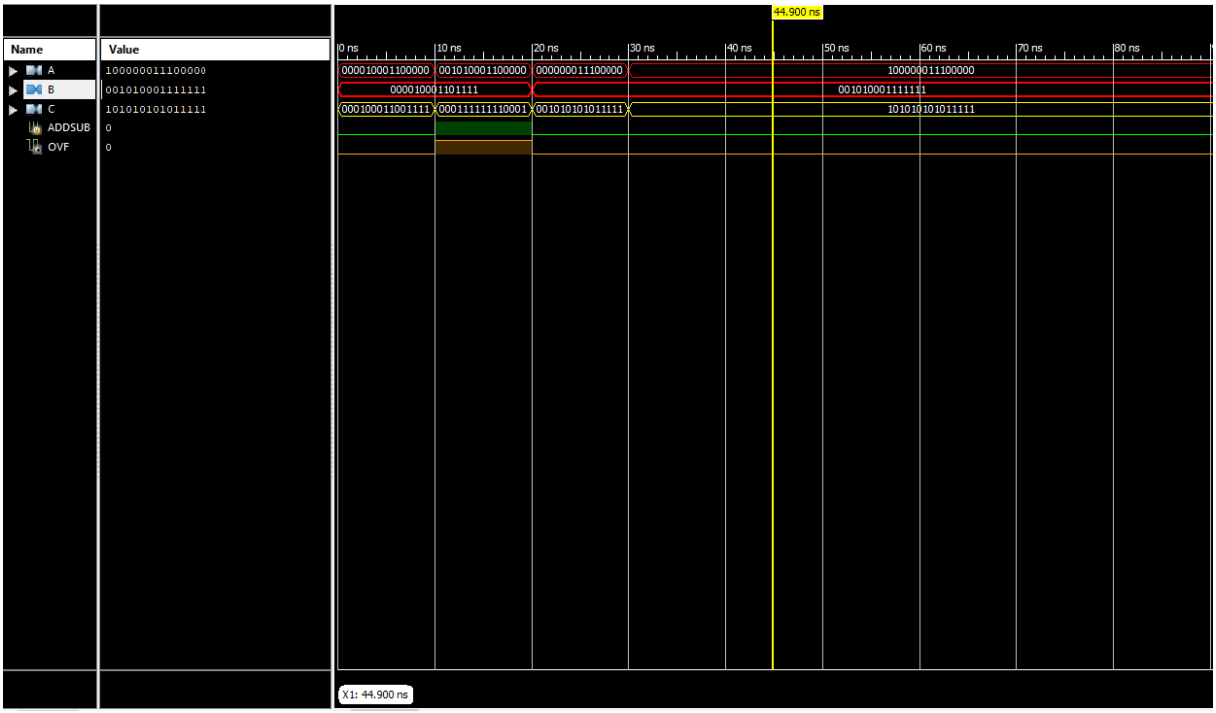


5 times 3-bits CLAs with add/sub controller and sum operations



3-bits CLA symbol

3-2) SIMULATION



These are the simulation results and the decimal number are as below;

1-) A(1120) + B(1135) = C(2255) Addition 0/ no over flow 0

2- A(5216) - B (1135) = C(4081) subtraction 1 / there is overflow 1

3-) A(224) + B(5247) = C(5471) Addition 0/ no over flow 0

4-) A(-16160) + B(5183) = C(-10913) Addition 0 (A is negative, b is positive) / no overflow 0

(same values as FA)

3-3) Implementation Results

time delay 21.095ns,

Number of 4 input LUTs: 84

4-) DISCUSSION

1. Which one of the two is better in terms of area?

Clearly, FA is better in terms of area because it is less complex than CLA.

FA has 54 LUTs while CLA has 84. FA requires less area than CLA.

2. Which one of the two is better in terms of time?

Clearly, CLA is better in terms of time because it has less delay than FA.

FA's time delay is 41.941 ns while CLA has 21.095ns. CLA is clearly faster than FA.

3. Define a new metric to measure the time-area tradeoff in two designs by multiplying the number of LUTs and time. Which one of the two designs is better in terms of this new metric?

For FA: 54*41.941 = 2264,814

For CLA : 84. 21.095 = 1771,98

CLA is better.

4. State the requirements of a good design in terms of area, time and the new metric you've defined.

To make a better design we need to use less area but need to be faster. So, time should be less too.

That shows us the new metric we have defined measures the designs in terms of product of these two which means better if they are less. So, if the result of new metric less, the design is better.

CLA is better.