NAME- SURNAME /SID : Tuğcan Barbin/ 25168

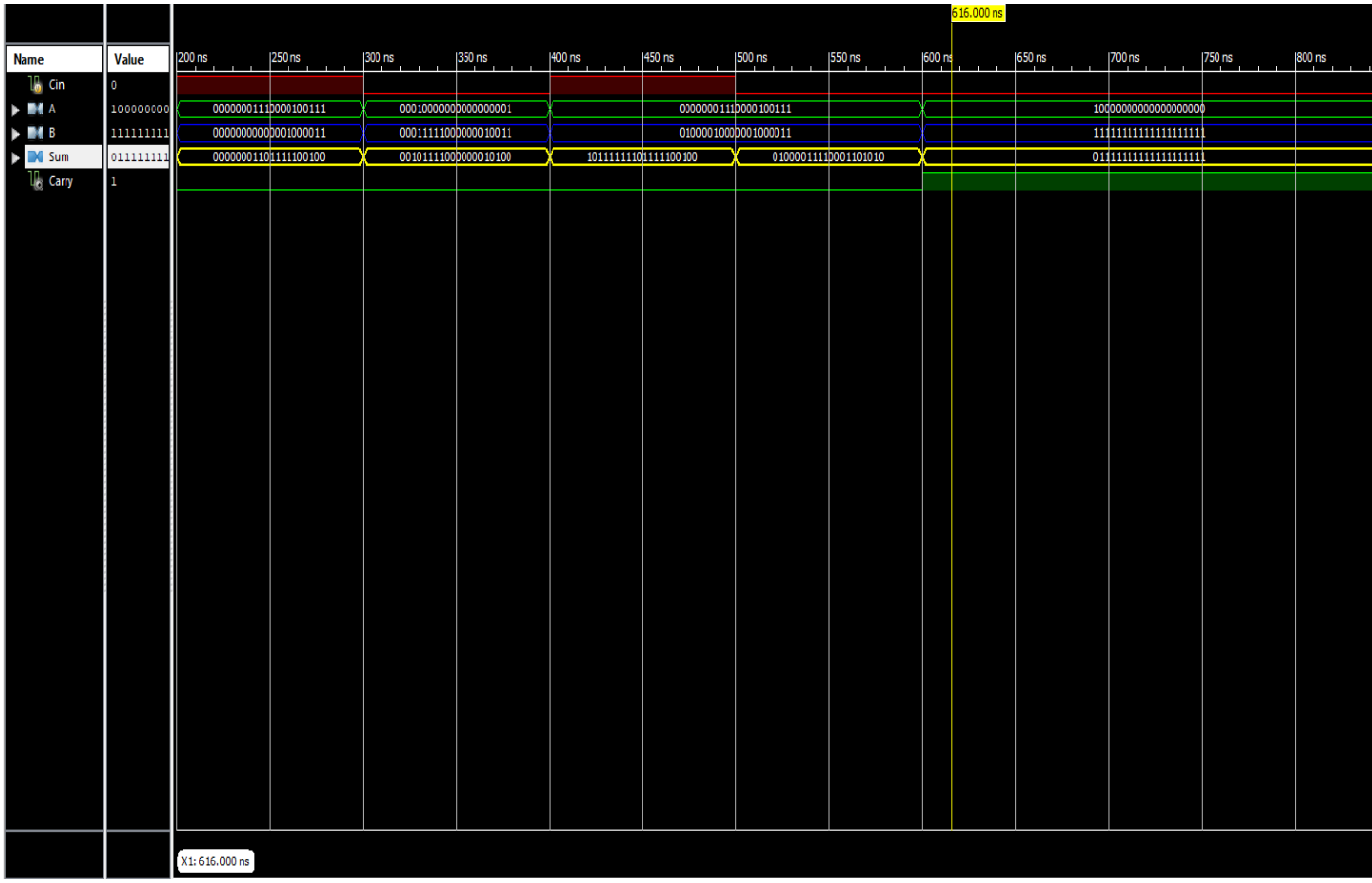
Project description

I have created 2 verilogs;

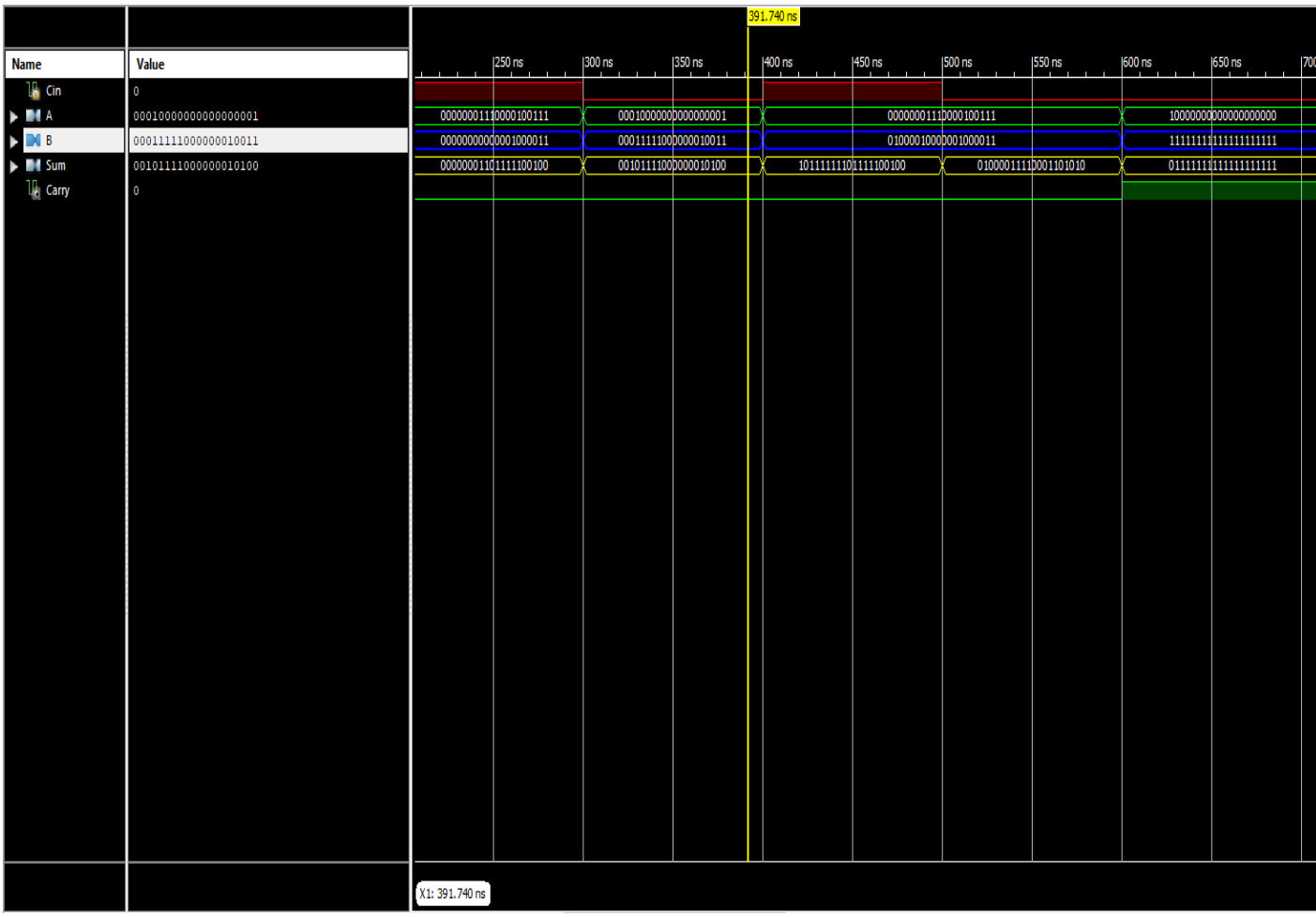
Firstly, I created 1 Full adder/ subtractor. Then, I created another Verilog to make a hierarchical design to build 20-bit RCA with Full adders that I have created.

Secondly, 20-bit CLA adder/subtractor by four 5-bits carry lookahead adders. I created a schema of CLA with 5bit to use as template to build 20-bit CLA.

1-)Screenshots



Screenshot of waveform of RCA.



Screenshot of waveform of CLA.

2-) QUESTİONS

2-1-) Differences between RCA and CLA in terms of synthesis and implementation is smaller than the previous lab.

CLA

27,949 ns

LUTs 47

RCA

28,977ns

LUTs 40

2-2-)

RCA is better in terms of size with 40 to 47

2-3-)

CLA is better in terms of time with 27,949 ns to 28,977

2-4-)

For RCA, 28.977 * 40 = 1159,08

for CLA, 27.949 * 47 = 1313,603

for both measurements, smaller is better. So, the new metric that we created is better if smaller.

So, RCA is better.