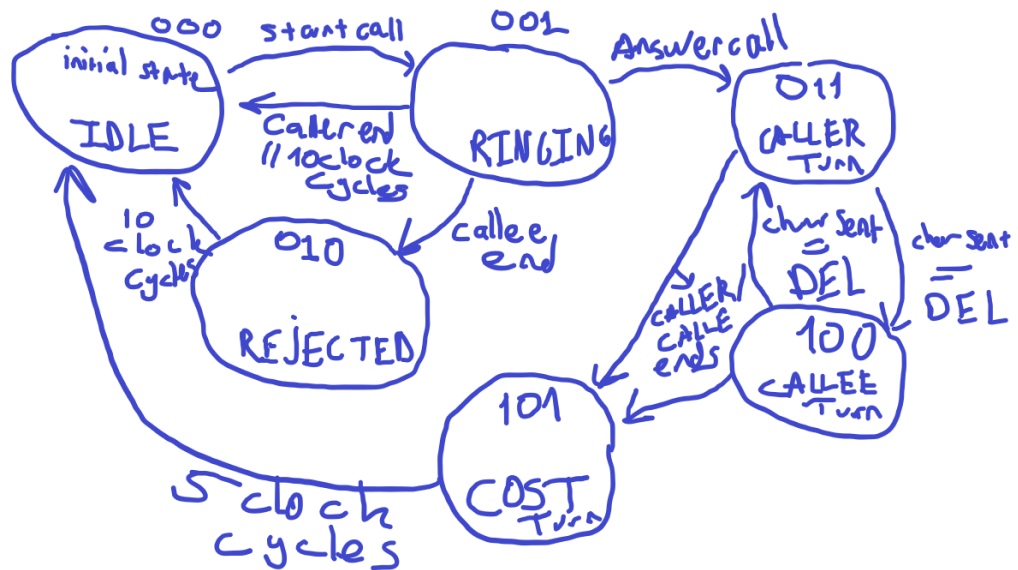


1-) I sketched up a state machine for my project;



As we can understand from sketches, I have 6 states as follows,

IF RESET == 1 THEN WE GO TO idle STATE WHICH IS INITIAL STATE.

1-1-) idle (Initial state)

At this state statusMsg is "IDLE ", and sentMsg is full of space.

If startcall, next state is ringing.

1-2-) ringing

At this state statusMsg is "RINGING " and sentMsg is full of space.

If none of the input(answer call or end call) is taken, after 10 clock cycles next state is idle

If answer call is 1, then conversation starts and next state is caller turn .

If endCallCaller is 1, then next state is idle again.

If endCallCallee is 1, then we rejected. So, next state is rejected.

1-3-) rejected

At this state statusMsg is "REJECTED" and sentMsg is full of space.

After 10 clock cycles we return to idle state.

1-4-) caller turn

At this state statusMsg is "CALLER "

And sentMsg is updated when the sendCharCaller is 1, if charSent is between 32 and 127 then it is a valid input. If input is not valid then the sentMsg is not updated.

If sentChar is DEL then next state is calleesturn and the sentMsg is reseted.

If endCallCaller or endCallCalle is 1 then next state is costturn state.

1-5-) calleesturn

At this state statusMsg is "CALLEE "

And sentMsg is updated when the sendCharCallee is 1, if charSent is between 32 and 127 then it is a valid input. If input is not valid then the sentMsg is not updated.

If sentChar is DEL then next state is calleesturn and the sentMsg is reseted.

If endCallCaller or endCallCalle is 1 then next state is costturn state.

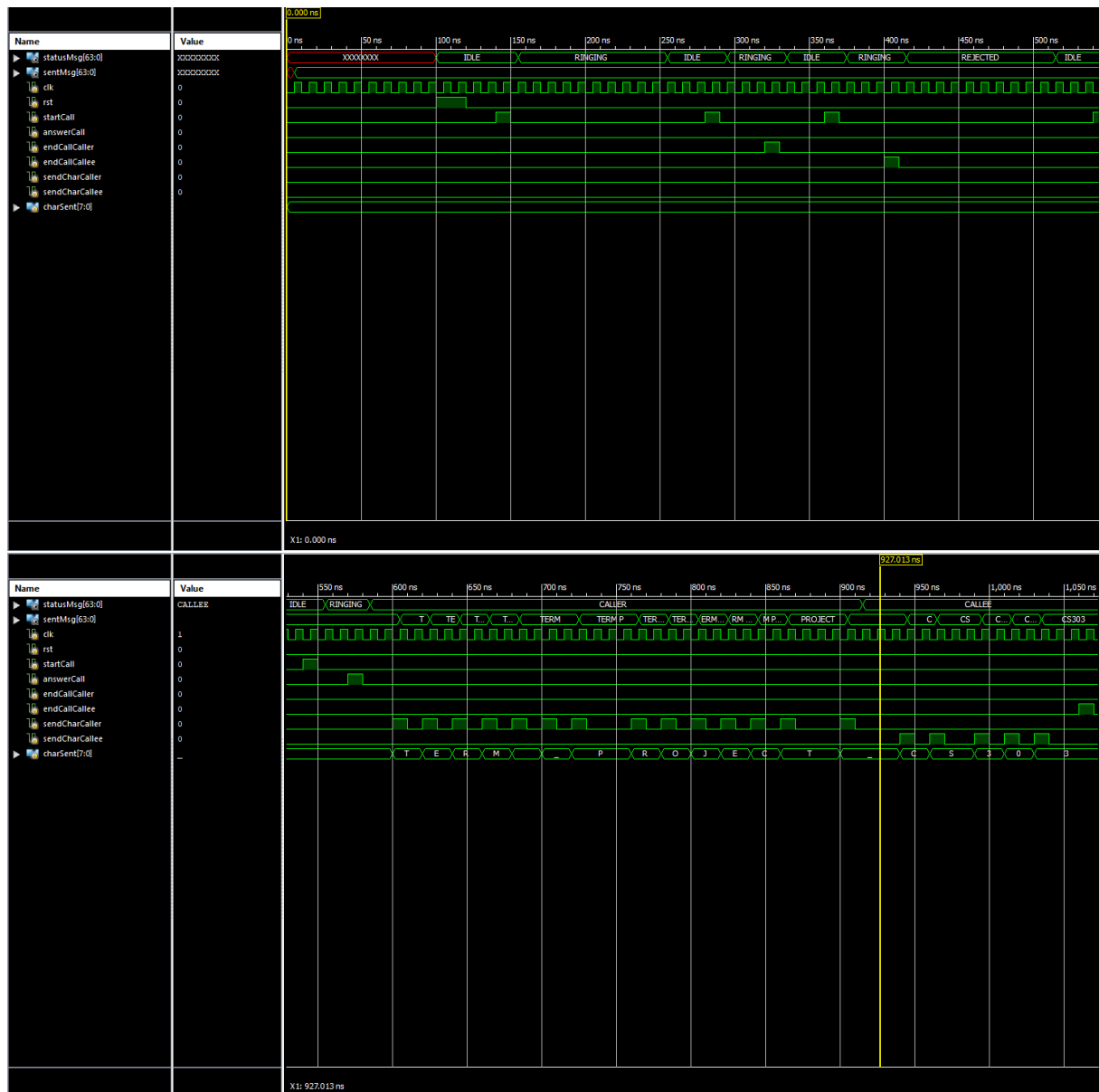
1-6-) costturn

sentMsg is updated as cost which represents the kuruş that we spent for send messages.

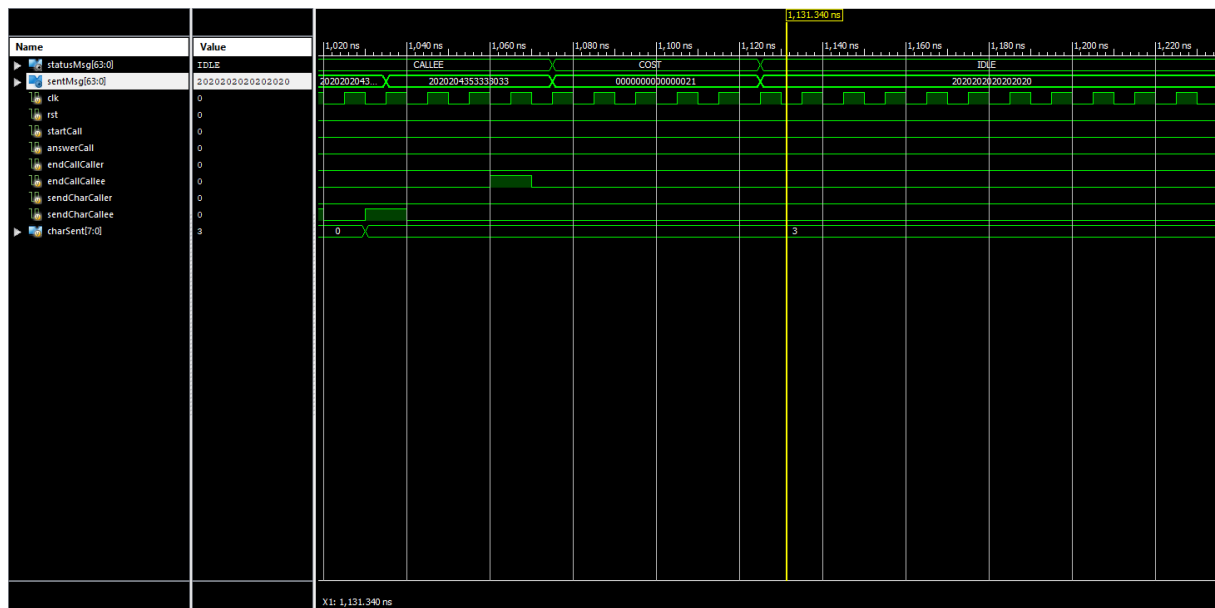
It will stay in costturn for 5 clock cycles and then next state is idle

***** clock cycles is calculated with a counter that counts the posedges of clock

2-) Simulation results showing that your design is working



FOR THE LAST SCREENSHOT I CHANGED THE REPRESENTATION OF SENTMSG FROM ASCII TO HEXADECIMAL TO REPRESENT THE COST OF CONVERSATION



3-) synthesize report

I copied some parts of it that represents I have no warning other than “More than 100% of Device resources are used” and no errors during compilation. Also, the parts that represents the area usage and time.

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.16 secs

```
=====
*                HDL Compilation                *
=====
```

Compiling verilog file "deneme222.v" in library work

Module <tel> compiled

No errors in compilation

Analysis of file <"tel.prj"> succeeded.

```
=====
*                HDL Analysis                *
=====
```

Analyzing top module <tel>.

calleesturn = 3'b100

callersturn = 3'b011

costturn = 3'b101

idle = 3'b000

rejected = 3'b010

ringing = 3'b001

Module <tel> is correct for synthesis.

Unit <tel> synthesized.

```
=====
=====
*                Final Report                *
=====
```

Final Results

RTL Top Level Output File Name : tel.ngc

Top Level Output File Name : tel

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 148

Cell Usage :

BELS : 292

GND : 1

INV : 1

LUT1 : 30

LUT2 : 12

```

# LUT2_D      : 2
# LUT3        : 39
# LUT3_D      : 1
# LUT3_L      : 3
# LUT4        : 99
# LUT4_D      : 7
# LUT4_L      : 32
# MUXCY       : 31
# MUXF5       : 1
# VCC         : 1
# XORCY       : 32
# FlipFlops/Latches : 127
# FDC         : 78
# FDE         : 32
# FDP         : 17
# Clock Buffers : 1
# BUFGP       : 1
# IO Buffers   : 147
# IBUF        : 15
# OBUF        : 132

```

```
=====
```

Device utilization summary:

```
-----
```

Selected Device : 3s100etq144-4

Number of Slices:	120 out of 960	12%
Number of Slice Flip Flops:	127 out of 1920	6%
Number of 4 input LUTs:	226 out of 1920	11%
Number of IOs:	148	

Number of bonded IOBs: 148 out of 108 137% (*)
Number of GCLKs: 1 out of 24 4%

WARNING:Xst:1336 - (*) More than 100% of Device resources are used

Partition Resource Summary:

No Partitions were found in this design.

=====

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-----+-----+-----+			
Clock Signal	Clock buffer(FF name)	Load	
-----+-----+-----+			
clk	BUFGP	127	
-----+-----+-----+			

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load
rst	IBUF	95

Timing Summary:

Speed Grade: -4

Minimum period: 6.979ns (Maximum Frequency: 143.287MHz)

Minimum input arrival time before clock: 10.282ns

Maximum output required time after clock: 4.571ns

Maximum combinational path delay: No path found

Timing Detail:

Total 10.282ns (7.701ns logic, 2.581ns route)
(74.9% logic, 25.1% route)

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 106 / 106

Offset: 4.571ns (Levels of Logic = 1)

Source: counter_0 (FF)

Destination: counter<0> (PAD)

Source Clock: clk rising

Data Path: counter_0 to counter<0>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)


```
-----
FDC:C->Q      7 0.591 0.708 counter_0 (counter_0)
OBUF:I->O      3.272      counter_0_OBUF (counter<0>)
-----
```

```
Total          4.571ns (3.863ns logic, 0.708ns route)
                (84.5% logic, 15.5% route)
```

=====

Total REAL time to Xst completion: 7.00 secs

Total CPU time to Xst completion: 6.61 secs

Total memory usage is 4513568 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 1 (0 filtered)

Number of infos : 49 (0 filtered)