Weekly meeting

Yeh Shun-Liang
International College of Semiconductor Technology
National Yang Ming Chiao Tung University

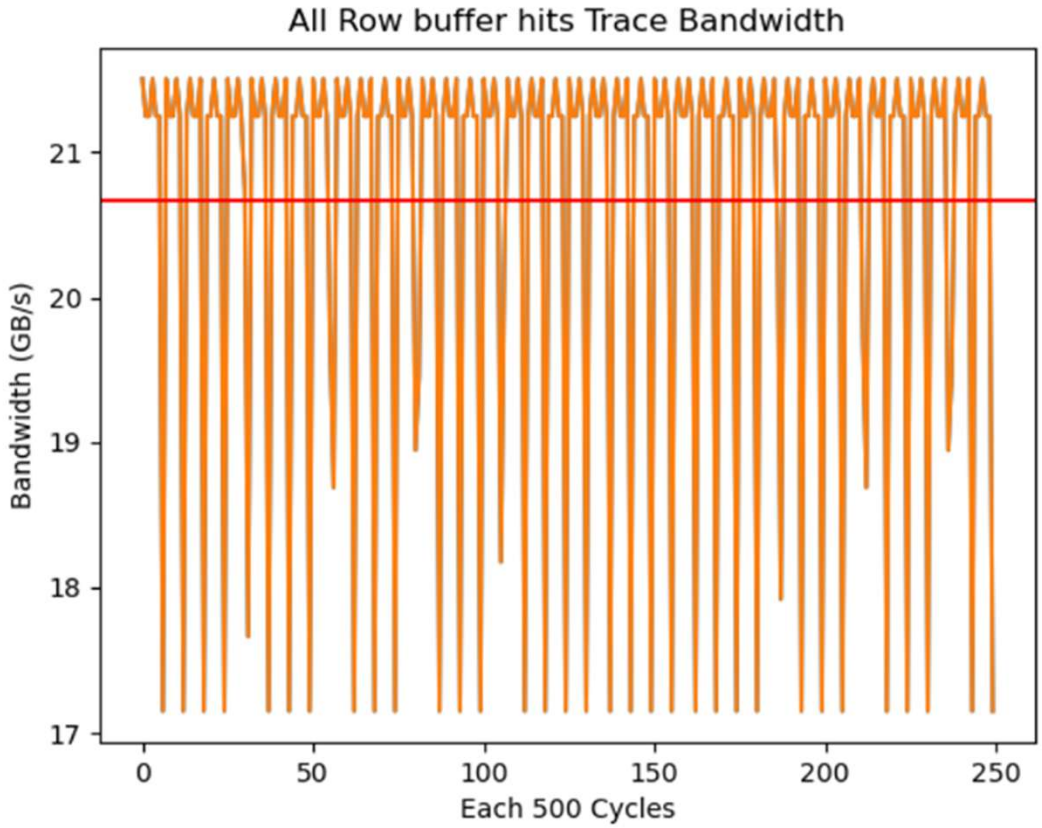
Recent Progress

- Run all row buffer hits memory trace and extract statistics
- Discuss Memory Interfaces with Sub-project's students
- Think about the detail architecture of memory controller

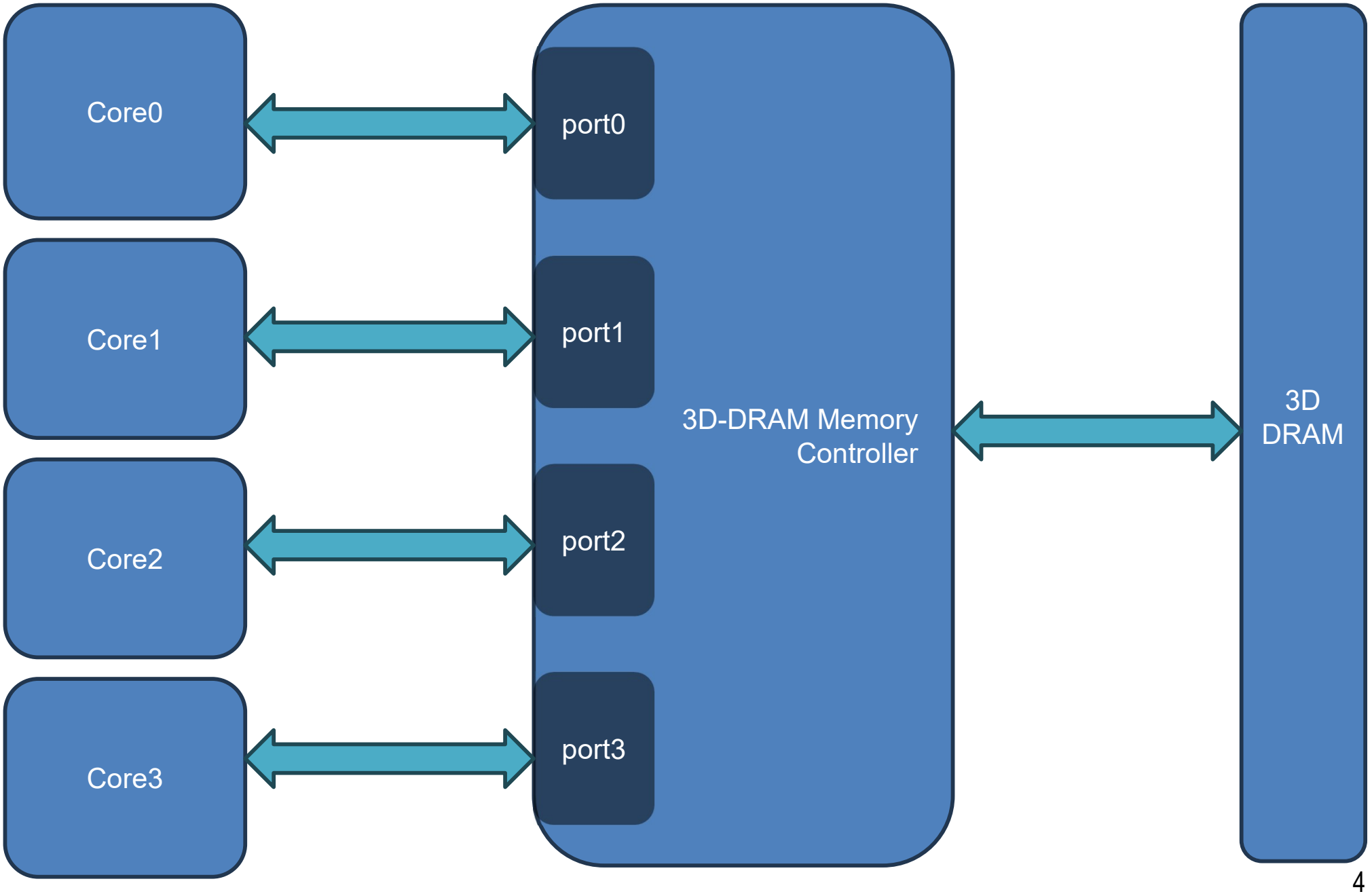
All row buffer hits Bandwidths

Assume 1Ghz, 1Gb bank	All row buffer hits Access
Average Latency	6.19 (ns)
Average Bandwidth	20.66 GB/s
Peak Bandwidth	21.5GB/s
Worst case Bandwidth	17.15GB/s
Total Average Bandwidth with 64 banks	1322.24GB/s

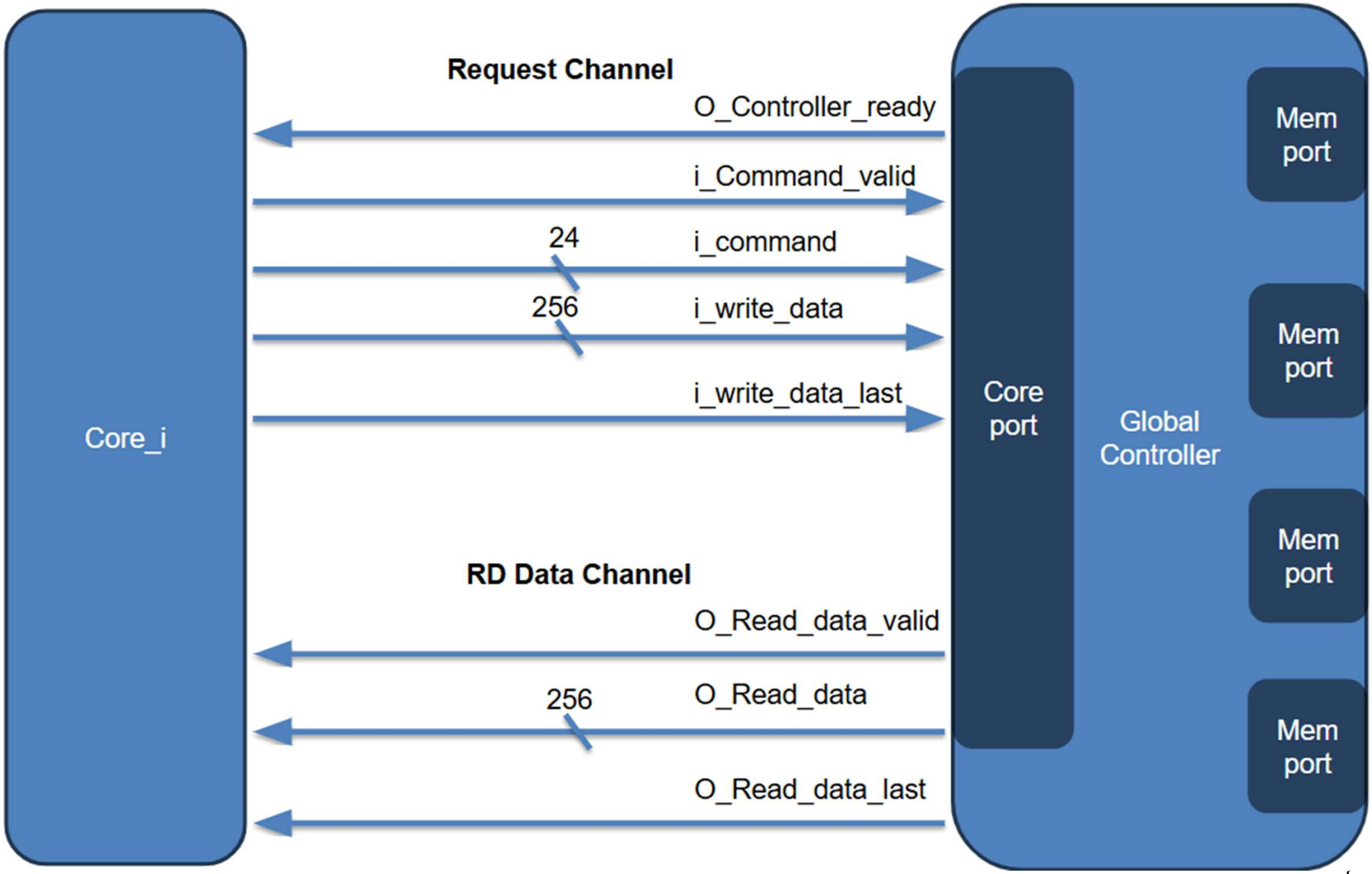
Refresh Timing Constraints	Durations
tREFI	3900ns
tRFC	110ns



3D-DRAM Memory Controller



3D-DRAM Memory Controller Interface

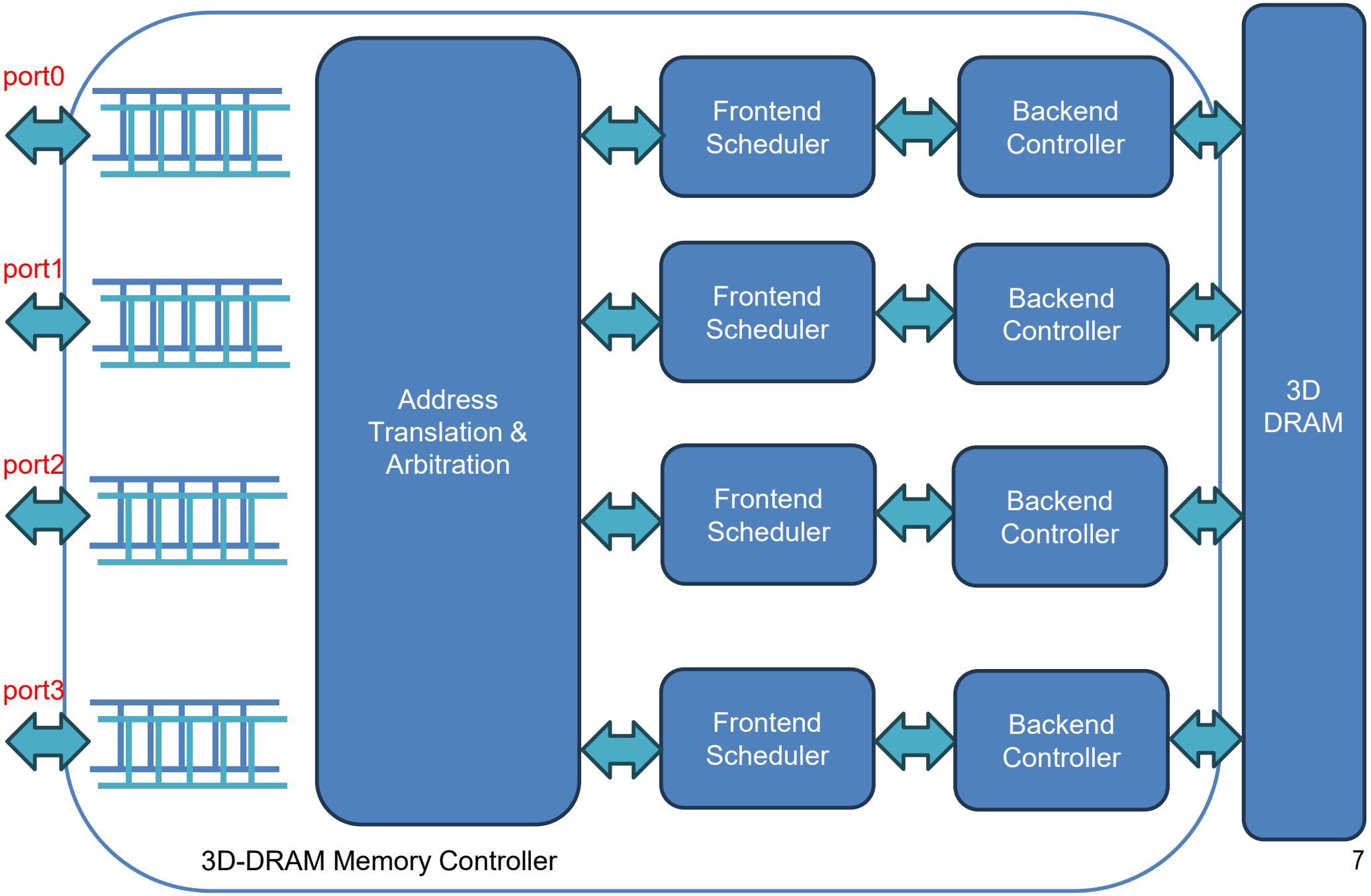


3D-DRAM Memory Controller Interface

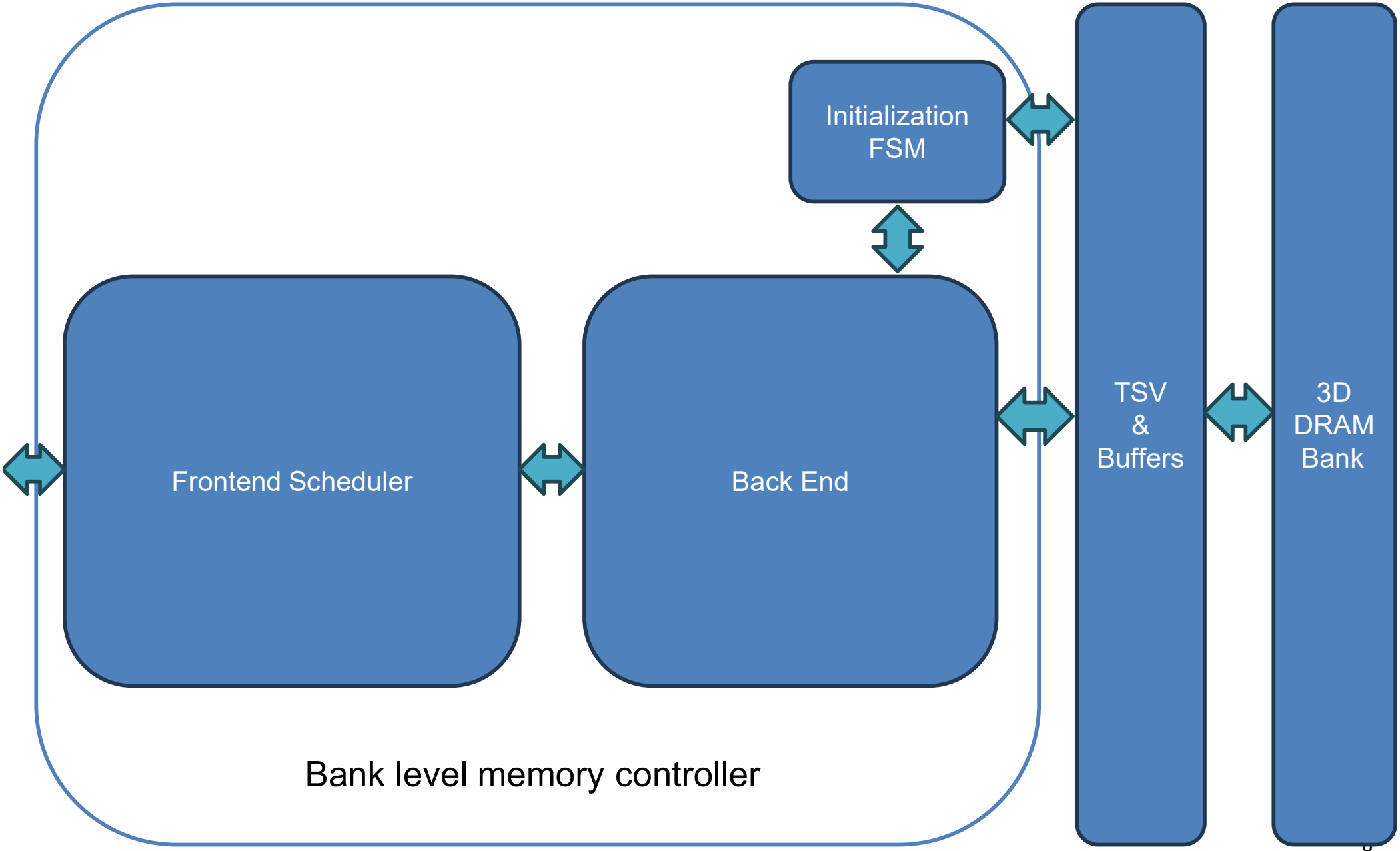
User DRAM subsystem access command					
Commands	R/W	Weights/KV $	Bank number	Row Addr	Column address
24bits	[24]	[23]	[21:20]	[19:4]	[3:0]
Description	Read or Write request	Type of requested data	The bank number to access	Access Row	Access Column

User DRAM memory controller interfaces			
Signal Name	Direction	Width	Description
power_rst_n	INPUT	1	Asychronous reset signal which resets the DRAM and the DRAM control, DRAM enter initialization mode start powering up after the assertion of the signal
clk1	INPUT	1	Main clock signal of 1GHz
clk2	INPUT	1	Secondary clock signal for sampling data of DRAM running at double the rate of clk1
Request Channel			
i_write_data_port0~3	INPUT	256	Write data only valid when request is a write command and the command is valid
i_write_data_last_port0~3	INPUT	1	Indicating the end of a write burst , 4 sequential write data to the same column address
i_command_valid_port0~3	INPUT	1	Indicating the command is valid
o_controller_ready_port0~3	OUTPUT	1	Indicating if the memory controller is ready to receive the command and data
i_command_port0~3	INPUT	24	Command signal for DRAM operations, for details please consults the Table
RD Data Channel			
o_read_data_valid_port0~3	OUTPUT	1	Read data valid signal, when asserted 1 the data on the o_read_data bus is valid
o_read_data_port0~3	OUTPUT	256	The read data from DRAM
o_read_data_last_port0~3	INPUT	1	Indicating the end of a write burst , 4 sequential write data to the same column address

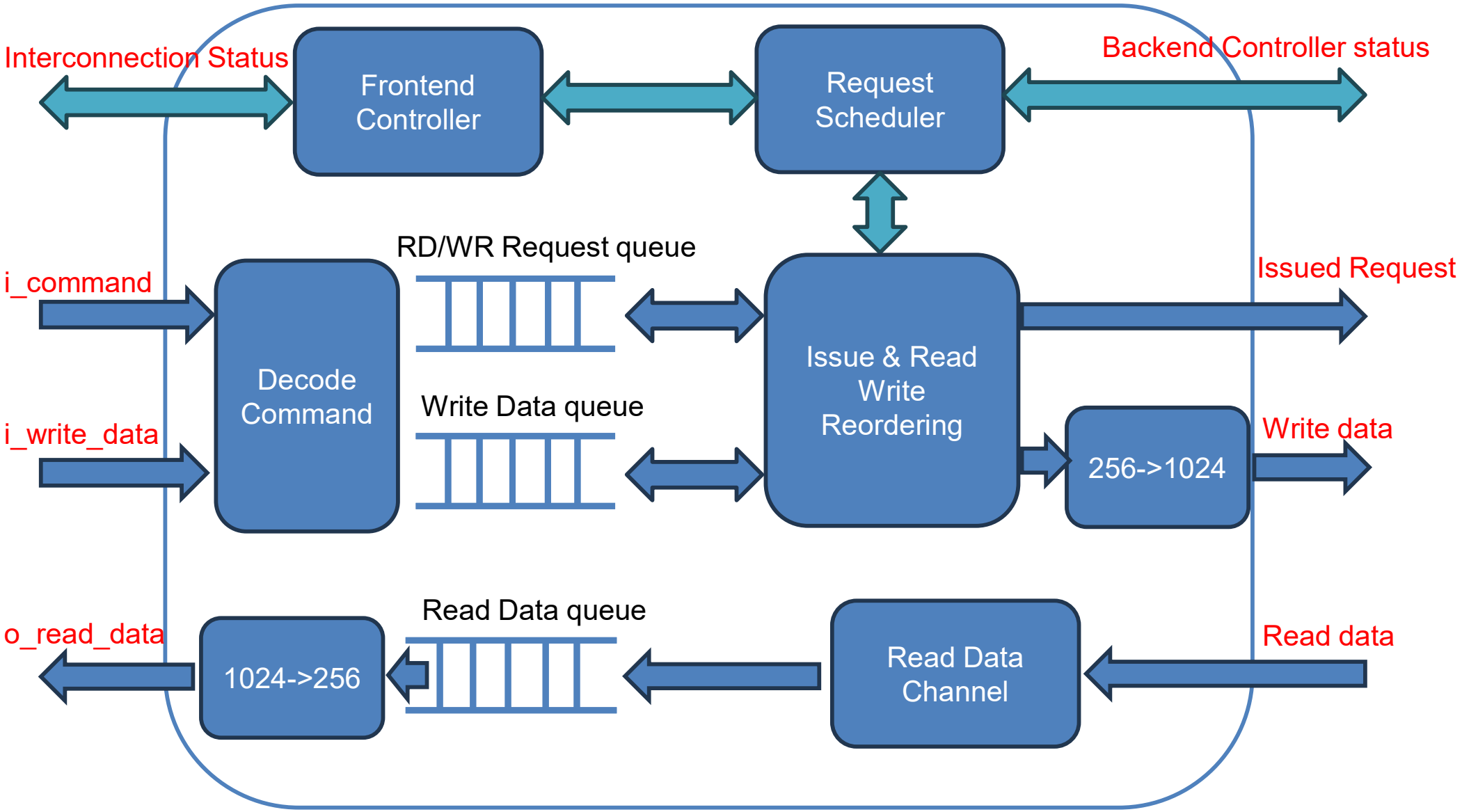
3D-DRAM Memory Controller



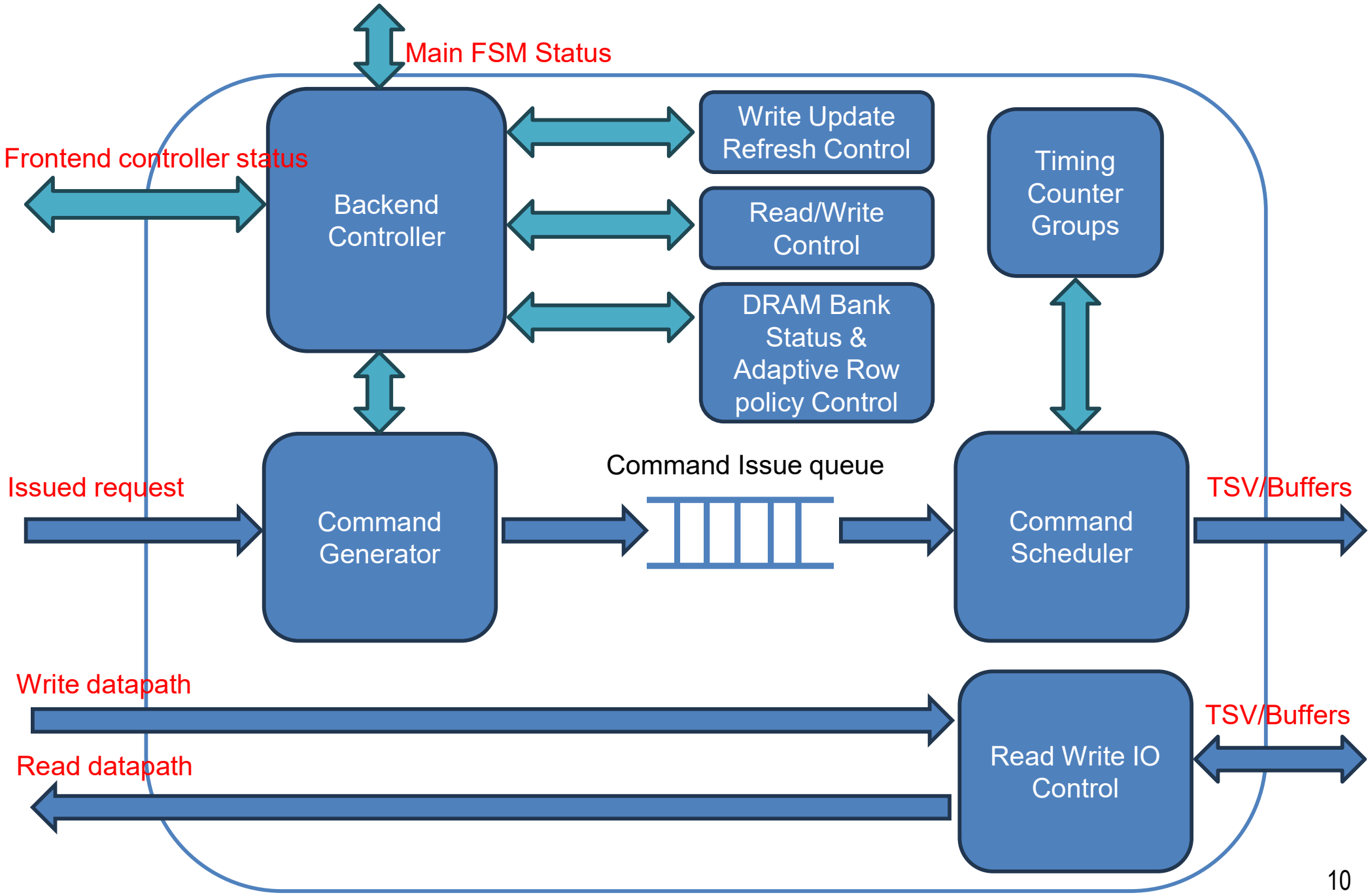
Bank Level Memory Controller



Frontend Scheduler



Backend Controller



Future Works

- Modify Senior's 3D-DRAM Verilog model to meet project's need
- Create a baseline bank level memory controller

References

- C. -Y. Chang, P. -T. Huang, Y. -C. Chen, T. -S. Chang and W. Hwang, "Thermal-aware memory management unit of 3D-stacked DRAM for 3D high definition (HD) video," *2014 27th IEEE International System-on-Chip Conference (SOCC)*

- Chang-Hsuan Chang, Ming-Hung Chang and Wei Hwang, "A flexible two-layer external memory management for H.264/AVC decoder," 2007 IEEE International SOC Conference, Hsinchu, Taiwan, 2007

- Design and implementation of DDR3 controller IP core and its verification, master thesis of Lanzhou Jiaotong University,王正宇,2012

- DDR3 controller design and research, master thesis of Fudan University,陆彦珩,2013

- D. Germchi, *A High Performance DDR4 Memory Controller on FPGA*, M.A.Sc. thesis, Dept. of Electrical and Computer Engineering, Univ. of Waterloo, Waterloo, ON, Canada, 2024.