

3/9/2021

Variant: [No Variations]

RELEASED TBD

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TOP VIEW

BOTTOM VIEW

DESIGN CONSIDERATIONS

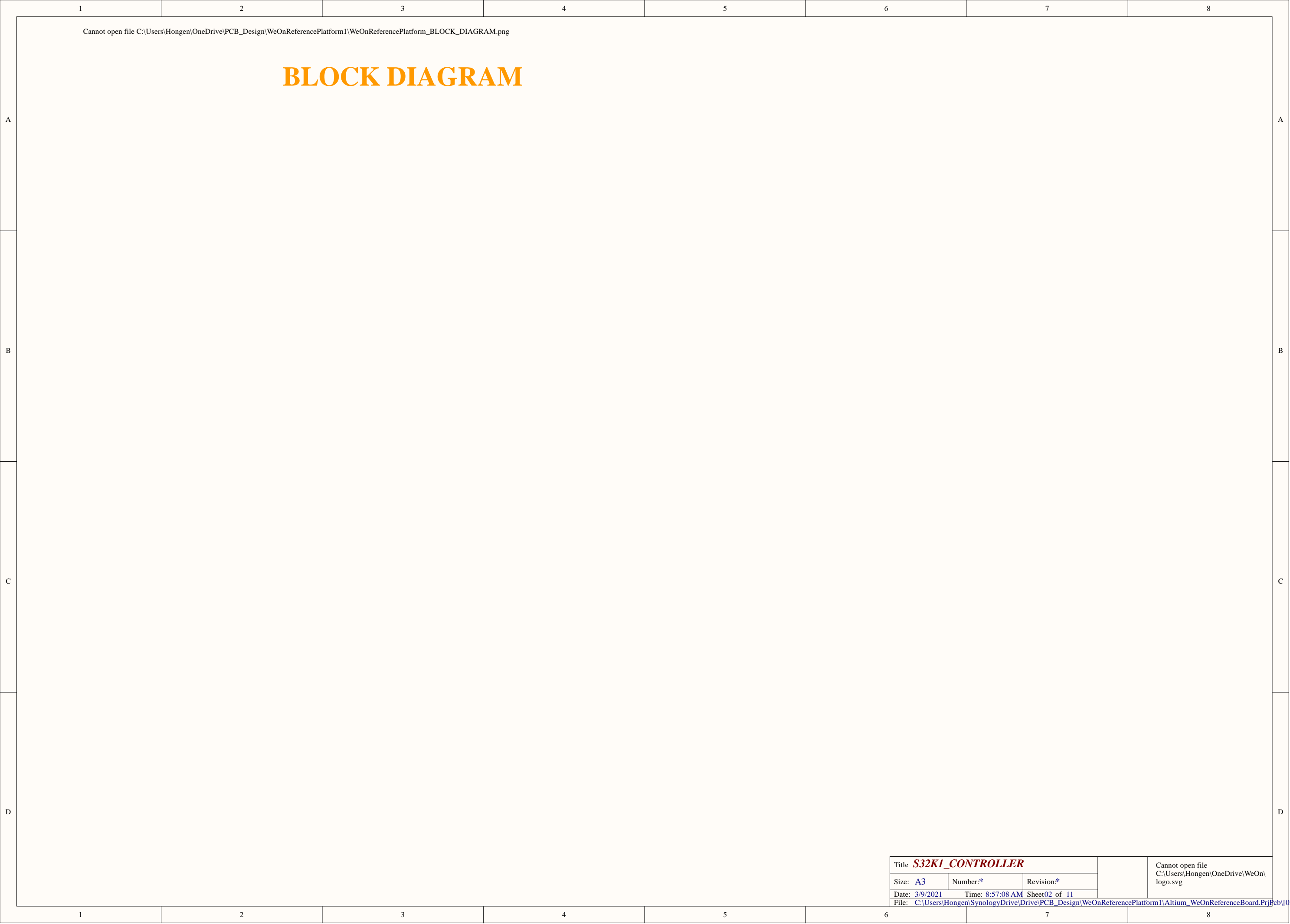
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Example text for informational
design notes.

DESIGN NOTE:
Example text for cautionary
design notes.

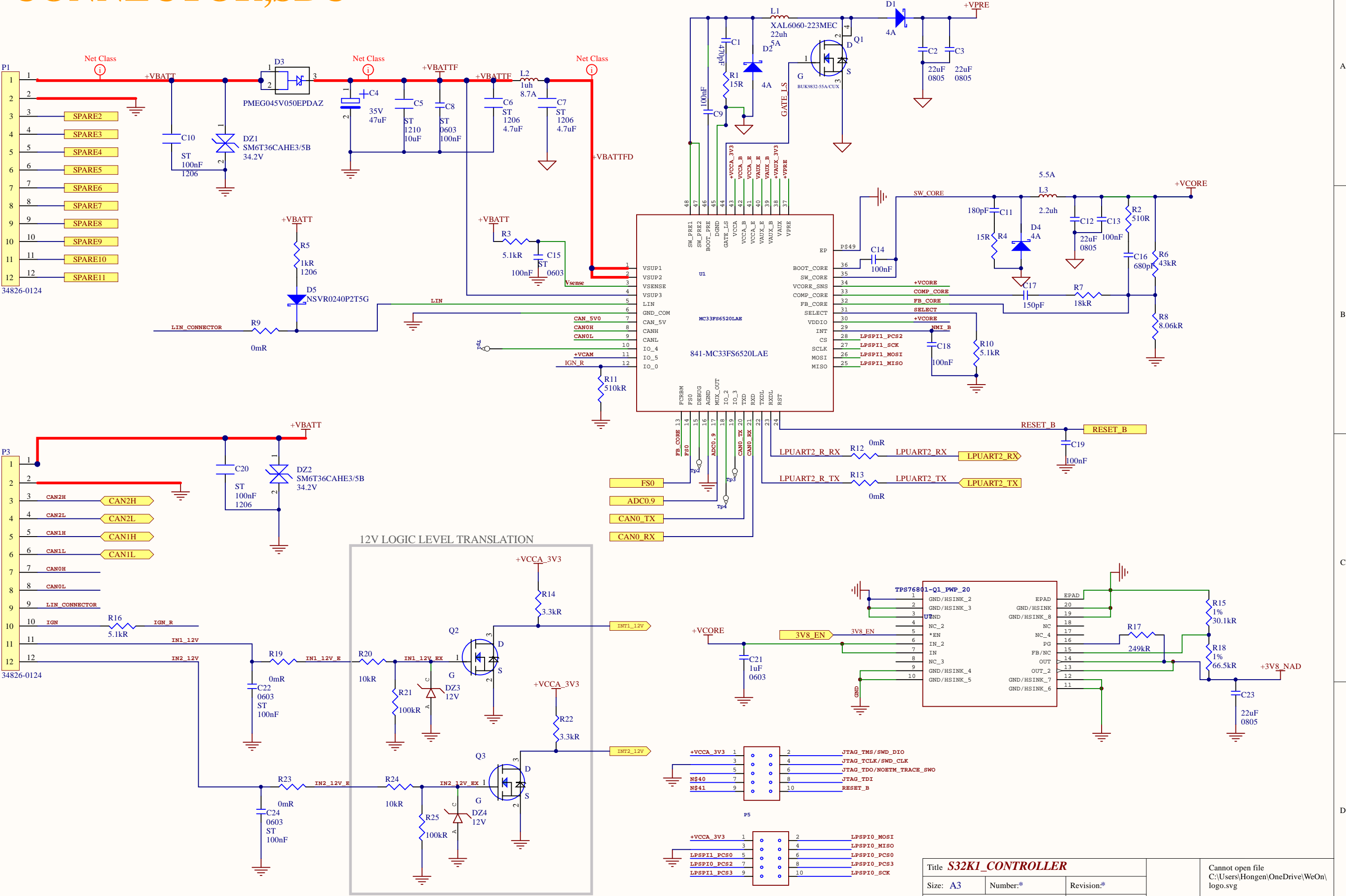
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Example text for debug notes.

DESIGN NOTE:
Example text for critical
design notes.

LAYOUT NOTE:
Example text for critical
layout guidelines.

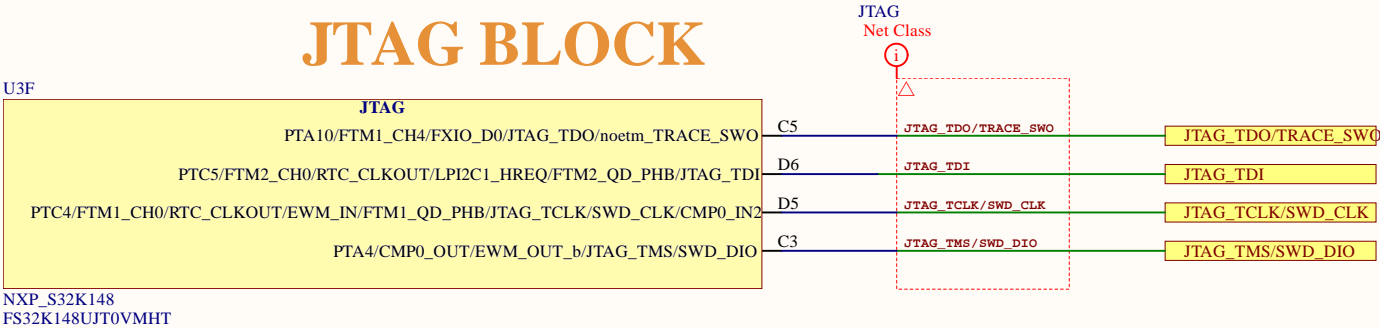


CONNECTOR,SBC

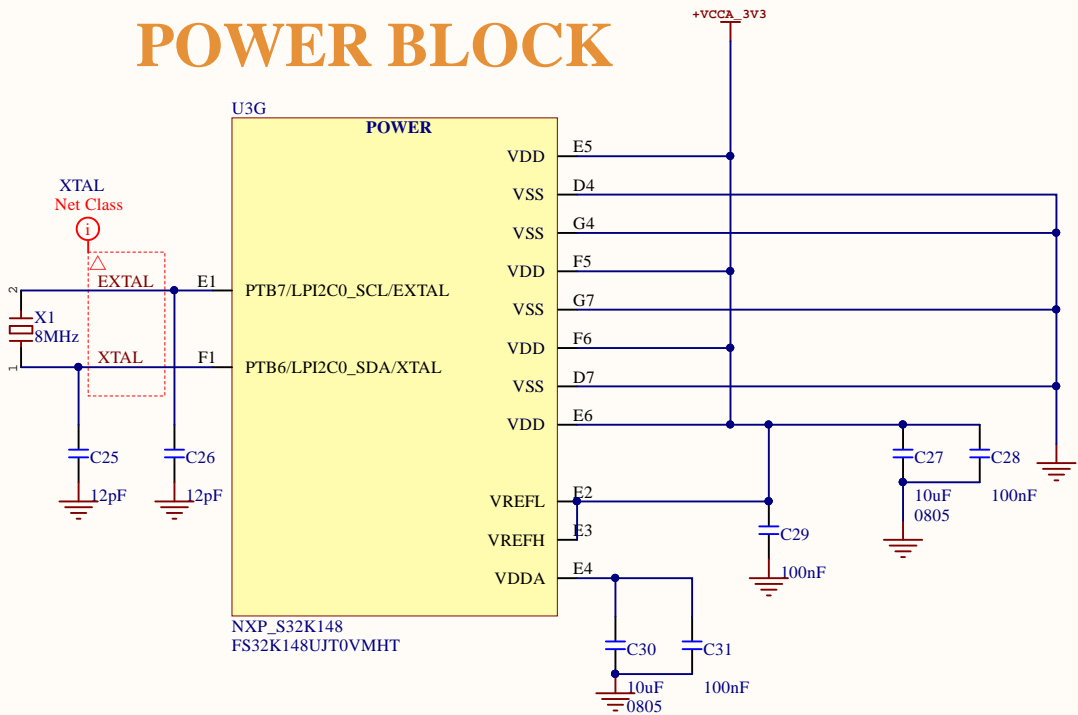


CPU-JTAG,POWER

JTAG BLOCK



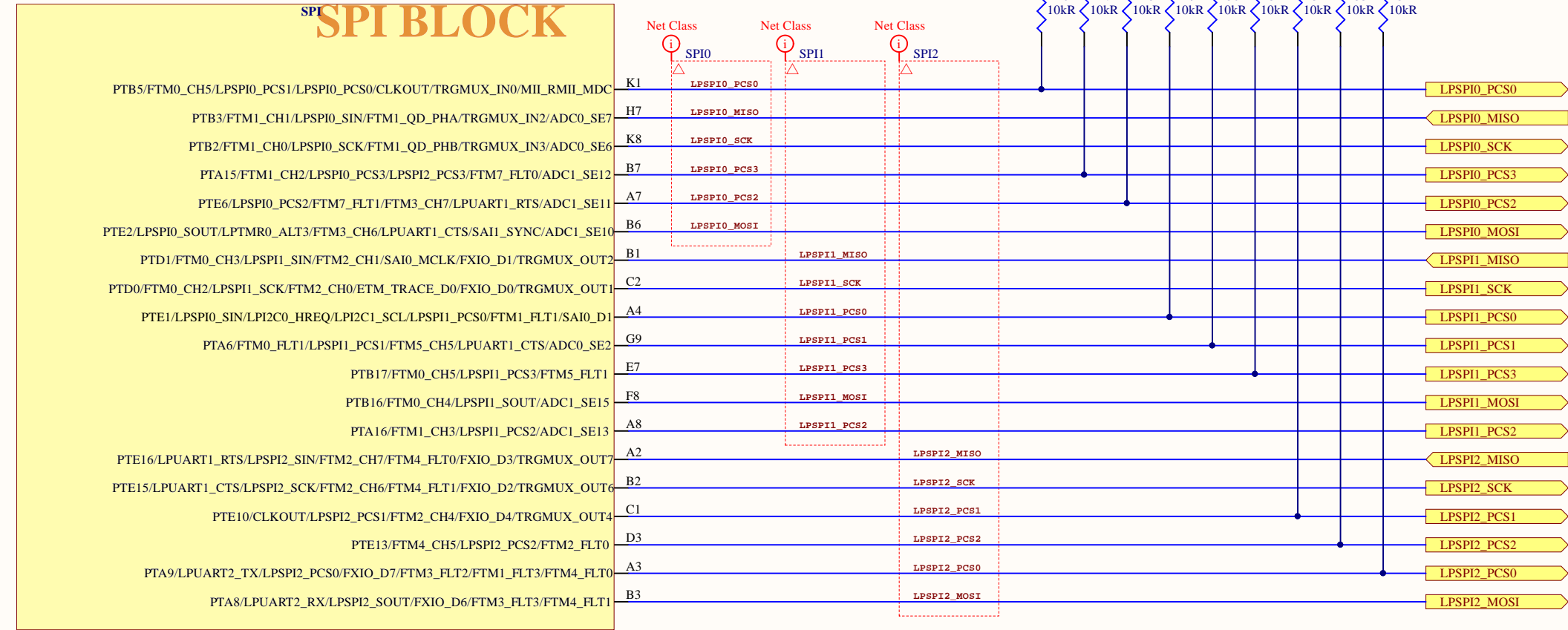
POWER BLOCK



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File: C:\Users\Hongen\SynologyDrive\Drive\PCB_Design\WeOnReferencePlatform1\Altium_WeOnReferenceBoard.PrjPcb\0			

CPU-UART,SPI

U3E

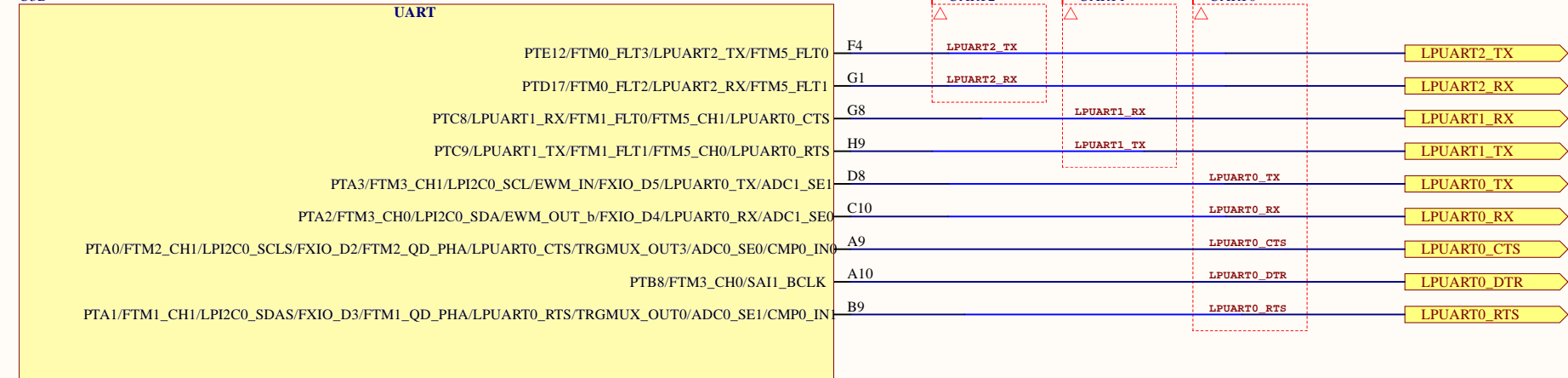


NXP_S32K148

FS32K148UJT0VMHT

UART BLOCK

U3D

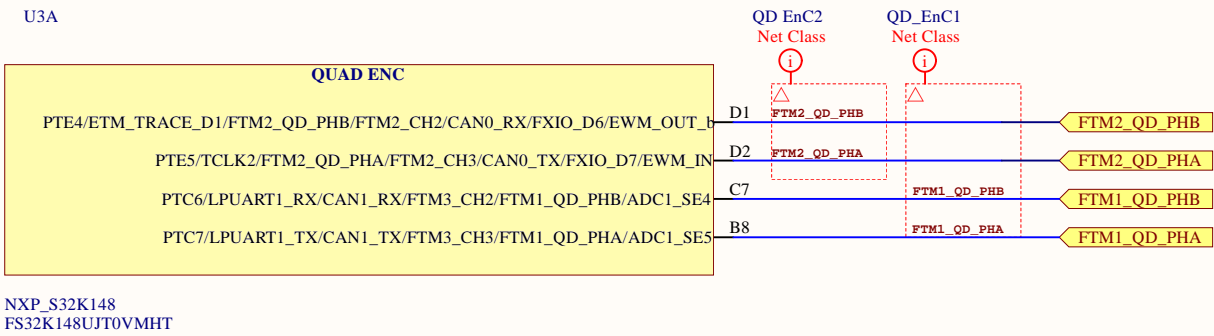
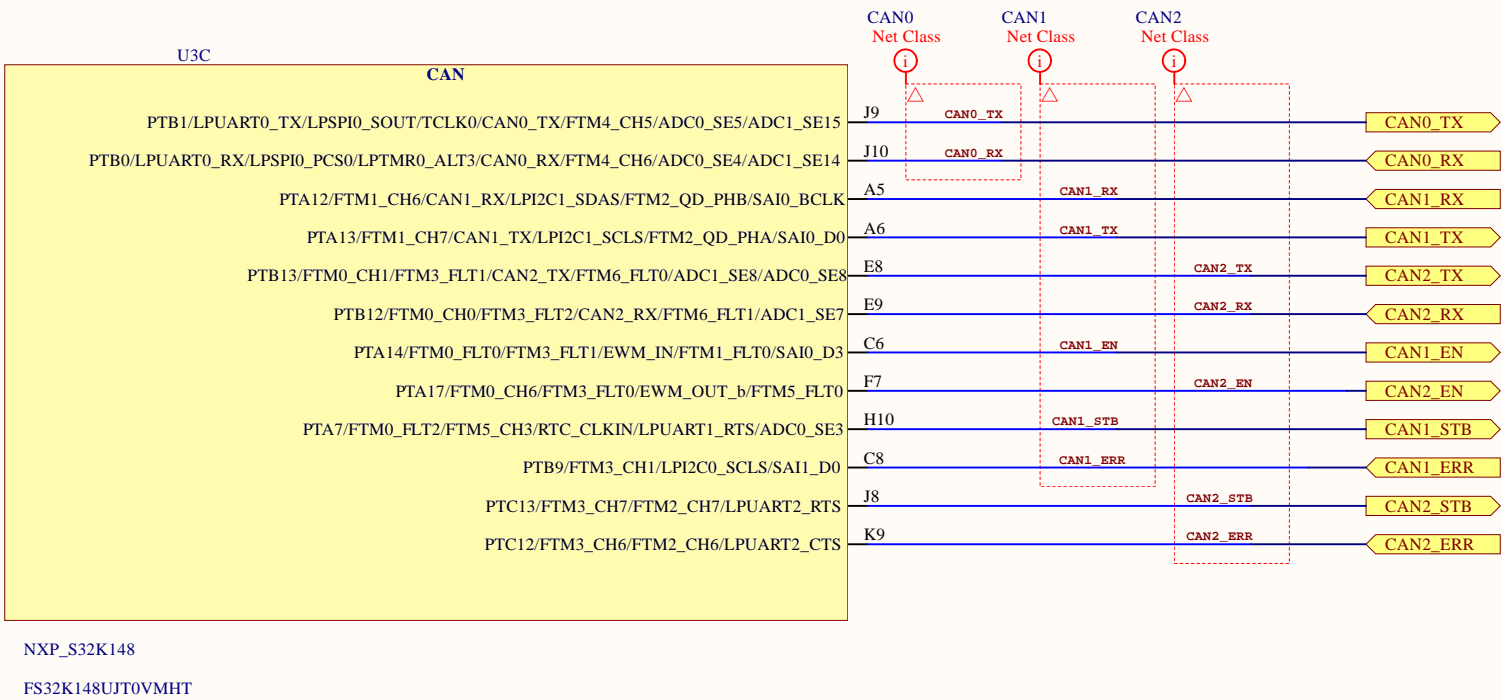


NXP_S32K148

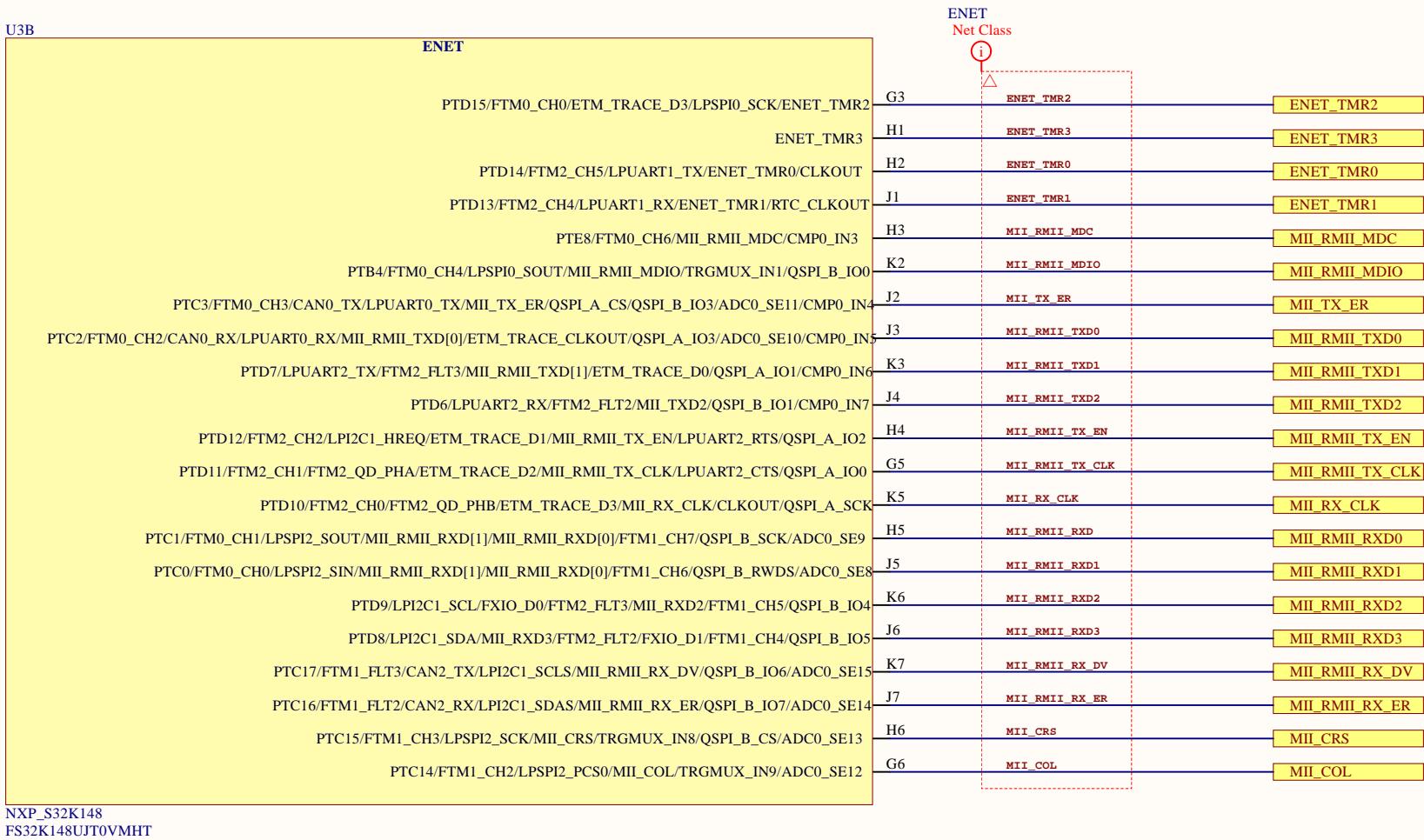
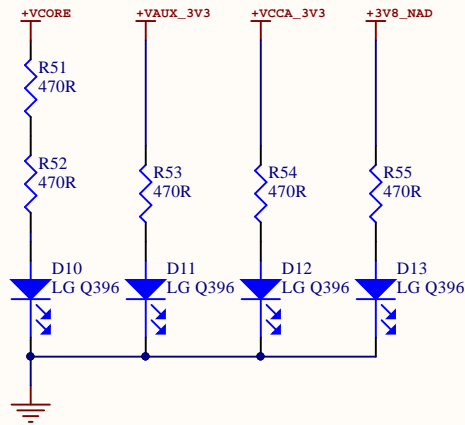
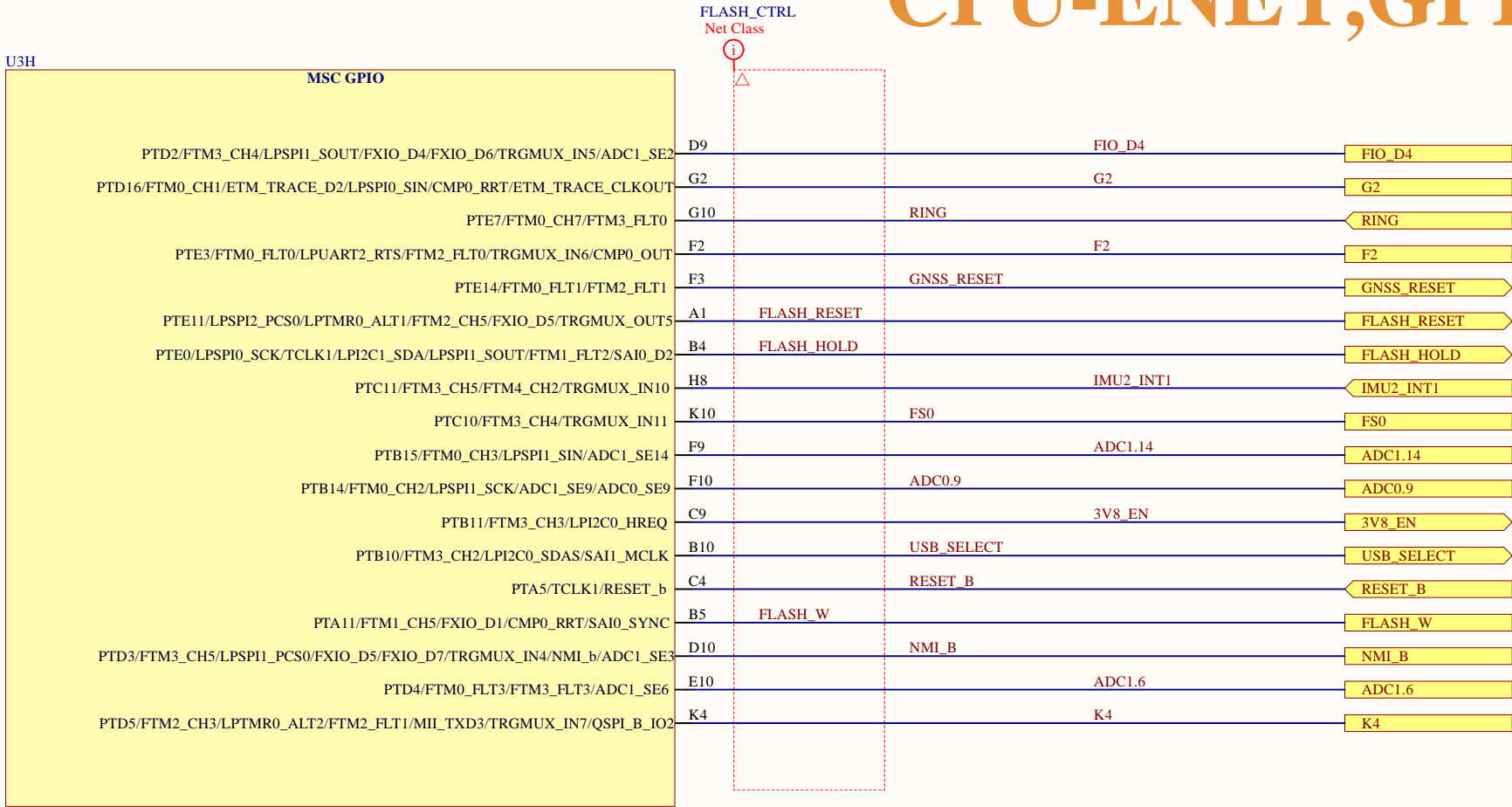
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CPU-CAN,QUAD_ENCODER

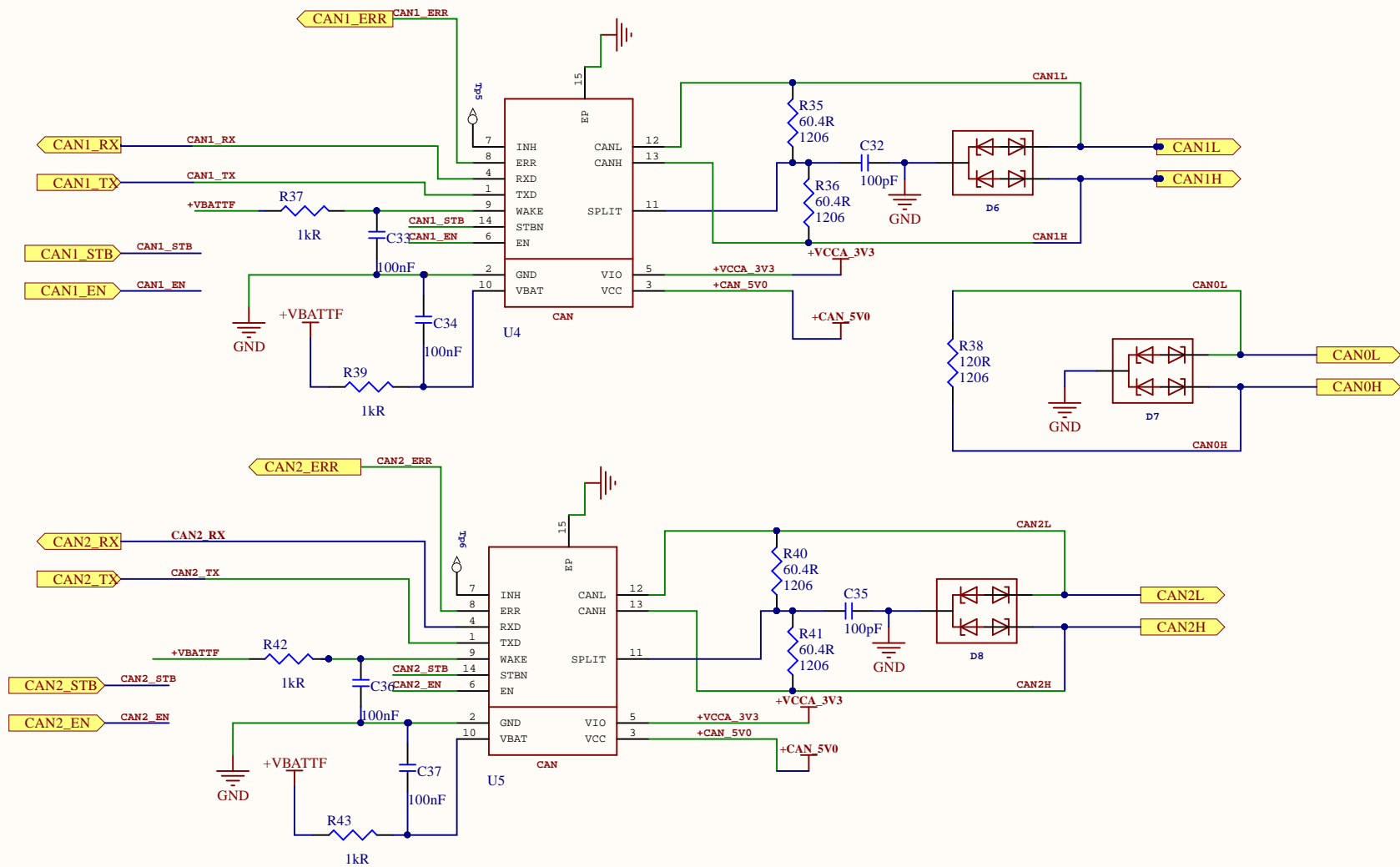


CPU-ENET,GPIO

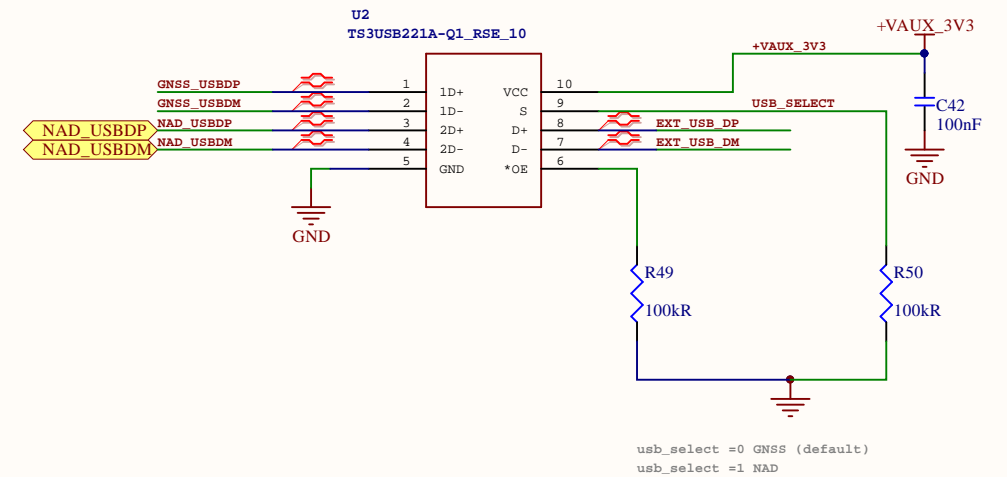
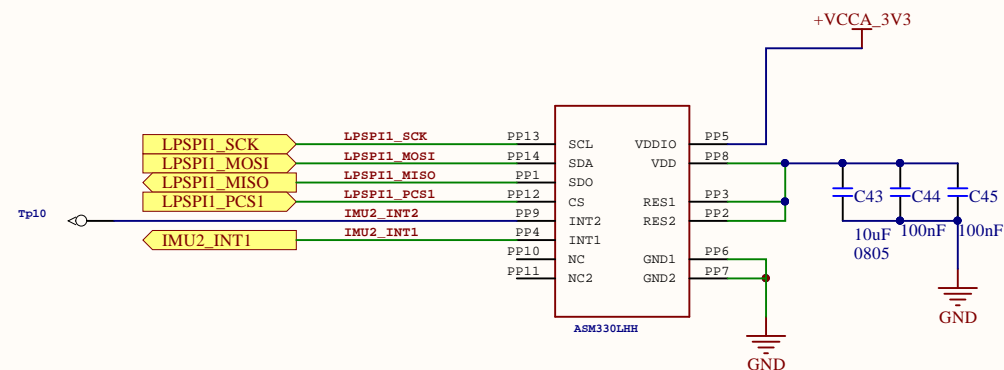
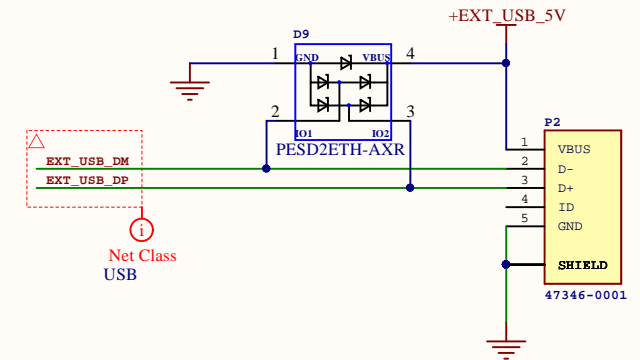
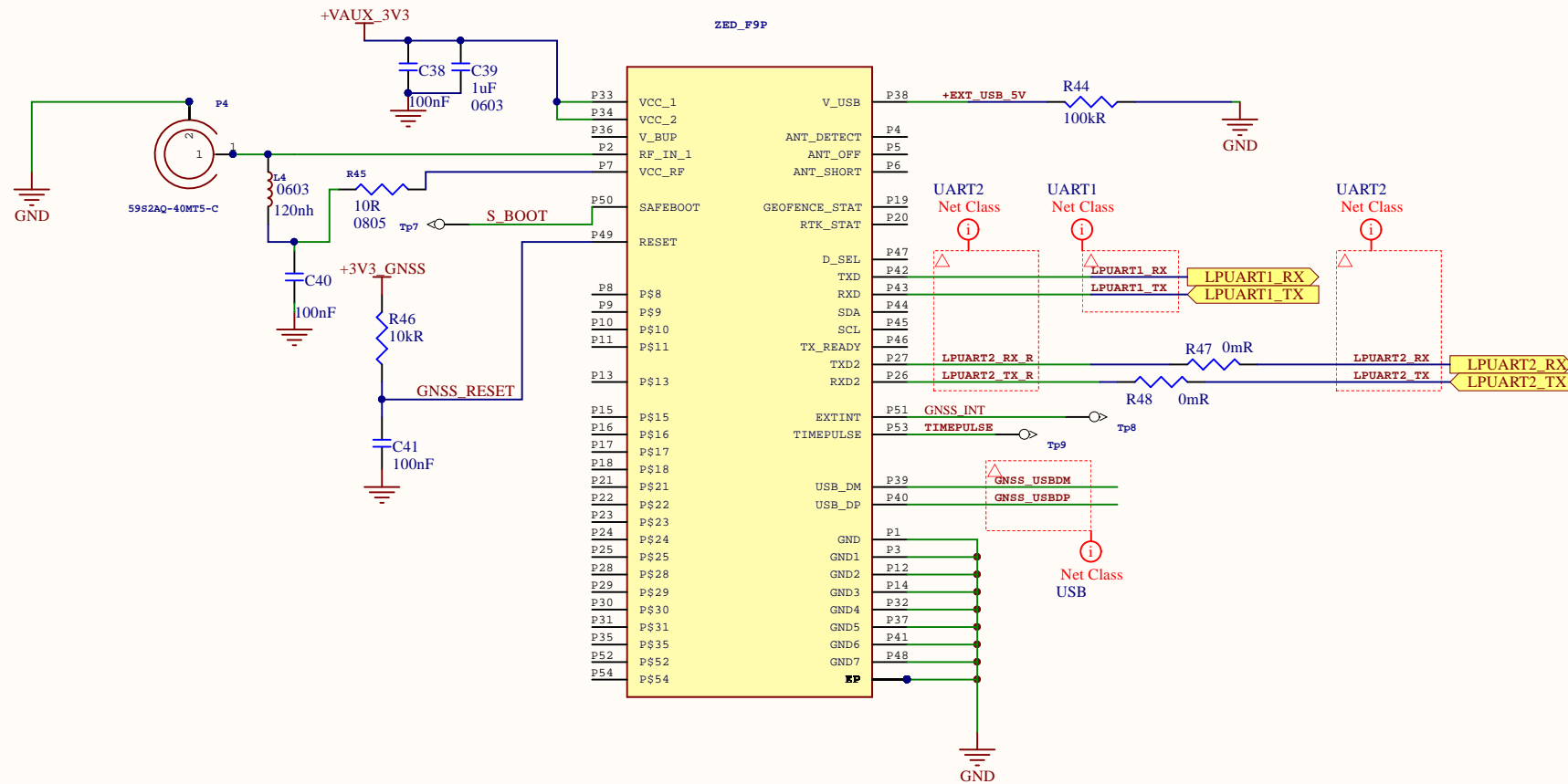


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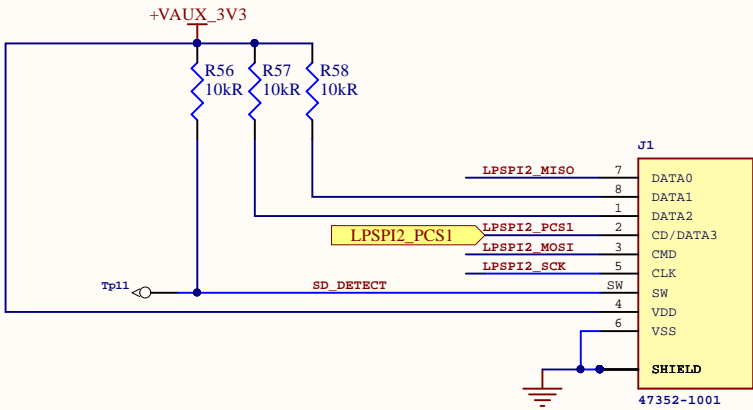
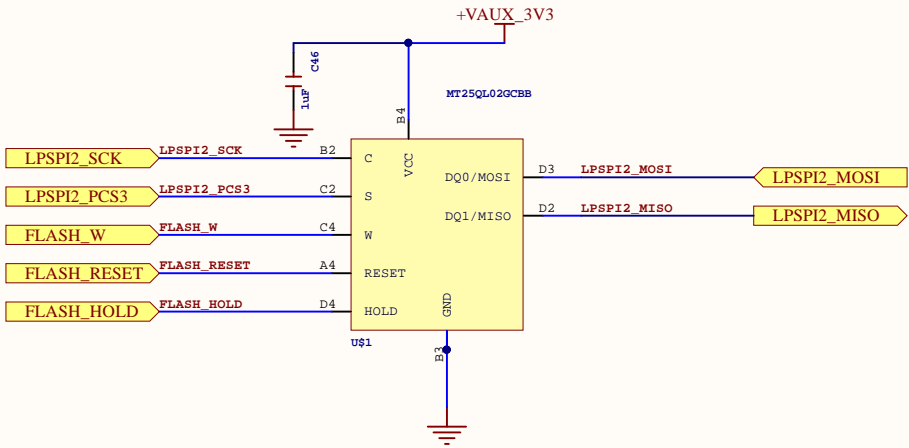
CPU-CAN TRANCEIVER



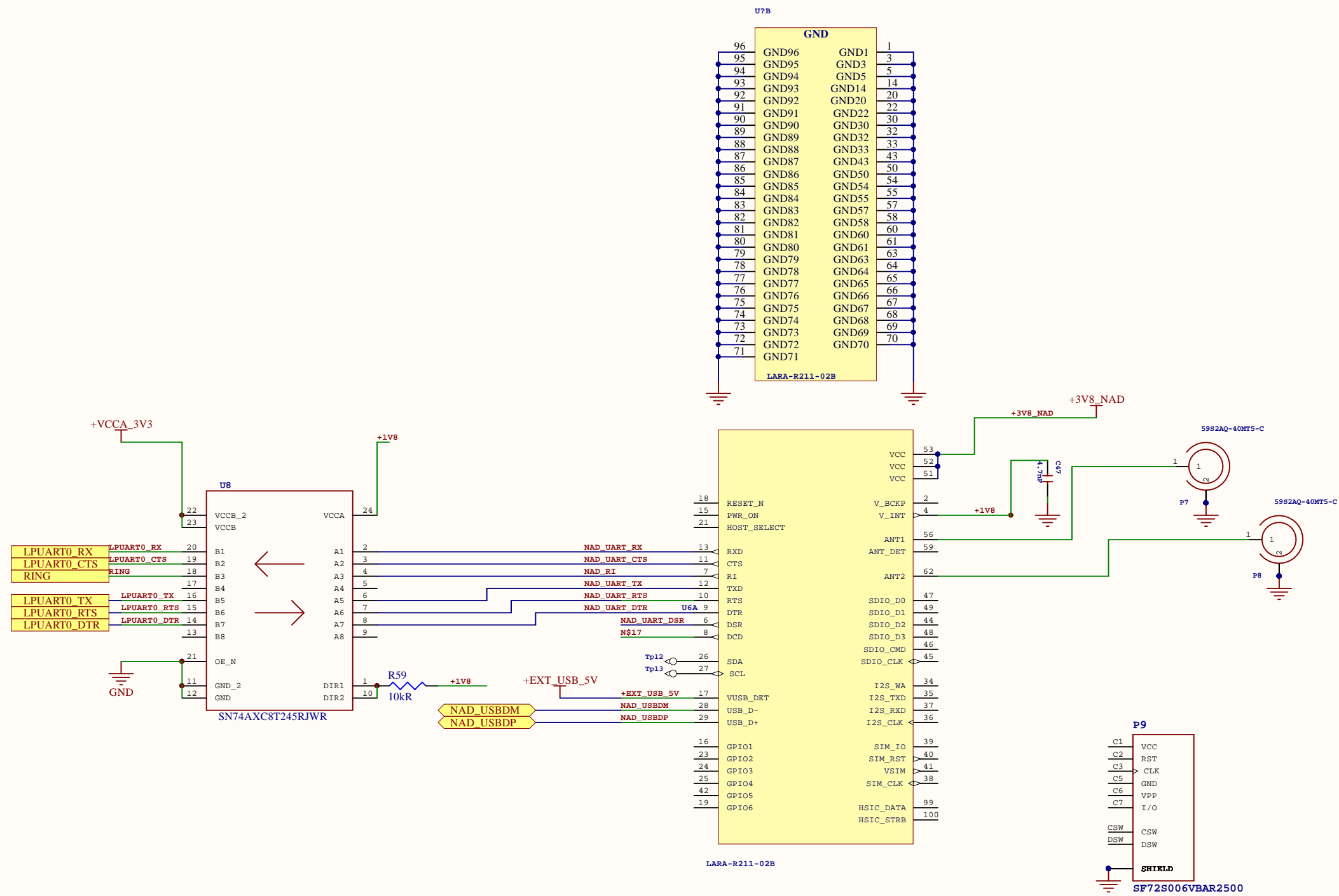
USB,IMU,GNSS



FLASH,SD



NAD



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