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Replace each AND gate in Figure 5-6 with an AND gate with one additional input and connect this input to the following: $S_1 + S_0$ This will force the outputs of all the AND gates to zero, and, on the next clock edge, the register will be cleared if S_1 is 0 and S_0 is logic one. Also, replace each direct shift input with this equation: $S_1 S_0$ This will...

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Digital Logic - Gates, Boolean Algebra - facstaff.bucknell.edu

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Digital Logic Design - University of California, Davis

Digital circuitry. Digital logic circuits can be broken down into two subcategories- combinational and sequential. Combinational logic changes "instantly"- the output of the circuit responds as soon as the input changes (with some delay, of course, since the propagation of the signal through the circuit elements takes a little time).

Digital Logic - learn.sparkfun.com

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