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CHAPTER 4 SOLUTIONS 9 effort should be about 4. This design has imbalanced delays and excessive efforts. The path effort is  $F = 12 * 6 * 9 = 648$ . The best number of stages is 4 or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of  $f = 648^{1/5} = 3.65$  each.

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