RegisteredMUX.Shetty.U74376412.USF.EE

The design has a register(D-f/f) connected to the output of the 4:1 Mux. The register is positive edge triggered and the output is 'Unassigned' until the first positive edge of clk.
Mux is combinatinal i.e output 'x' does not depend on clk and is driven based on 'sel'. A one bit register (Sequential) is driven by the clk and holds the Mux output value.
The cursor shows the difference between combinational output(x) and sequential output(y) with delay of 1/2 clk period (i.e delay until the positive edge of clk). Also there are no glitches in this design.