Computer Organization Lab 4

1. Describe the input fields of each pipeline register

Ans:

```
// IF/ID
wire [32-1:0] ID_PC_add1, ID_instr;

Pipe_Reg #(.size(64)) IF_ID(
.clk_i(clk_i),
.rst_n(rst_n),
.data_i({PC_add1, instr}),
.data_o({ID_PC_add1, ID_instr})
);
//

// ID/EX
wire [32-1:0] EX_PC_add1, EX_signextend, EX_ReadData1, EX_ReadData2;
wire EX_ALUSrc, EX_Branch, EX_MemRead, EX_MemWrite, EX_RegWrite;
wire [2-1:0] EX_ALUOP;
wire [21-1:0] EX_instr_20_0;
wire  EX_RegDst, EX_MemtoReg;

Pipe_Reg #(.size(158)) ID_EX(
.clk_i(clk_i),
.rst_n(rst_n),
.data_i({ID_PC_add1, signextend, ReadData1, ReadData2, ALUSrc, Branch,
MemRead, MemWrite, RegWrite,
MemtoReg, ALUOP, ID_instr[20:0], RegDst}),
.data_o({EX_PC_add1, EX_signextend, EX_ReadData1, EX_ReadData2,
EX_ALUSrc, EX_Branch,
EX_MemRead, EX_MemWrite, EX_RegWrite, EX_MemtoReg, EX_ALUOP,
EX_instr_20_0, EX_RegDst})
);
//
```

```
// EX/MEM
wire [5-1:0] MEM_WriteReg_addr;
wire [32-1:0] MEM_PC_add2, MEM_ALUResult, MEM_ReadData2;
wire MEM_Branch, MEM_zero, MEM_MemWrite, MEM_RegWrite,
MEM_MemRead,MEM_MemtoReg;

Pipe_Reg #(.size(107)) EX_MEM(
.clk_i(clk_i),
.rst_n(rst_n),
.data_i({WriteReg_addr, PC_add2, ALUResult, EX_ReadData2, EX_Branch, zero,
EX_MemWrite, EX_RegWrite, EX_MemRead, EX_MemtoReg}),
.data_o({MEM_WriteReg_addr, MEM_PC_add2, MEM_ALUResult,
MEM_ReadData2, MEM_Branch,
MEM_zero, MEM_MemWrite, MEM_RegWrite, MEM_MemRead, MEM_MemtoReg})
);
//

// MEM/WB
wire [5-1:0] WB_WriteReg_addr;
wire [32-1:0] WB_DM_ReadData, WB_ALUResult;
wire WB_RegWrite,WB_MemtoReg;

Pipe_Reg #(.size(71)) MEM_WB(
.clk_i(clk_i),
.rst_n(rst_n),
.data_i({MEM_WriteReg_addr, DM_ReadData, MEM_ALUResult, MEM_RegWrite,
MEM_MemtoReg}),
.data_o({WB_WriteReg_addr, WB_DM_ReadData, WB_ALUResult, WB_RegWrite,
WB_MemtoReg})
);
//
```

2. Explain your control signals in the sixth cycle(both test data test_1.txt and test_2.txt are needed)

Ans:

test1:

IF ID EX MEM WB

slt | or | and | addi | addi

RegDst : 1

ALUOP1 : 1

ALUOP0 : 0

ALUsrc : 0

Branch : 0

MemRead : 0

MemWrite : 0

RegWrite : 1

MemtoReg : 0

test2:

IF ID EX MEM WB

sw | sw | addi | addi | addi

RegDst : 1

ALUOP1 : 1

ALUOP0 : 0

ALUsrc : 0

Branch : 0

MemRead : 0

MemWrite : 0

RegWrite : 1

MemtoReg : 0