Introduction to Layout and Simulation

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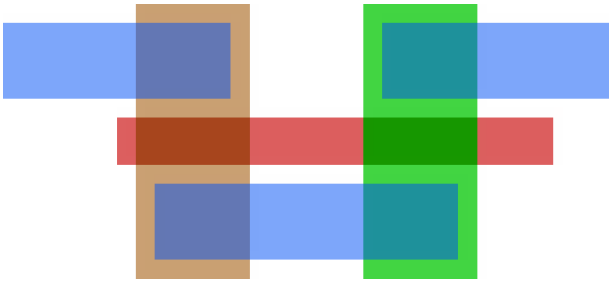
Summary

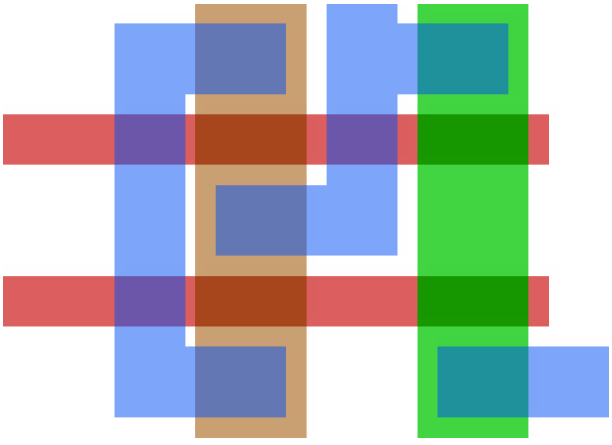
In this lab, we use Magic to implement and layout some basic gates including NOR, NAND and layouts for bigger gates. We attempted to minimize the area of each graph and make them logically as simple as possible.

0.1 Invertor



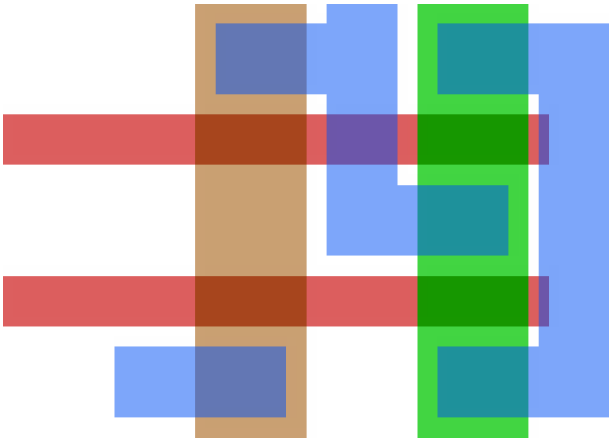
Bounding Box : 64 x 29 λ
Area : 1856 λ^2
Description: Simple gate and self explanatory with one strip of polysilicon between pdiff and ndiff material. Metal to connect the output.

0.2 NAND2



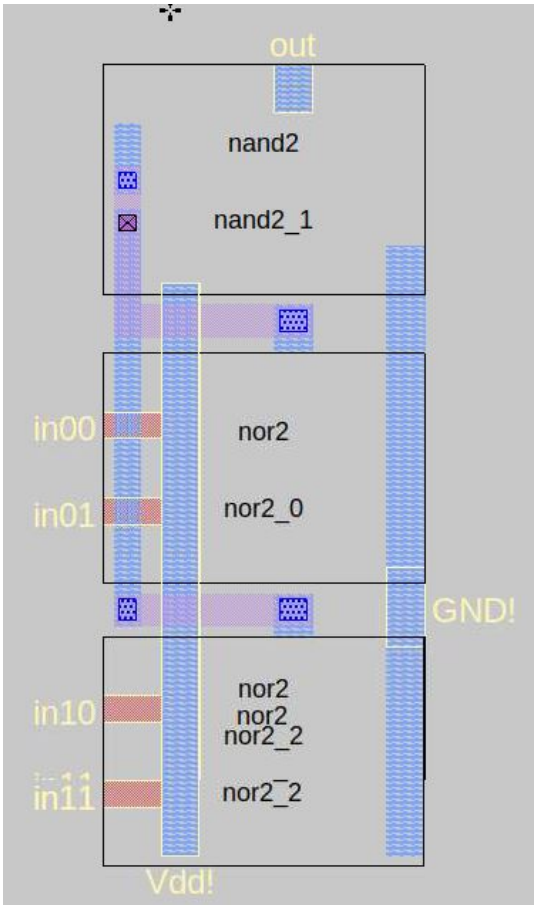
Bounding Box : 60 x 43 λ
Area : 2580 λ^2
Description: We designed the NAND2 with two strips of polysillicon, each with one strip of pdiff and ndiff perpendicular. The pull-up network is powered on the outside edges of the pdiff with the inside being the output. The pull-down network is simple sequential transistors.

0.3 NOR2



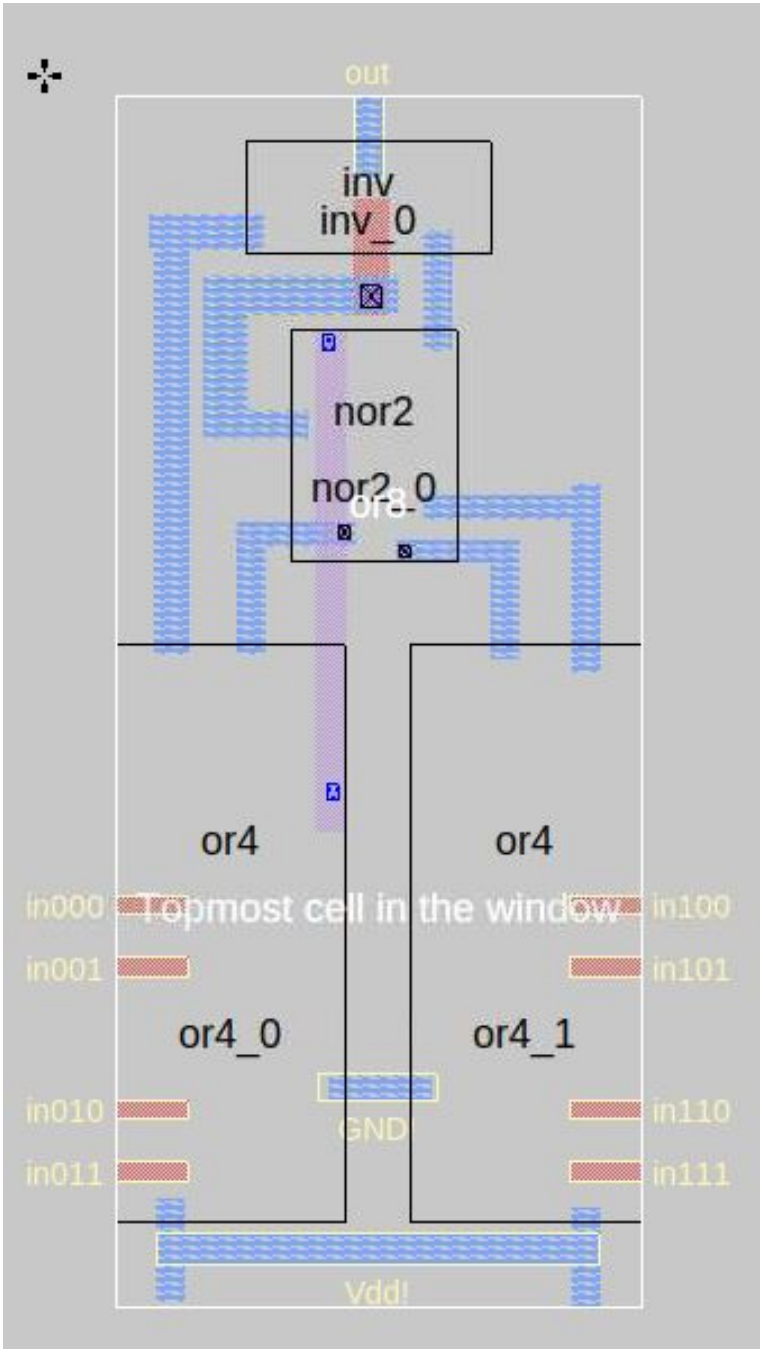
Bounding Box : 60 x 43 λ
Area : 2580 λ^2
Description: Pretty much sane as nand2 with the pull up and pull down network logic flipped. Pull-down ndiff contains an parallel transitors and pullup is a simple and sequential transistors.

0.4 OR4



Bounding Box : 60 x 150 λ
Area : 9000 λ^2
Description: Consists of two nor gates and one nand gate.

0.5 OR8



Bounding Box : 137 x 315 λ
Area : 43155 λ^2
Description: Consists of 2 or4 gates, that connect to an nor gate and then an invertor. Had issues with VDD and GND.