Lab 2: Introduction to VHDL

In this lab, you are asked to design and implement a combinational circuit on your BASYS 3 using VHDL. Combinational logic circuits are time-independent, memoryless circuits whose outputs solely depend on the *combination* of inputs.

You are asked to design a combinational circuit. This circuit can be a solution for a real-life problem. Draw the truth table (and include it in your report) and find the simplest equation that relates the outputs to inputs.

The Vivado & Basys References on Moodle will guide you on how to implement your design in VHDL using Vivado. Read the tutorials.

Research and try to answer the following questions in your report:

- How does one specify the inputs and outputs of a module in VHDL?
- How does one use a module inside another code/module? What does PORT MAP do?
- What is a constraint file? How does it relate your code to the pins on your FPGA?
- What is the purpose of writing a testbench?

1) Implement the circuit you designed in VHDL (Follow the tutorial). As this will be the only design source, this will automatically be the top module. Write a testbench code to simulate the inputs and display the output waveform (Follow the tutorial). Show this to your TA and get their approval. Include a screenshot of the waveform in your report. Also draw the RTL schematic in Vivado, and add a screenshot to your report.

2) You are also expected to demonstrate this circuit on your Basys 3 FPGA. You should use the switches as inputs and LEDs as outputs. For this purpose, create a constraint file. There is an example constraint (XDC) file on Moodle. Make sure that you comment the lines that you do not use, uncomment the ones that you do use, and make sure that the ports you specified here match those in your top module exactly in name. (You can comment lines by putting # in front). You can check which pin corresponds to which switch/LED/etc from the Basys 3 Reference Manual, which is also on Moodle. Program your device. Once your device is working, show it to your TA and get their approval. In your report, include example photos of your working FPGA.

Do not forget to add all the code that you have written to your report (except for the constraints).