

## Lab 4: Arithmetic Logic Unit

The purpose of the lab is to build an Arithmetic Logic Unit (ALU). An ALU is a combinational circuit that can perform mathematical operations and is an essential building block for most digital devices ([https://en.wikipedia.org/wiki/Arithmetic\\_logic\\_unit](https://en.wikipedia.org/wiki/Arithmetic_logic_unit)).

- 1) Design an ALU. It should have **eight** functions: **addition**, **subtraction**, and six others of your choice including at least **one bitwise** and **one shift** operation (Check the list on the Wikipedia page). Implement it in VHDL in a modular fashion. Simulate your modules and put the **simulation results** in your report. Generate an **RTL schematic** and explain it briefly in your report. Deploy your ALU on your **FPGA** and display the outputs through LEDs. Show your schematics and working FPGA to your TA to get their approval. Include representative photos of your FPGA in your report.

Do not use operators from libraries. Implement your operations yourself. (Hint: You can first design a one-bit adder and then use this component for implementing other operations)