Lab 6: Greatest Common Divisor

The purpose of this lab is to design a circuit that calculates the greatest common divisor (GCD) of two 8-bit numbers. There are multiple ways to calculate the GCD of two binary numbers. You can choose one and implement it.

In this lab, you are allowed to reuse the code that you have written in the Arithmetic Logic Unit lab. If you have lost your code or do not want to adapt, you can also use code from other resources **by properly citing them**. In either case, **please do not include recycled/borrowed codes in your report.**

Study the document "VHDL Registers and Counters" on Moodle and make sure that you know how to implement registers in VHDL. Check the example codes therein. The critical point in this lab is to properly use registers, and decide when and how to load them.

Design a module that calculates the GCD of two 8-bit numbers. This module should start calculating with a start signal from a button, and when the calculation is done, it should indicate the result via an output signal.

(Hint: You may have two registers for the inputs, and one for the output. As long as the start button is pressed, load into the input registers from the inputs, and reset your output. When the button is not pressed, start doing your calculation on these registers.)

Demonstrate this module on your FPGA. Take 8-bit numbers from **switches**, the start signal from a **button**; and display the result on the **LEDs**. Show a few working examples to your TA and get their approval. Include photos in your report.

For your report, run a testbench simulation using inputs 140 and 12. How many clock cycles does the calculation take from the start signal till the end?

In your report, clearly explain your design, show your results, and try to answer the following questions:

- What was your algorithm to calculate the GCD?
- Is your module a combinational circuit or an FSM? If the latter, is it a Moore machine or a Mealy machine? Would it be cheaper to implement GCD as a combinational circuit or as an FSM? Would it be faster? What are the drawbacks in each case?
- How many clock cycles did it take in your simulation to calculate the GCD? Do you think this can be optimized? How so?