EEE 202 - Lab 5 Report - Band Pass Filter

Design a band-pass filter with given specifications for 50Ω load resistance.

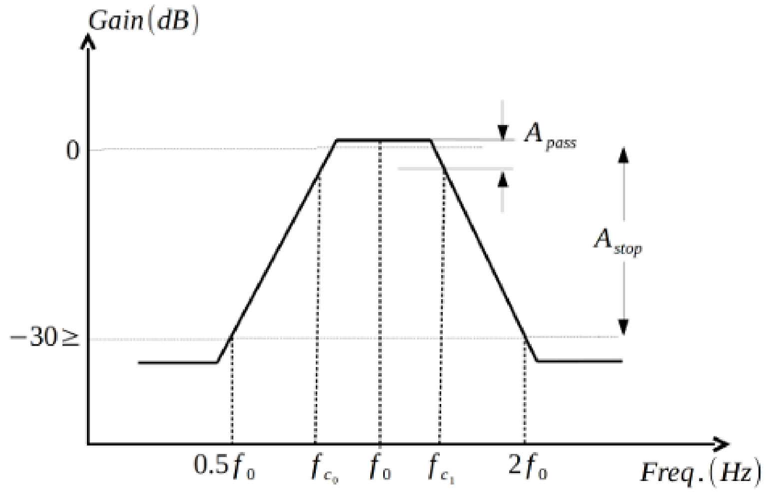

Figure 1: Frequency response of the filter

Central frequency: $2Mhz \leq f_0 \leq 5Mhz$
Passband width: $f_{c_1} - f_{c_0} = 0.05f_0$
Gain variation in the passband: $A_{pass} \leq 3dB$
Stopband attenuation: $A_{stop} \geq 30dB$

Introduction:

In this lab, we are asked to build a band-pass filter with the given specifications. This can be achieved using a variety of design methods. I chose to implement the filter using a “Butterworth Filter” as it is completely passive.

Theory:

Butterworth filters are designed according to the following steps.

1. First find the desired order of the filter.

The required order of a filter can be found according to the formula given as:

$$H(\omega) = \frac{P_L}{P_A} = \frac{1}{1+(f_0/\Delta f)^{2n}+(f/f_0-f_0/f)^{2n}}$$

Plugging in the frequencies and the desired power delivery we get the value for the required order.

$$20log_{10}(\frac{1}{1+0.05^{2n}+2.5^{2n}}) <- 30dB$$

Note that this is the gain at $0.5f_0$. The value of n is found to be approximately 1.867. The minimum integer value for the order is found to be 2 from this formula.

2. Find the values for the required components.

The values for the capacitors and inductors are found from the formula provided below.

$$C_i = \frac{a_i}{2\pi R\Delta f} \quad \text{and} \quad L_i = \frac{Ra_i}{2\pi\Delta f}$$

where a_i's are the butterworth numbers.

n	b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
1	2.000							
2	1.4142	1.4142						
3	1.0000	2.0000	1.0000					
4	0.7654	1.8478	1.8478	0.7654				
5	0.6180	1.6180	2.0000	1.6180	0.6180			
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176		
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450	
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902

Figure 1: Butterworth numbers.

From these formulas the values for the components are 25.72nF and 64.307μH.

3. Add a parallel inductor to shunt capacitors and a series capacitor to serial inductors.

The added components should be designed to resonate with their counterpart at the center frequency. The required values for these components are found to be 80.39nH and 32.15pF.

Software:

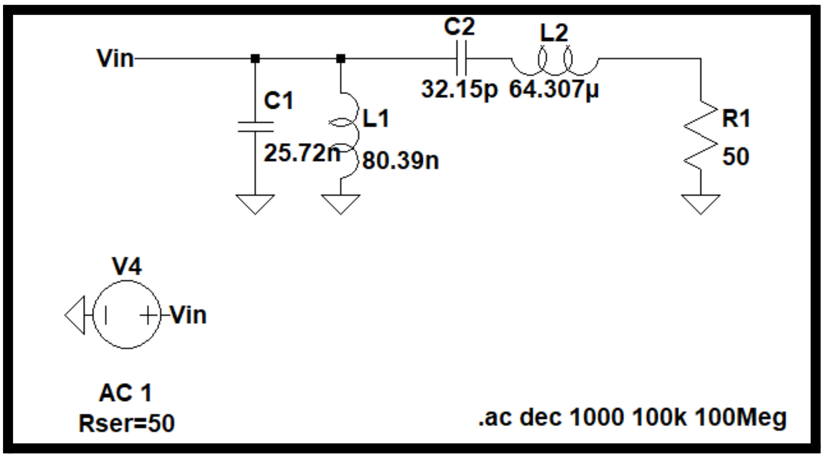

Figure 2.1: LTSpice Schematic

The circuit was designed with the values from the theory section and has the following transfer function. -6dB is the maximum value since the source has a 50Ω series resistance. This causes the circuit to act as a voltage divider at the center frequency. $2V_{out} = V_{in}$ hence -6dB

The bandwidth is supposed to be 175KHz since $\Delta f = 0.05 f_0$

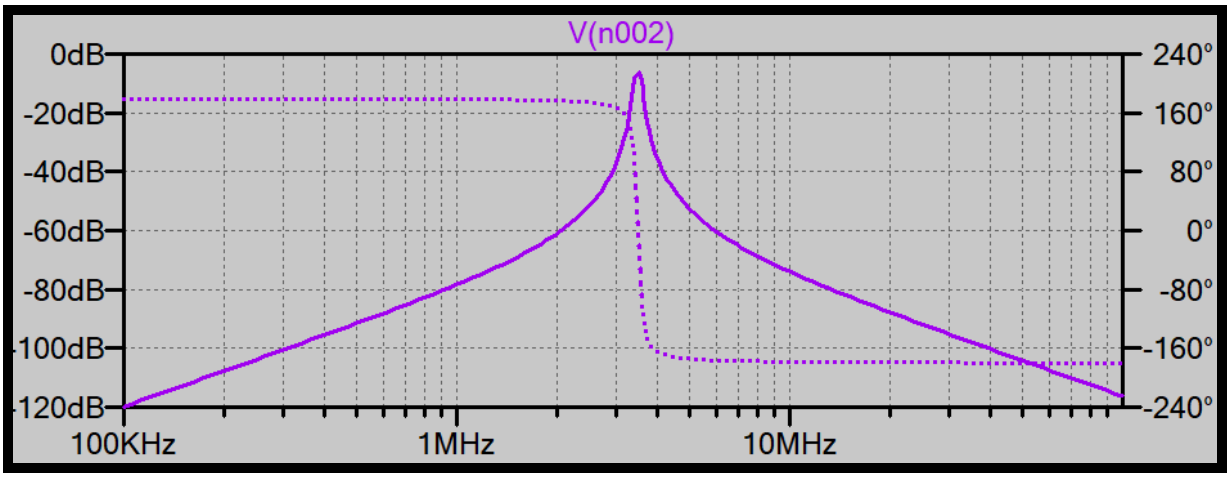

Figure 2.2: Bode plot of the transfer function.

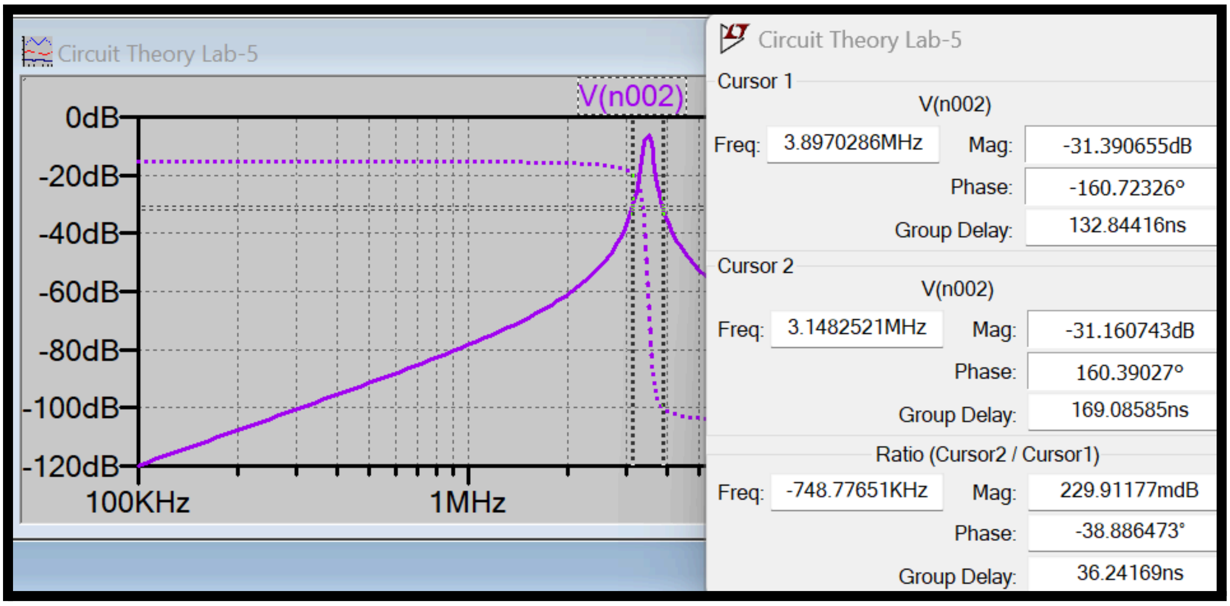

Figure 2.3: -30dB

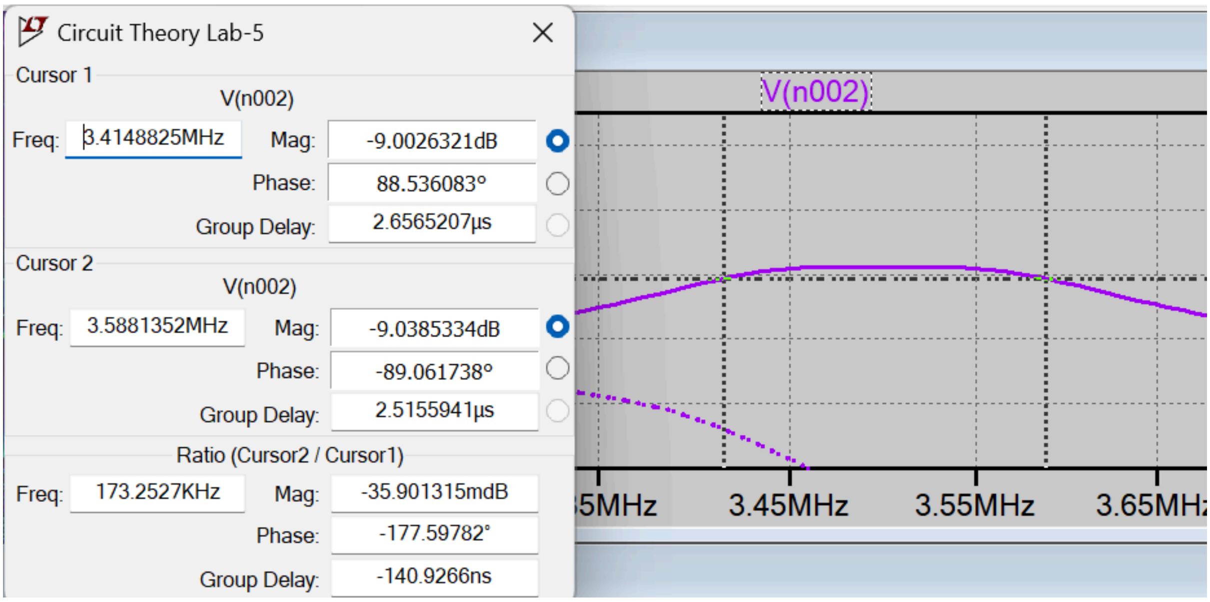

Figure 2.4: Bandwidth

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Hardware:

The same circuit was implemented for the hardware part with the output provided below:

Figure 3.1: Hardware implementation of the circuit

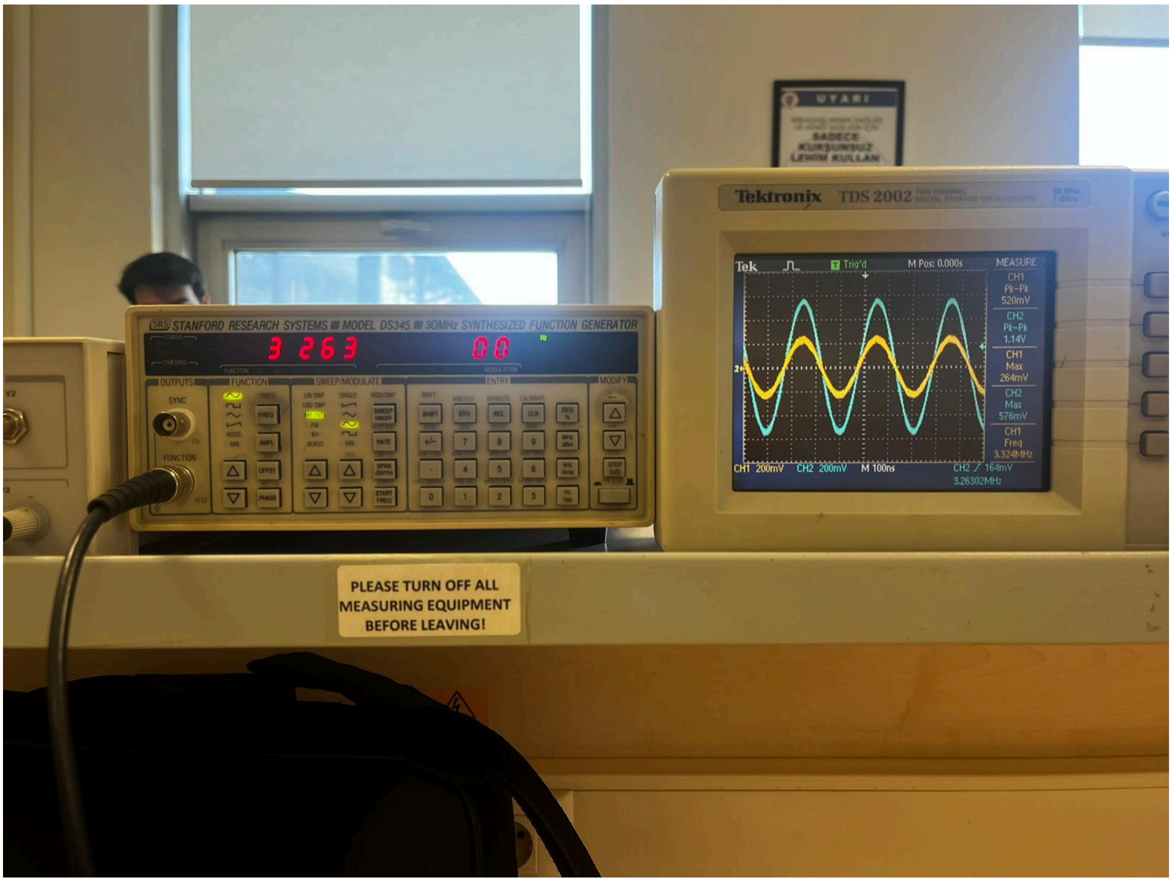

Figure 3.2: Output of the filter.

$20log(0.5) \ = \ -6dB$ for the provided value.

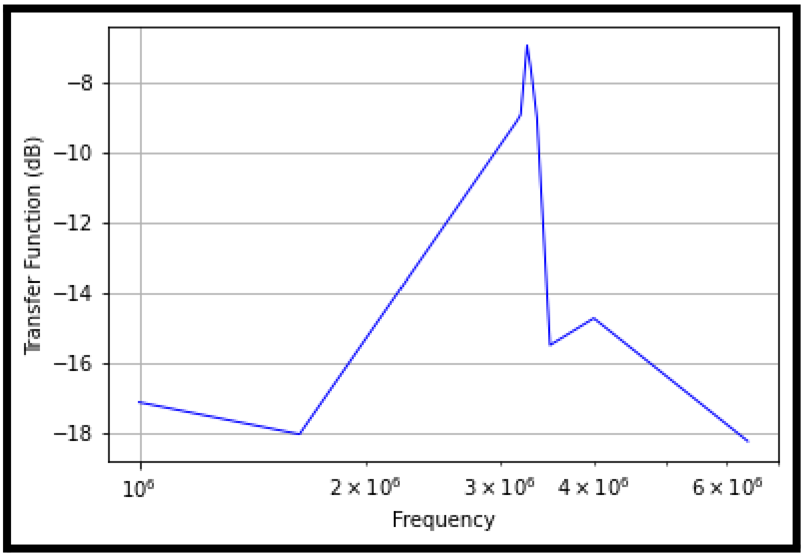

Figure 3.3: Bode plot of the transfer function

Freq	Vout	Vin	Vout/Vin	H(w)
1000000	0.02	0.144	0.138889	-17.1466
1632000	0.035	0.28	0.125	-18.0618
3163000	0.504	1.44	0.35	-9.11864
3200000	0.472	1.32	0.357576	-8.93264
3263000	0.512	1.14	0.449123	-6.9527
3300000	0.5	1.2	0.416667	-7.60422
3363000	0.334	0.944	0.353814	-9.02451
3500000	0.12	0.716	0.167598	-15.5146
4000000	0.074	0.404	0.183168	-14.743
6400000	0.032	0.262	0.122137	-18.263

Table 1: Values from hardware implementation

Conclusion:

In conclusion, we designed a second-order butterworth bandpass filter. We used the formula to find the desired order of the filter and then calculated the values for the components required. We then used these values in LTSpice to simulate the filter. We later implemented the filter during our hardware lab. Comparing our values from the software and hardware, center frequency gain was -6dB and -6.9dB in software and hardware respectively. Our error for center frequency gain was 15%.

References:

Atalar. A, Köymen.H, Analog Electronics. [Acessed: May 5,2024]