

EEE 202 Lab 3 Report - Waveform Generator

Design a circuit that generates the voltage waveform shown in Figure 1. The design should be based on OPAMPS and RC circuits.

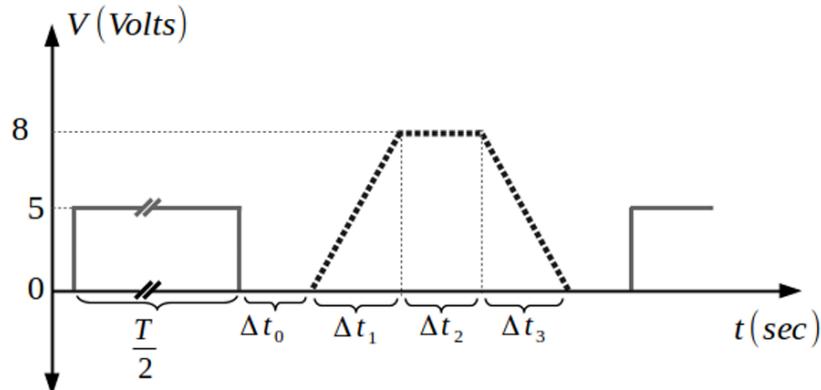


Figure 1: **Input** (solid gray line) is a square pulse. One period of the **output** is shown by dashed lines.

$$\Delta t_0 = 2ms, \Delta t_1 = 2ms, \Delta t_2 = 3ms, \Delta t_3 = 2ms$$

$$\text{Input peak voltage: } 5V$$

$$\text{Output peak voltage: } 8V$$

$$\text{Input frequency: } f < 50Hz, T = \frac{1}{f}$$

Introduction:

In this lab, we are asked to generate a waveform with the specifications given above.

Theory:

In order to get the desired output. A circuit composed of three main sections is utilised. First, a RC-delay section to get the desired time differences.

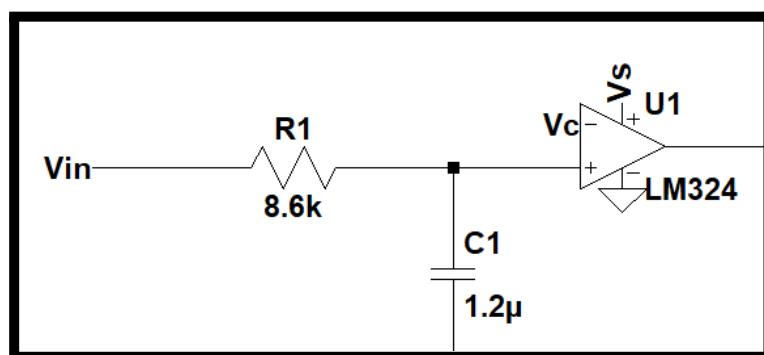


Figure 1: RC-delay Circuit

The RC-delay circuit is implemented in order to get two waveforms shifted 1.3 ms and 6.3 ms each. It achieves this delay by comparing the voltage of an RC circuit with a pre-determined voltage. So we need to reach the decided voltage(2.5V) at the desired times.

$$5V - 4.6e^{-\frac{t}{RC}} = 2.5$$

The RC value can be calculated to be 0.0021 and 0.0103 for the 1.3ms and 6.3 delays respectively.

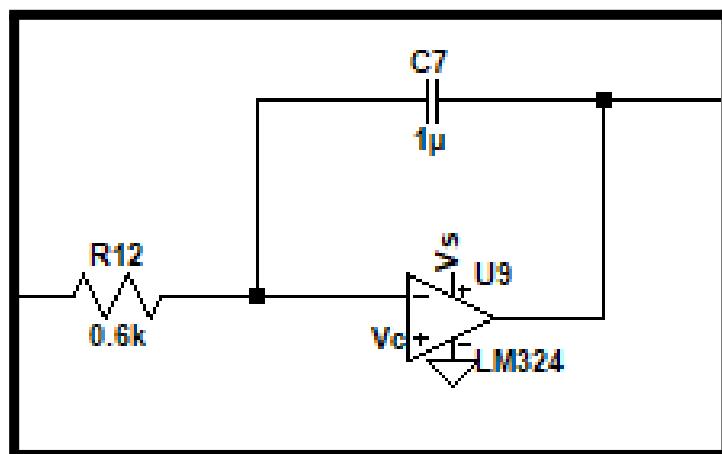


Figure 2: Integrator Circuit

The integrator circuit is required to integrate the RC-delay outputs. The integrated waveform of the RC-delay outputs will be a triangular wave, which we need for the rising and falling edges of the waveform. The RC value of the integrator will determine the slope of the triangular output. The calculations for the RC value are as follows.

$$Slope = \frac{\Delta V}{\Delta t} = \frac{8V}{2ms} = 4 \cdot 10^3$$

$$\frac{V_{in} - V_{comp}}{R} + \frac{d(V_{comp} - V_c)}{dt} C = 0$$

$$V_c = \frac{1}{RC} 5t$$

$$\frac{1}{RC} 2.5 = 4 \cdot 10^3$$

$$RC = 0.0006$$

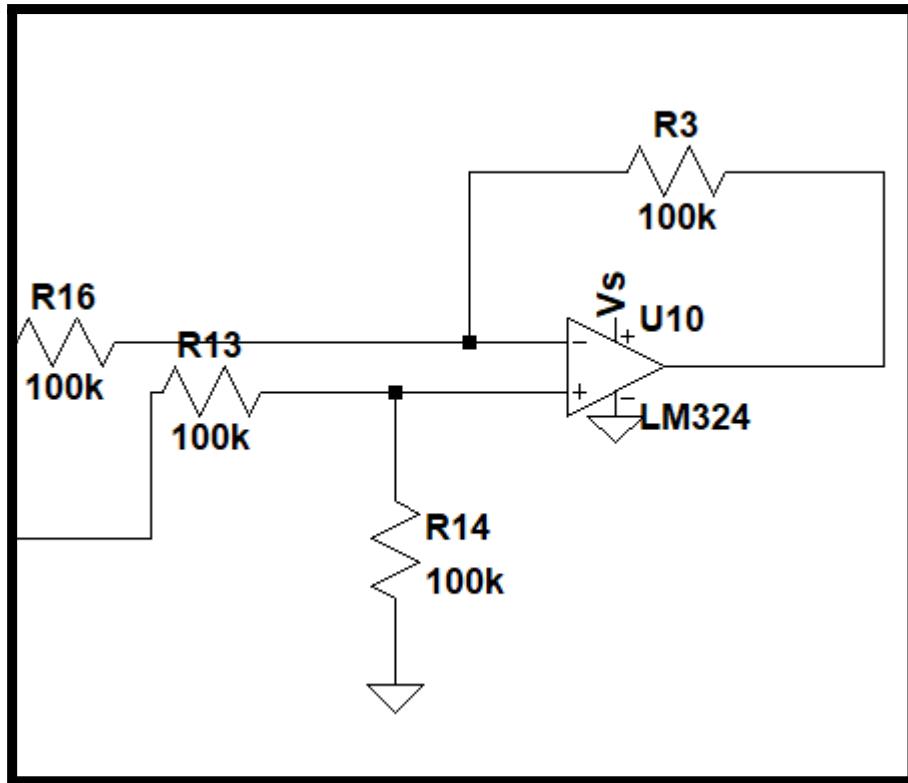


Figure 3: Subtraction Circuit

We need to subtract the integrated waveforms. Performing nodal analysis on the subtraction circuit gives us the formula for the output as:

$$\frac{V_1 - \frac{V_2}{2}}{R} + \frac{V_{out} - \frac{V_2}{2}}{R} = 0$$

$$V_1 - V_2 = V_{out}$$

Software Implementation:

Combining the parts into a single circuit gives us our implementation for the LTspice simulation.

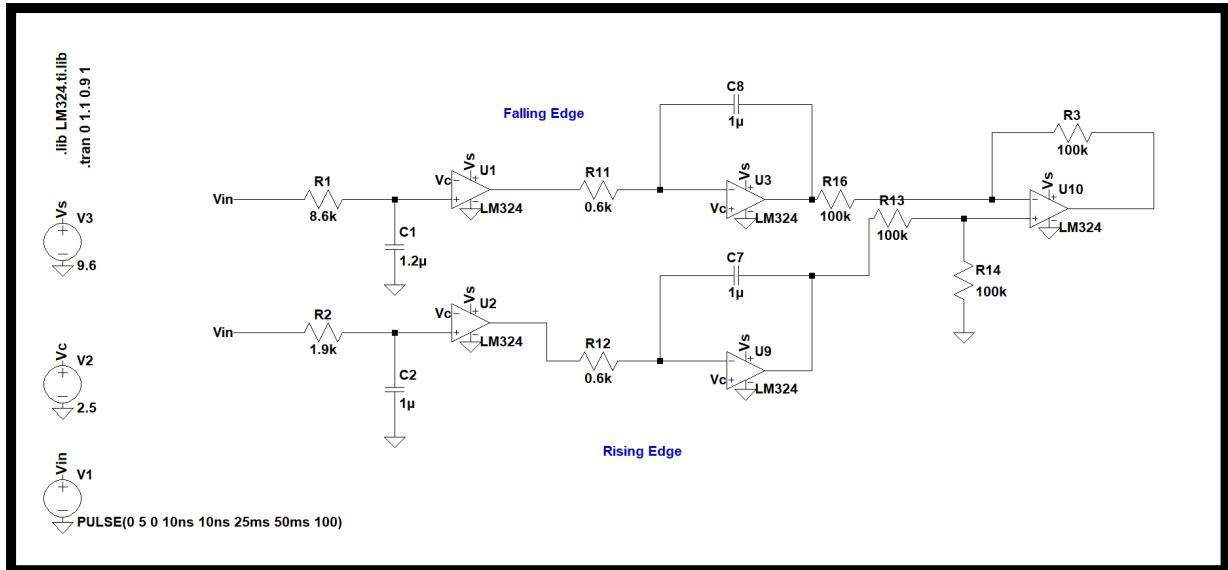


Figure 4: Software Circuit

After implementing the circuit with the given RC values the waveforms are as shown:

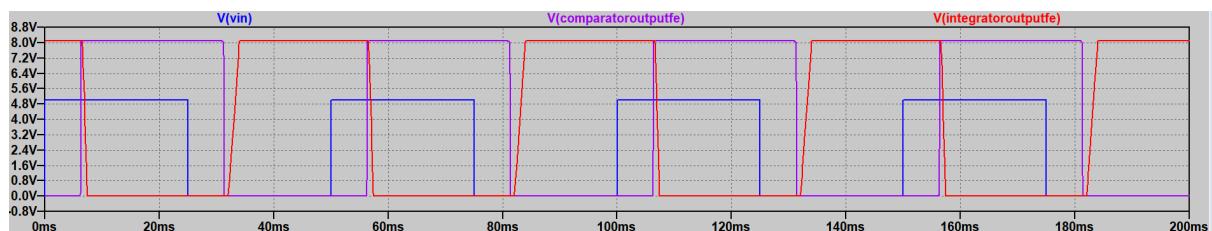


Figure 5: Falling-Edge Comparator and Integrator Output

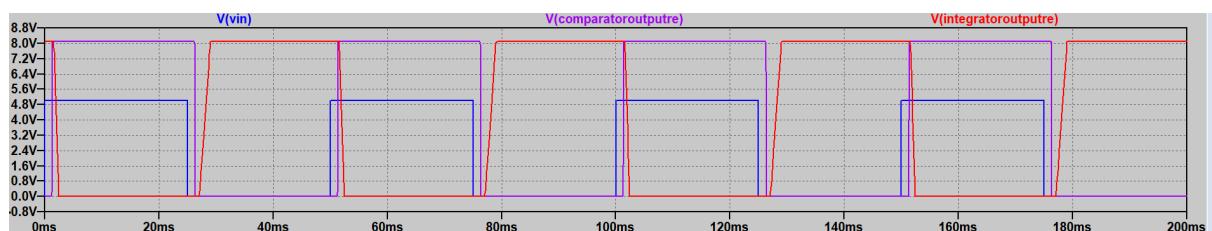


Figure 6: Rising-Edge Comparator and Integrator Output

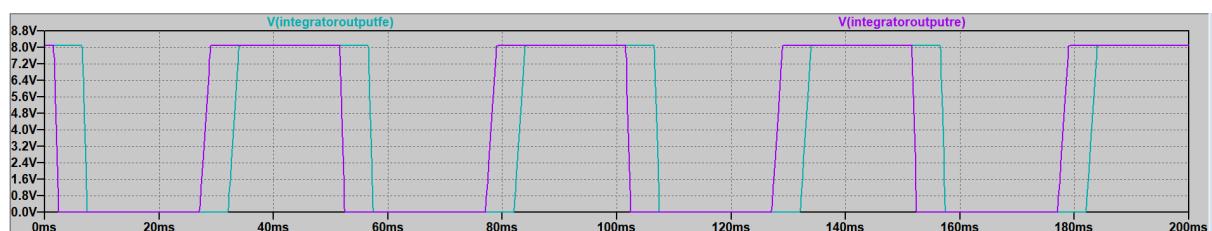


Figure 7: Integrator Outputs Side by Side

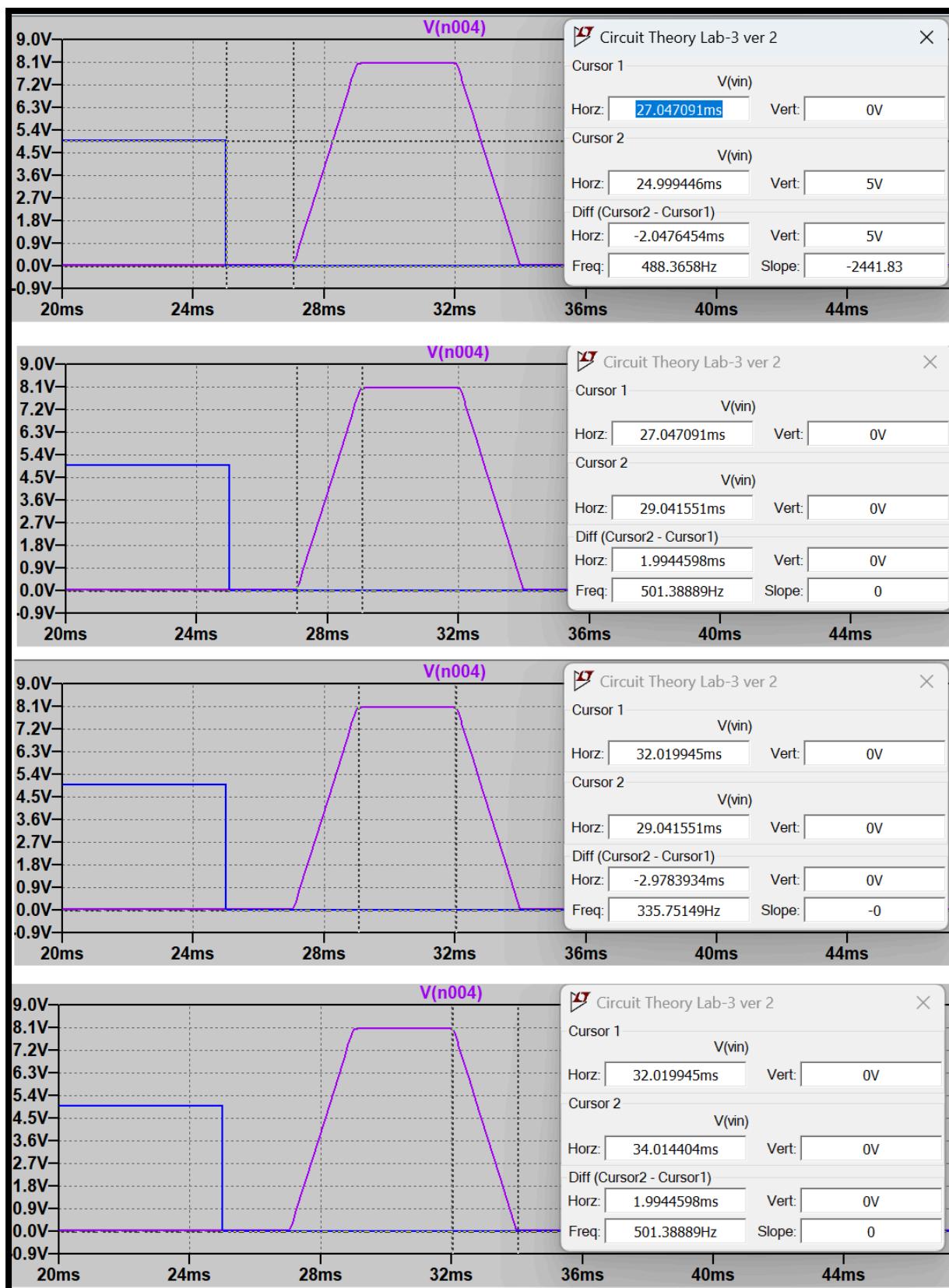


Figure 8: Software Implementation Waveform

Hardware Implementation:

While implementing the hardware, the same RC values are used. However, the capacitance was minimized while the resistance was increased to minimize the error. The voltage spikes or drops around the edges were also eliminated with this method.

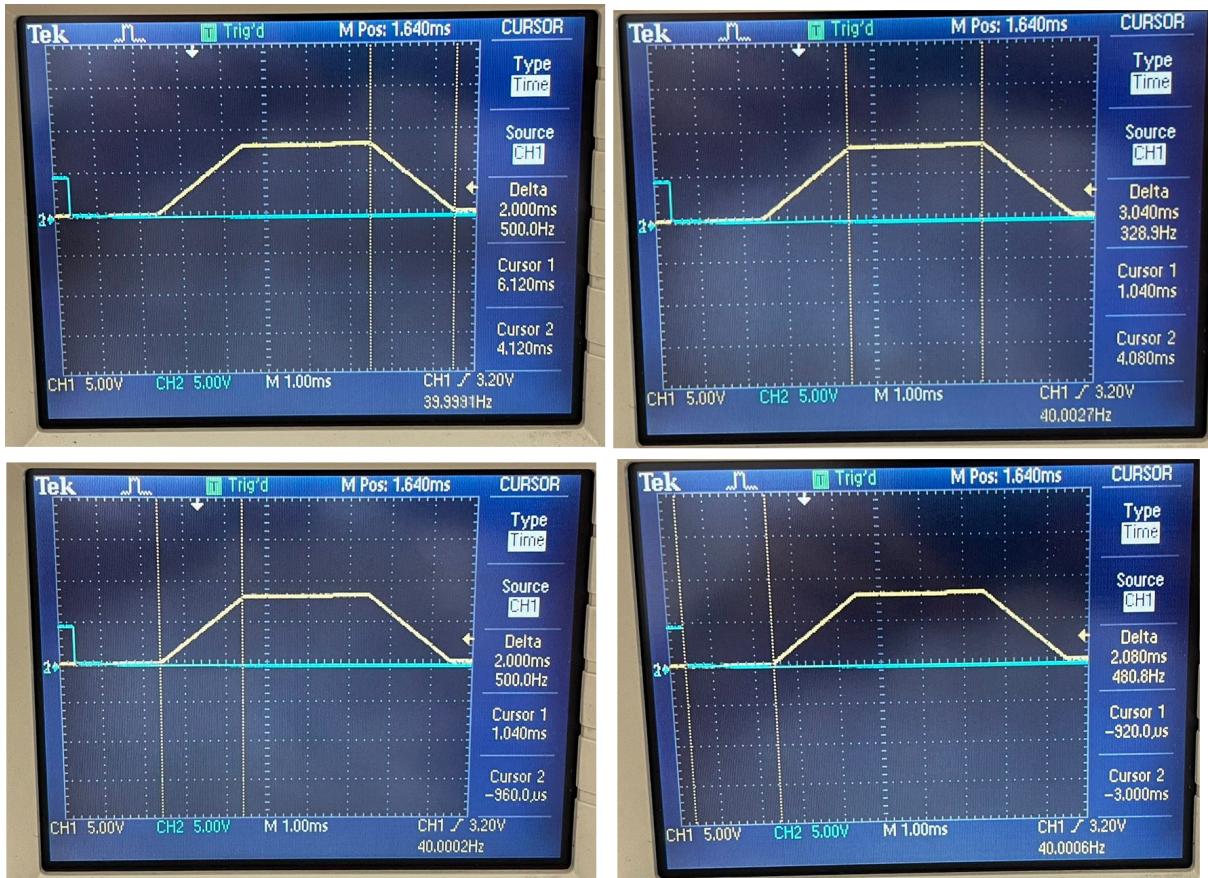


Figure 9: Output Waveform Time Measurements



Figure 10: Output Waveform

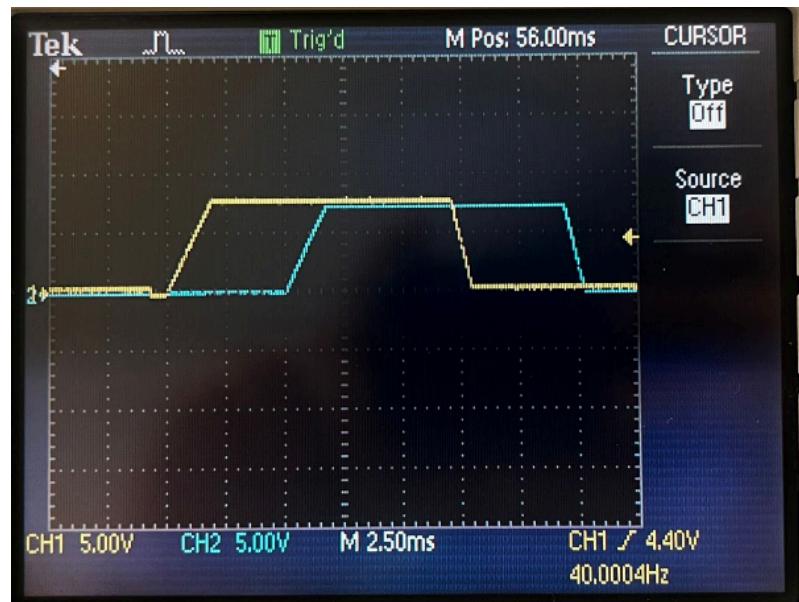


Figure 11: Integrator Outputs

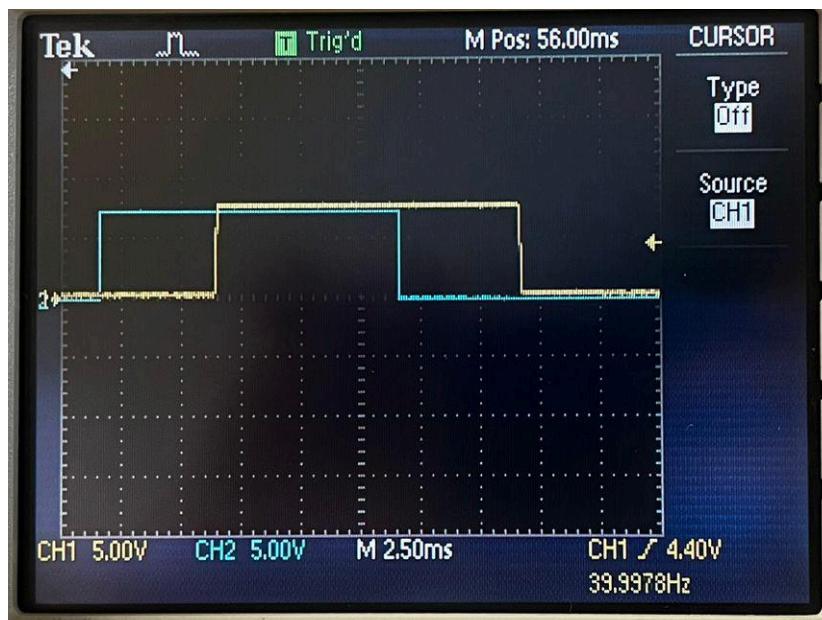


Figure 12: Comparator Outputs

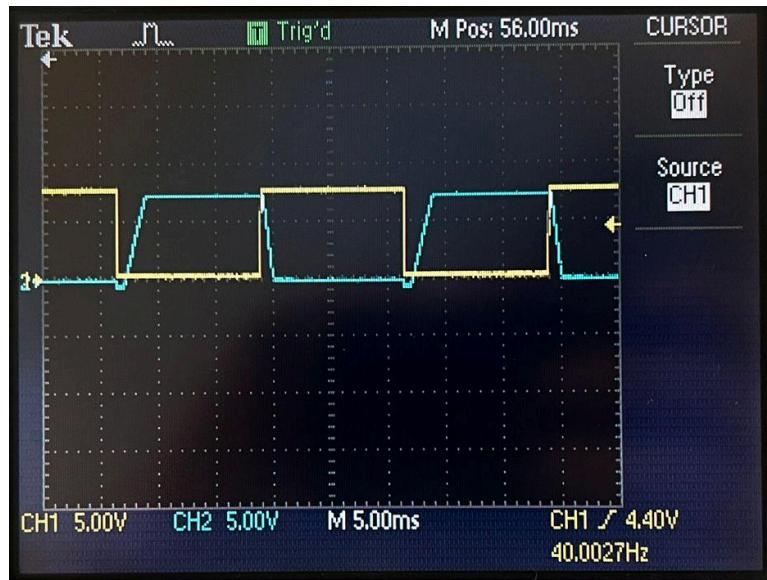


Figure 13: Comparator and Respective Integrator Output

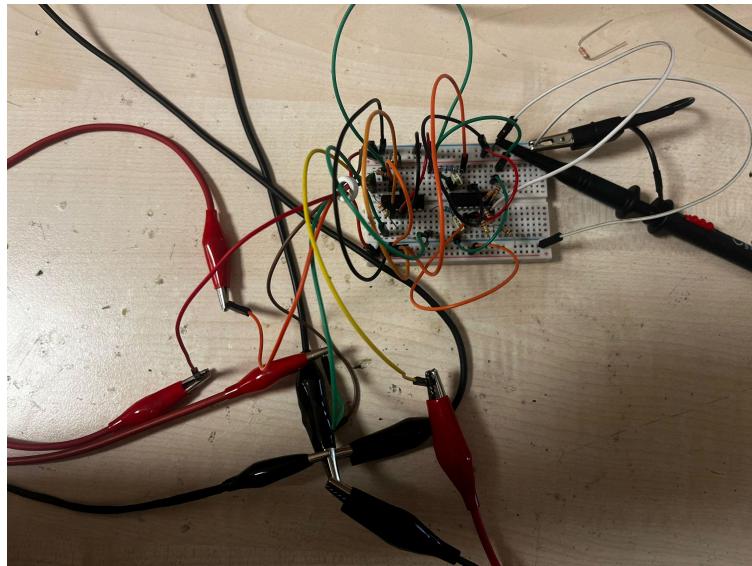


Figure 14: Hardware Circuit

Error Calculation:

The possible errors of this circuit stem from non-ideal OPAMP's, oscilloscope's minimum measuring width for the given time interval, and the fact that exact RC values cannot be achieved using the standard values for the components. In the end, the highest error rate was 4% with the lowest being 0%.

Conclusion:

In conclusion, in this lab we designed three components to create the desired waveform. A RC-delay circuit featuring a comparator, an integrator, and a subtractor. The mathematical calculations for these components were performed and the appropriate values for the components were selected. In the end, the circuit was designed and implemented both in software and in hardware. The error rates were between 0-4% for the desired time intervals. There were no additional spikes.