EE313 Laboratory #3

Single-Supply Push-pull Class-B Power Amplifier

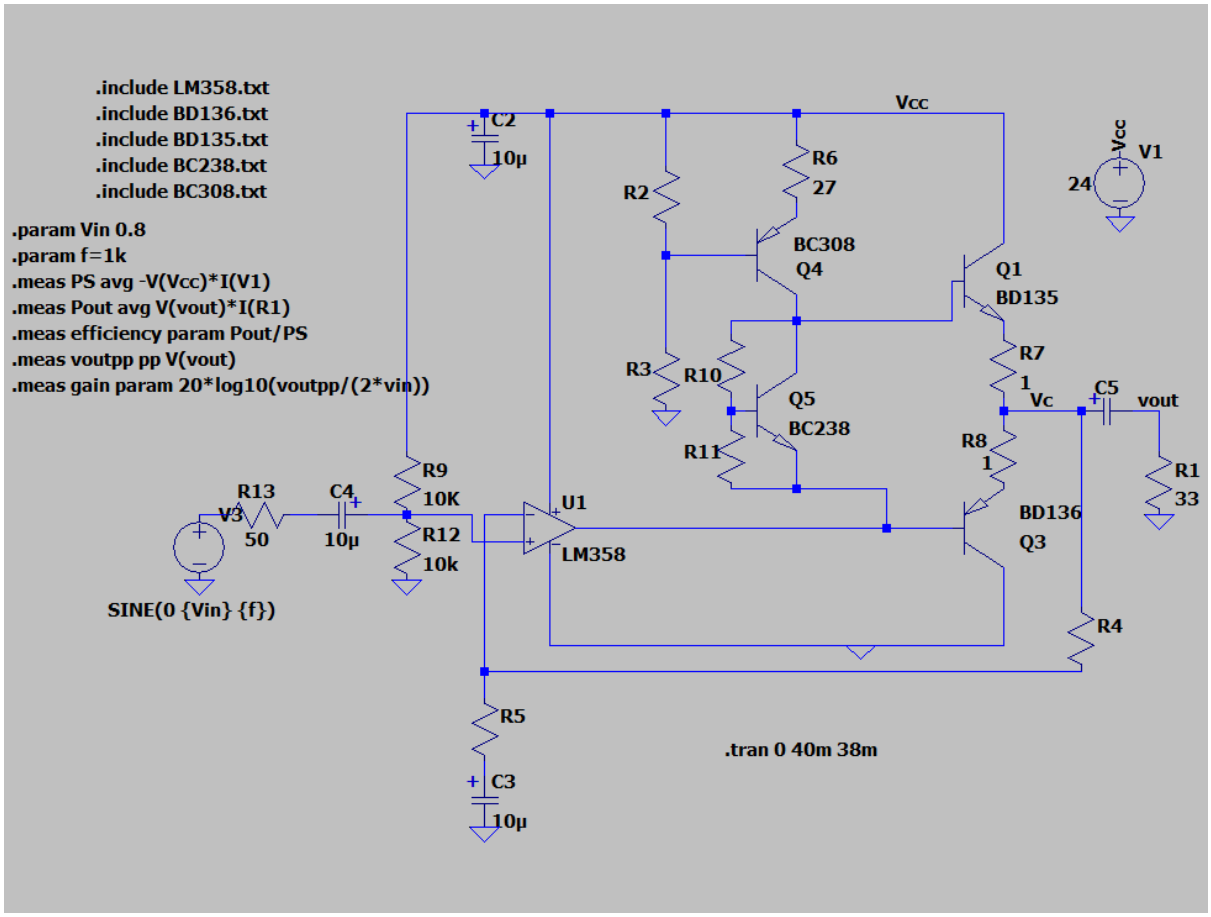
Design a single-supply complementary push-pull Class-B power amplifier capable of delivering at least 0.95W to a 33Ω resistive load. The supply voltage is +24V. It should operate with sinusoidal voltages with a gain equal to 20+mod(BilkentID,7) dB. The SRS DS345 signal generator provides the input *without* an offset. The −3dB bandwidth should cover 150Hz to 15KHz.

Specifications:

1. The amplifier should deliver at least 0.95W power to a 33Ω resistance ($16V_{pp}$ to a 33Ω power resistor) at 1KHz with the chosen gain value.
2. The harmonics (the highest is possibly the third harmonic) at the 0.95W output power level should be at least 40 dB lower than the fundamental signal at 1 KHz.
3. The power consumption at quiescent conditions should be less than 500mW.
4. The amplifier's efficiency (output power/total supply power) should be at least 40% at max power output (0.95W) at 1KHz.
5. The −3dB bandwidth of the amplifier should be at least 150Hz to 15KHz.

Preliminary work (Due November 18, 2024)

Provide a schematic of your design, showing a component list. Use Diptrace to generate the schematic. Available transistors: BC238 (npn, small-signal), BC308 (pnp, small-signal), BD135 (npn, power), BD136 (pnp, power). A suggested circuit for a gain of 20dB is given below. If the chosen gain value is different than 20dB, you should change the input signal accordingly (.step param Vin …).



- You need to use a large-value DC block capacitor between the output of the amplifier and the load resistor. Its reactance at the lowest frequency (150Hz) should be less than 33Ω.
- R1 is the 33 Ω load resistor connected to the output through a DC-block capacitor.
- R7 and R8 are emitter resistors, protecting emitter-follower configuration output transistors (to some degree) against short circuits. When the output load resistor is shorted, the voltage across R7 or R8 grows, reducing the base-emitter voltage, hence limiting the current.
- Q4, R6, R2, and R3 form a current source. The current value should be chosen in the 6-8mA range to supply the base current of Q1. Choose R3 so that the current through it is about $1/10^{th}$ of the chosen current. Adjust the value of R2 so that the collector current of Q4 is at the chosen value. For R2 and R3, use the standard value resistors. (Do not try to connect the resistors in series or in parallel to achieve the required value).
- Q5, R10, and R11 form a V_{BE} multiplier. The V_{CE} of Q5 should be in the range 1V to 1.1V ($V_{CE} \approx (1+R10/R11)V_{BE}$). This value should be adjusted to make the quiescent current of Q1 and Q2 very small (a few mAs). You should properly choose the resistors R10 and R11 (using standard resistor values in the range 1K to 10K) to achieve Class-B condition. If the V_{CE} of Q5 is too high, the circuit gets more into Class-AB operation, and the efficiency decreases. If the V_{CE} of Q5 is too low, the output voltage's distortion (harmonic content) will increase due to cross-over distortion.
- OPAMP provides the base current of Q3. The data sheet of LM358 tells us that it can provide a sink current of 10mA (minimum), 20mA (typical).
- The OPAMP, along with R4 and R5, form a feedback circuit to set the gain of the amplifier. The voltage gain is given by (1+R4/R5). Note that the negative feedback circuit is connected between the output and the − input of the OPAMP since Q3 has no phase inversion. Choose the resistor values in the range 1K to 33K.
- The voltage divider network (R9 and R12) provides the bias voltage to the positive input of the OPAMP. This bias voltage is equal to the quiescent voltage at the node Vc because of the DC feedback through R4. (At DC, R5 is not in the picture since there is a DC block capacitor of C3). R9 is chosen equal to R12 to make Vc quiescent voltage at half the supply voltage.
- R13 simulates the source impedance of the DS345 signal generator in LTSpice. Note that the peak-to-peak reading on the DS345 signal generator assumes that there is a load of 50Ω connected to its output. Since the input impedance of this amplifier is much higher, the actual input voltage is twice the read value.
- C2 is a power supply decoupling capacitor needed in every circuit to make power supplies act like AC short circuits.
- Find the gain and efficiency of the amplifier as a function of the input level. Use the spice directives as follows:

```
.step param Vin begin end step          (to step the peak input voltage)
.param f 1k                             (to set the input frequency to 1KHz)
.meas Pout AVG V(vout)*I(R1)            (to find the output power, R1 is the 33 Ω load
resistor    with a voltage label of vout)
.meas PIN AVG -V(vcc)*I(V1)             (vcc is the positive supply voltage label, V1 is the
positive voltage source)
.meas Efficiency param Pout/PIN         (Efficiency is the ratio of the output power to supply
power)
.meas voutpp pp V(vout)                 (measure the output load resistor p-p voltage)
.meas gain param 20*log10(voutpp/(2*Vin)   (list the gain in dB at each input level)
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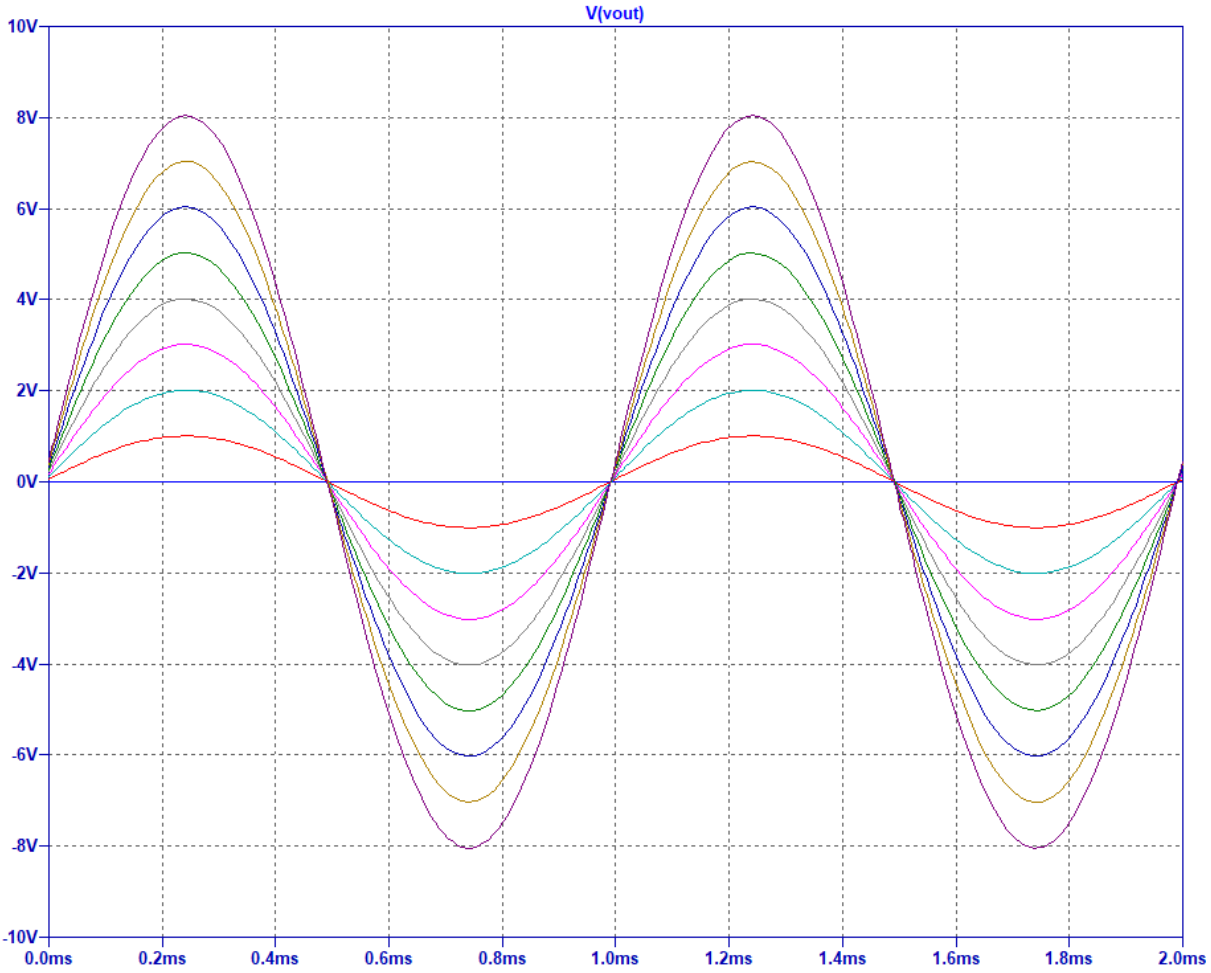
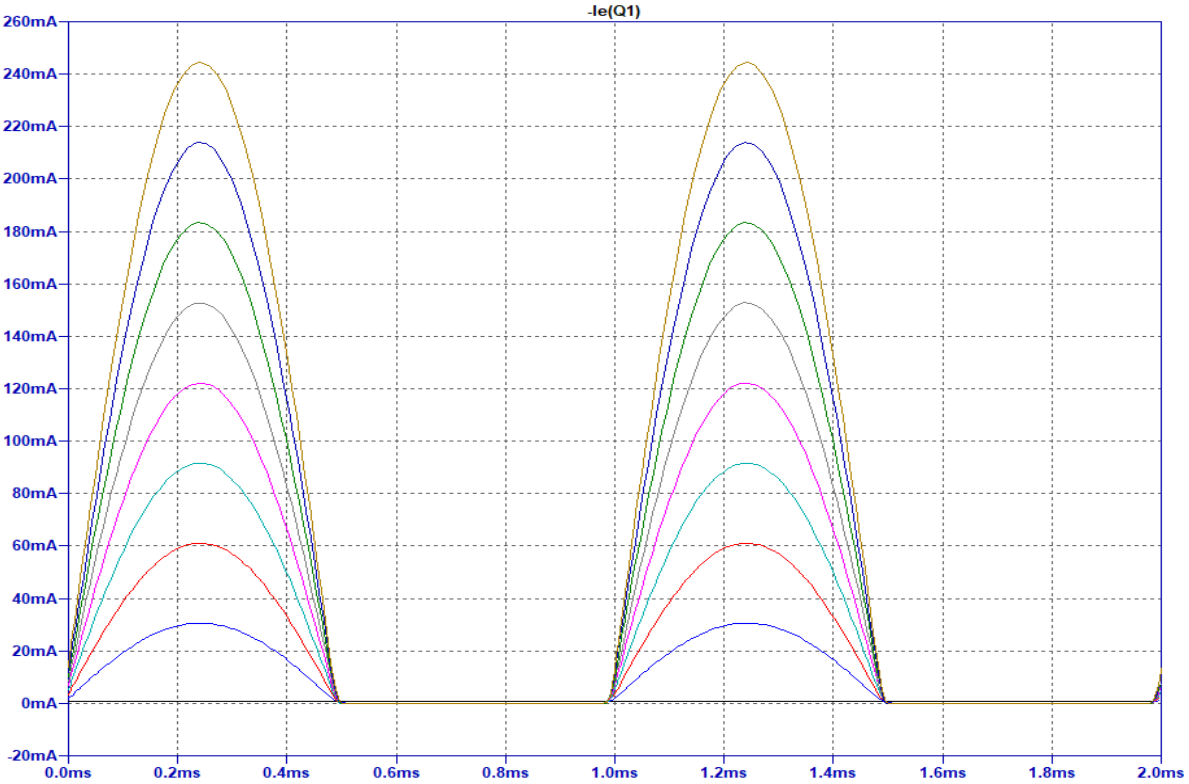
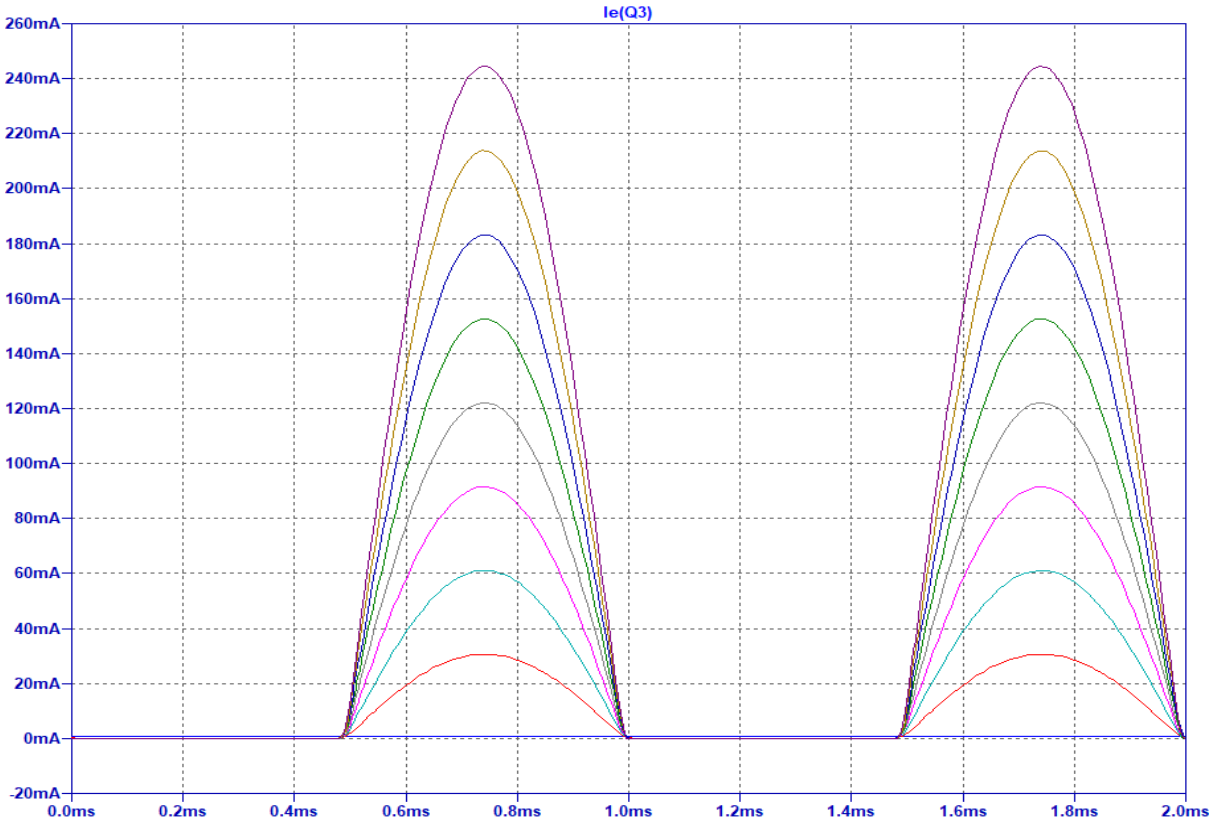


The emitter current of Q1 should be like below. Note that the current is zero for half the period.



The emitter current of Q3 should be like below:



After running the simulation, click CTRL-L to see the results at each step. In your report, the graphs should show two cycles of the output waveform, like the one shown above (For an accurate FFT, you need 20 cycles in the plot window).

Power delivered by the supply as a function of input level (between 0 and 0.8V in 0.1V steps)

Measurement: ps

step	AVG(-v(vcc)*i(v1))	FROM	TO
1	0.237084	0	0.002
2	0.455168	0	0.002
3	0.686443	0	0.002
4	0.917858	0	0.002
5	1.14906	0	0.002
6	1.38028	0	0.002
7	1.61135	0	0.002
8	1.84221	0	0.002
9	2.07325	0	0.002

The output power as a function of input level:

```
Measurement: pout
  step             AVG(v(vout)*i(r1)) FROM             TO
     1             2.95905e-21        0                0.002
     2             0.0153105          0                0.002
     3             0.0612245          0                0.002
     4             0.137701           0                0.002
     5             0.244733           0                0.002
     6             0.382345           0                0.002
     7             0.55054            0                0.002
     8             0.749326           0                0.002
     9             0.979015           0                0.002
```

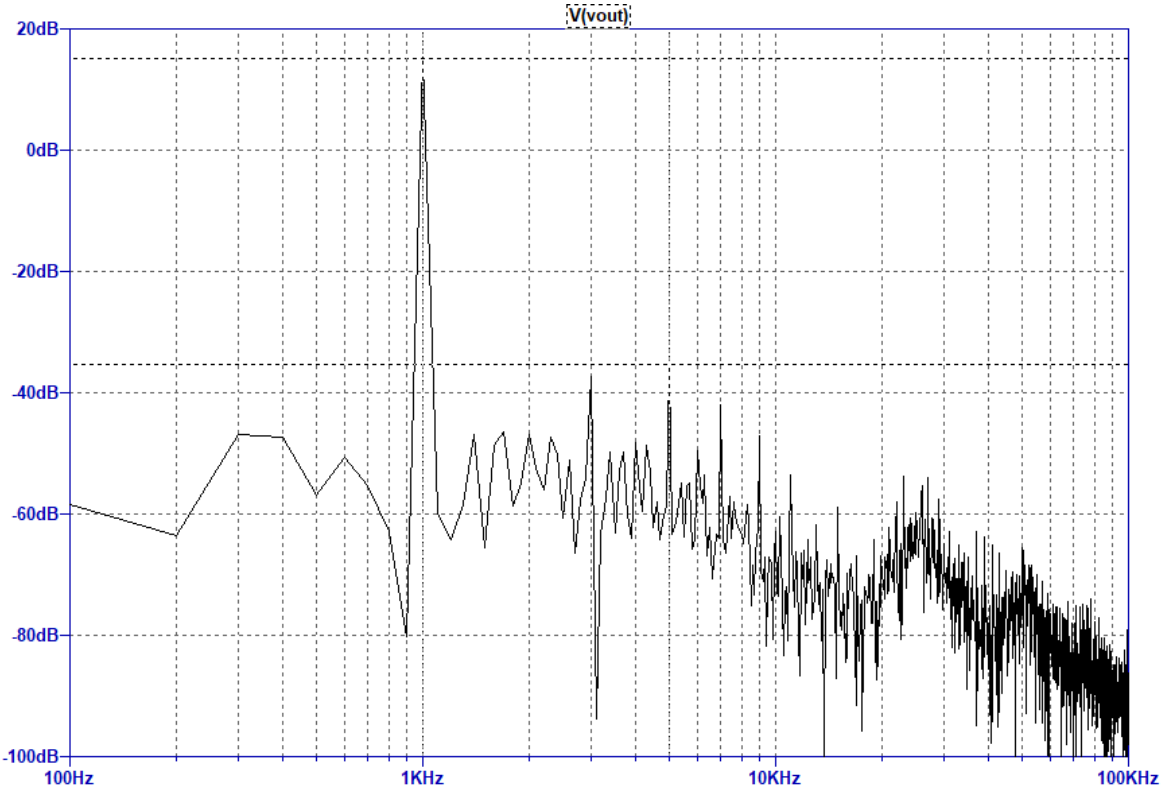
The efficiency as a function of input level:

Measurement: efficiency

step	pout/ps
1	1.2481e-20
2	0.0336371
3	0.0891908
4	0.150024
5	0.212986
6	0.277005
7	0.341663
8	0.406754
9	0.472212

Note that LTSpice can show the instantaneous power dissipated on a component by ALT-Click. You can find the average power by CTRL-Click on the instantaneous power symbol in the graph window if an integer number of signal cycles is shown. The common resistors in the lab can dissipate a maximum of 0.25W. No resistor (except the load resistor) in the circuit should exceed this value.

To find the magnitude of the harmonics, simulate with 10 complete cycles visible on the plot window. Then, right-click on the plot window, View → FFT, to see the amplitude of different harmonics. You can find the dB difference between the fundamental (at 1 KHz) and the third or fifth harmonic (at 3 kHz or 5kHz) using the difference between the two cursors (double click on v(vout). In the example below, the difference between the fundamental and 5^{th} harmonic is 50.3dB.



Cursor 1			
	V(vout)		
Freq:	1000Hz	Mag:	15.010424dB
		Phase:	-86.550738°
		Group Delay:	-1.5586466ms
Cursor 2			
	V(vout)		
Freq:	5KHz	Mag:	-35.279932dB
		Phase:	-108.81223°
		Group Delay:	2.2020668ms
Ratio (Cursor2 / Cursor1)			
Freq:	4KHz	Mag:	-50.290355dB
		Phase:	-22.261497°
		Group Delay:	3.7607135ms

- Find the amplifier's gain as a frequency function for the maximum input level using transient analysis and spice directives. Note that small-signal analysis is not suitable for a Class-B amplifier. Use the spice directive:

  .step param f begin end step

  .param Vin 0.8

  with {f} defined as the frequency parameter of the input source.

Upload your LTSpice asc file as well as your report to Moodle.

Experimental work (Due November 24, 2024)

Build your design on the breadboard neatly. Do not connect the load resistor R1 yet. Use heat sinks for power transistors. Place the active components so that the required wiring is either short or there is no need for wires. Cut the leads of resistors to prevent dangling, which may cause short circuits between nodes. Make sure that the orientation of transistors is correct. If you connect them backward, the transistors will die, and the debugging will be difficult. Check the interconnection wires before plugging them in. Some interconnection wires may have nonfunctioning pins. Place your components so that a small number of interconnection wires is needed.

Follow the steps below:

1. Apply the supply voltage while gradually increasing it. The supply current should be small (less than 20mA for 24V). If not, check your connections. There may be missing connections or faulty cables, and the transistor pins may be incorrect. Measure the voltage between the base and emitter for each transistor. Make sure that you measure a voltage of around 0.6V. Measure the collector-emitter voltages of each transistor. All transistors must be in the active region.
2. Measure the voltages at all nodes and compare them with the expected values. If the voltages at different points of the same node are different, those points are not connected to each other: You either have a faulty wire or a bad contact in the breadboard.
3. Measure the collector-emitter voltage of the V_{BE} multiplier circuit. It should be about 1.0V to 1.1V. A higher voltage will result in a higher quiescent current.
4. Measure the voltages at the input pins of the OPAMP with respect to ground. They should both be about 12V.
5. Measure the voltage between Vc and ground. It should be also about 12V. If not, check the connection of R4.
6. Apply the 1KHz 0.1V peak input signal from the lab signal generator. Connect the oscilloscope to the output load. You are on the right track if you see an amplified signal with zero offset at the output pin.
7. You may now increase the input signal while observing the power supply current.
8. Connect the 33Ω load resistor. Apply a 0.1V peak. You should still see the amplified signal with zero offset. The power supply current should increase.
9. Measure the gain as a function of frequency at the maximum input level. Determine the lower and upper frequency where the gain drops by 3 dB.
10. Find the amplitude of the harmonics under the full-power condition using the FFT feature of the oscilloscope at 1KHz with 0.95W output power.
11. Measure the power supply current under quiescent conditions.
12. Measure the efficiency as a function of input level at 1KHz.

Debugging:

1. With no input signal, check the DC voltages of all transistors. V_{BE} should be 0.6V for the npn transistors, and −0.6V for the pnp transistor. Check the V_{CE} for all transistors. They should be in the active region.
2. Older breadboards may have increased contact resistance if the connections are loose. Try using other holes in the breadboard for better contact resistance.
3. If the quiescent current is too high, check the voltage across the V_{BE} multiplier circuit. It should be about 1 to 1.1V. If it is higher, reduce the value of R10 one step.

4. If there is distortion at the top of the signal, the current source transistor Q4 is not providing enough current. You can change this current with the bias resistors R2 or R3. Measure the DC voltage across R6 to determine the current. It should be about 6mA. If there is distortion at the bottom of the signal, Q4 is providing too much current, and the OPAMP cannot sink it. Try reducing the current of Q4 by changing the bias resistors R2 or R3.
5. When you make changes, change the resistors one step at a time. Do not make large step changes.
6. If the harmonics are larger than expected, you may have a cross-over distortion problem. Check the V_{BE} multiplier circuit voltage.

Grading criteria:

Preliminary work (10 pts)

Satisfaction of all five criteria in LTSpice: 2 pts each

Experimental work (10 pts)

Receiving a check by the assistant: 3pts

Experimental satisfaction of all five criteria: 5 pts, 1pt each

Efficiency plot as a function of input level: 1pt

Gain plot as a function of frequency at max input level: 1pt