

EEE 313 - Electronic Circuit Design - Lab 4 Preliminary Report

Tuna Şahin - Wide-Band Amplifier

1 - Introduction:

In this lab we were asked to implement a two-stage wide-band amplifier with feedback. Due to the feedback, the gain of the amplifier is stable and not ' β ' dependent.

2 - Calculations:

I arbitrarily chose $I_{C1} = 9mA$ and $I_{C2} = 33mA$ at DC to leave room for the current swing at AC so it is less than 70mA. (We need $V_{E1} = V_{E2} \approx 1V$)

We need to choose $R_1, R_3, R_4, R_5, R_6, R_8$ biasing resistors to obtain these values.

By writing the mesh for the base emitter line of the first transistor:

$$I_{C1} \frac{R_1}{\beta} + R_2 I_{C1} = 12 - V_{BE} \Rightarrow 9m = \frac{11.4}{R_1/400 + R_2} \quad (i) \quad \text{We obtain a solution: } R_1 = 390k, R_4 = 47$$

For the second transistor:

$$V_{TH} = 12 \frac{R_6}{R_5 + R_6} \text{ and } R_{TH} = R_5 \parallel R_6 \quad V_{TH} - \frac{I_{C2}}{\beta} R_{TH} - V_{BE} - I_{C2} R_8 = 0 \quad (ii)$$

We get a solution as: $R_5 = 3900, R_6 = 820, R_8 \approx 40$

Gain resistors are chosen as $R_9 = 560$ and $R_4 = 47$ which give a ratio of approximately 12.

Emitter bypass capacitor $C_4 = 220\mu$ from the formula $X_{C4} = R_8 \parallel \left(\frac{1}{g_{m2}}\right)$

All of the bypass capacitors are chosen as $10\mu F$.

Collector resistors are chosen as their maximum value where the wave does not saturate.

3 - LTSpice Schematic:

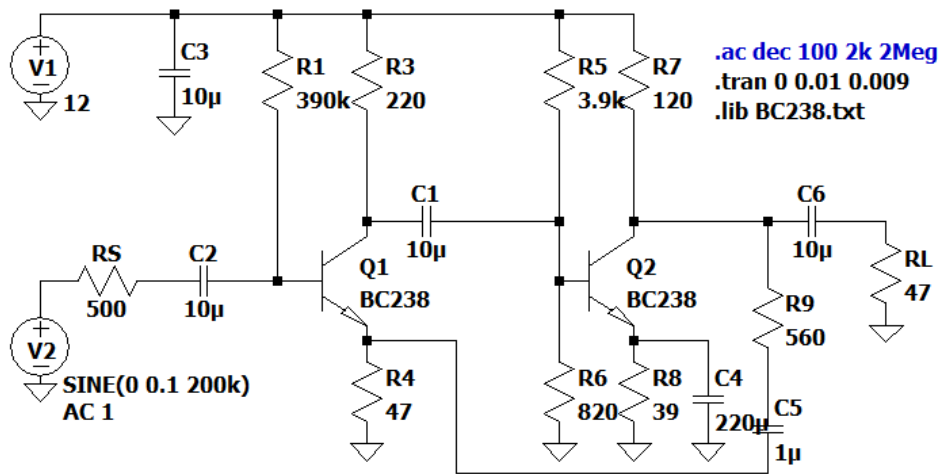


Figure 3: LTSpice Schematic

(i) One equation, two variables. Arbitrarily chose 390k for R_1

(ii) One equation, three variables. Arbitrarily chose R_5 and R_6

4 - LTSpice Simulations:

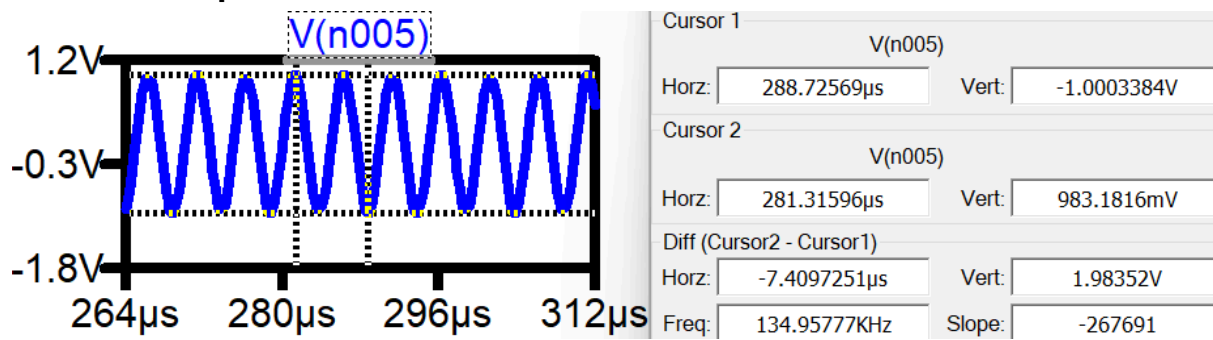


Figure 4.1: $V_{out} = 1.98V_{pp}$ when $V_{in} = 0.2V_{pp}$ (Gain = 19.91dB)

Specification 1: The current consumption is less than 70mA

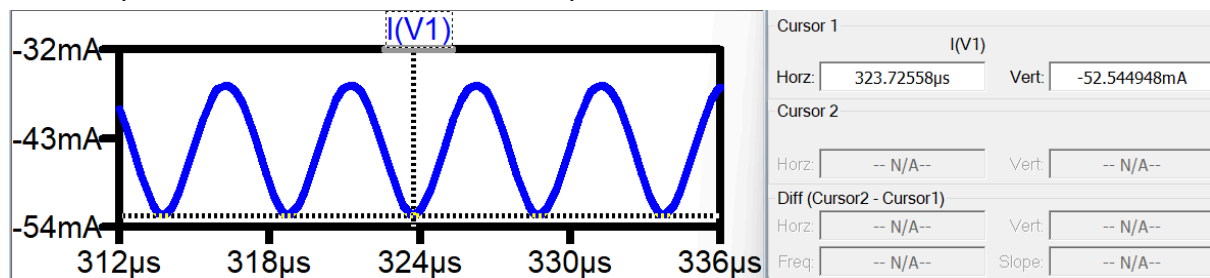


Figure 4.2: Peak Source Current Observed to be 52.5mA

Specification 2: The small-signal bandwidth is at least 2KHz-2MHz while the mid-band gain is 20dB±0.5dB (by AC analysis)

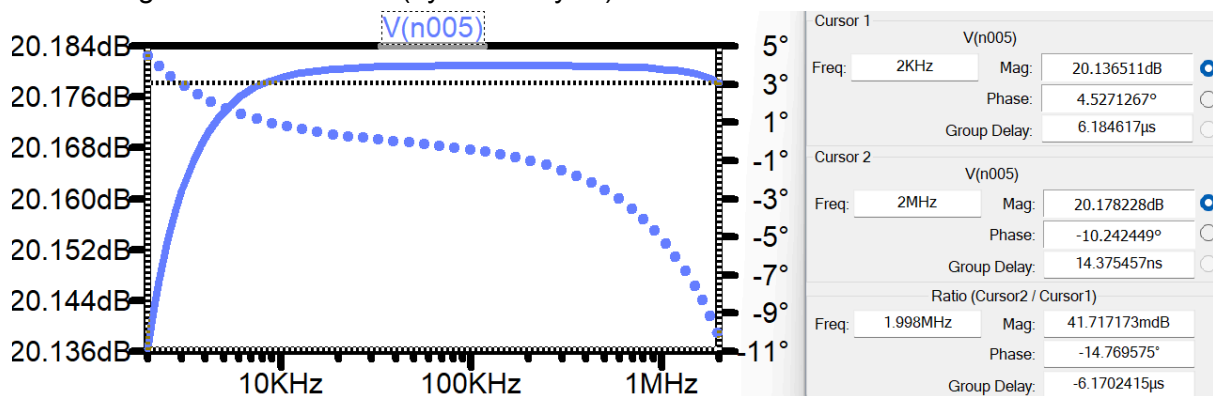


Figure 4.3: -3dB Bandwidth is found to include 2kHz-2MHz (AC Sweep Settings: 200Hz - 20MHz)

Specification 3: The harmonic content of the output voltage is better than -30dBc with 0.1V peak input signal at 200KHz

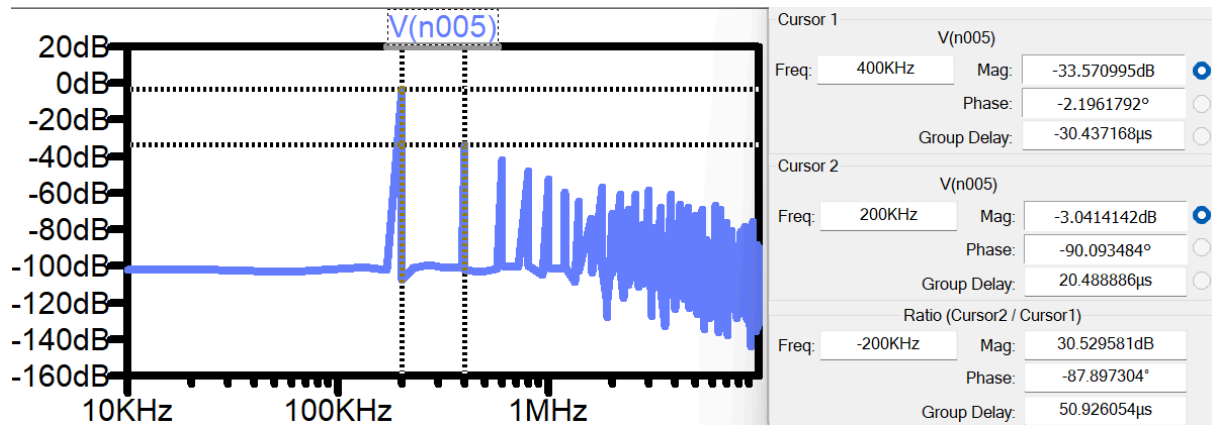


Figure 4.4: The Highest Harmonic (2rd) is 30.5dB Lower than the fundamental harmonic.

Determination 1: The small-signal input impedance of the amplifier at 200KHz (the adjusted value of R_S in AC analysis until the voltage gain drops by 6dB compared to $R_S=0$)

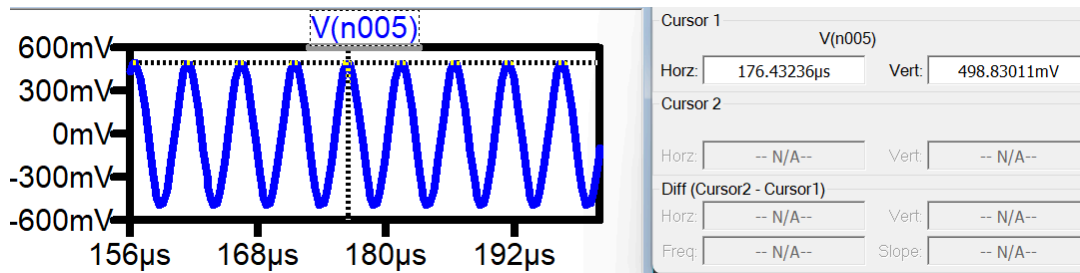


Figure 4.5: The gain is 14dB when $R_S = 60k$ ($V_{in} = 0.2V_{pp}$ and $V_{out} = 1V_{pp}$)

Determination 2: The small-signal output impedance of the amplifier at 200KHz (the adjusted value of R_L in AC analysis until the voltage gain drops by 6dB compared to $R_L=\infty$)

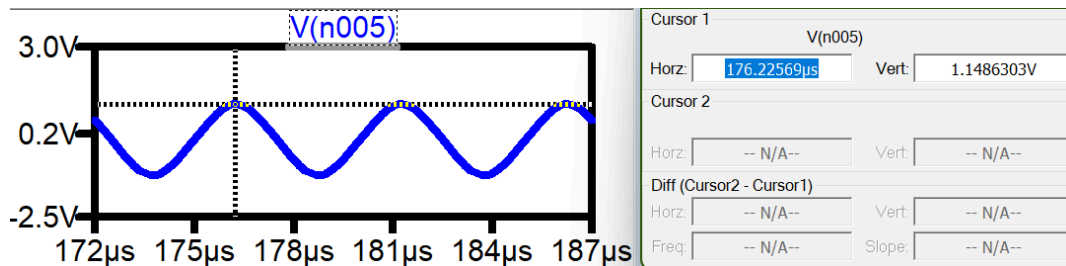


Figure 4.6.1: Gain = 21.21dB when $R_L = \infty$ ($V_{out} = 2.3V_{pp}$ and $V_{in} = 0.2V_{pp}$)

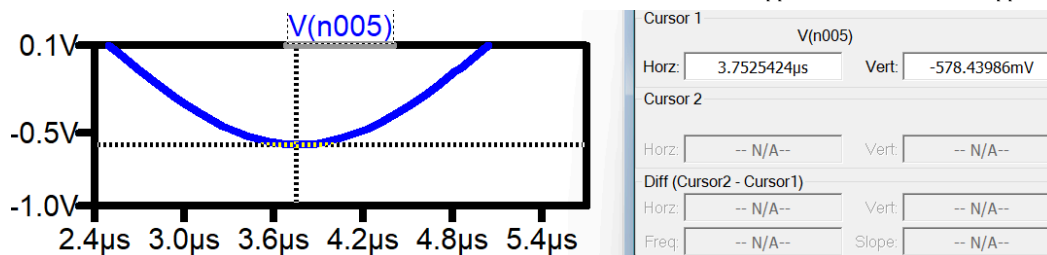


Figure 4.6.2: Gain = 15.23dB when $R_L = 9$ ($V_{out} = 1.156V_{pp}$ and $V_{in} = 0.2V_{pp}$)

Determination 3: The phase margin of the open-loop system.

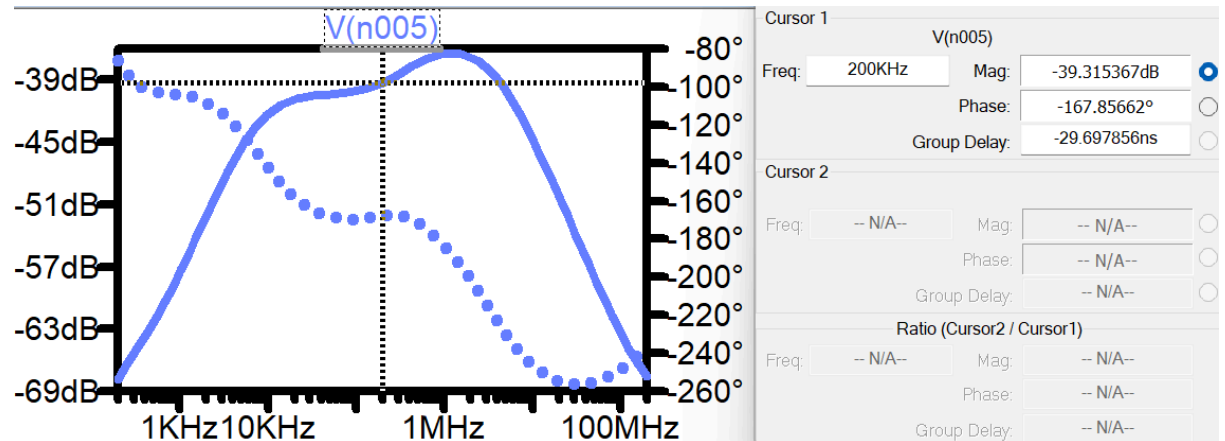


Figure 4.7: Phase Margin is found to be 200 degrees.

5 - Conclusion

To summarise, we were asked to design a two-stage amplifier that had to satisfy some criteria. The amplifier I designed has a band (-3dB) between 16MHz and 74Hz. That interval includes the desired band of 2kHz to 2MHz. The amplifier had a 50mA current consumption which is less than the upper limit of 70dB. And the amplifier's output had a 30.5dB difference between the fundamental harmonic and the second highest harmonic.

- The maximum value of R_S that had -6dB of gain was found to be 60k Ω .
- The minimum value of R_L that had -6dB of gain was found to be 9 Ω
- The phase margin of the open-loop system was found to be 200 degrees

Figure 5: DipTrace Schematic and Component List