DESIGN AND IMPLEMENTATION OF A HIGH EFFICIENCY AC-AC BUCK CONVERTER

André L. Lohman[1] , Elis M. Vieira[1] , Juliene Polasse[1] , Eduardo F. R. Romaneli[2] , Roger Gules[2,3]
[1]Department of Electrotechnics – DAELT
[2]Graduate Program in Energy Systems - PPGSE
[3]Graduate Program in Electrical and Computer Engineering - CPGEI
Federal University of Technology - Parana, Curitiba – Parana, Brazil
e-mail: andre.lohmann91@gmail.com, juliene.polasse@gmail.com, elismarinavieiro@gmail.com, felix@utfpr.edu.br, rgules@utfpr.edu.br

***Abstract* - This paper presents an AC-AC Buck converter in which a modulation technique was applied in order to reduce losses due to dissipative snubbers. Theoretical analysis and numerical simulation were performed. A 100W prototype was built and tested. Efficiency curves show that snubber losses are minimized with the use of a simple open-loop control technique.**

***Keywords* – AC-AC, Buck, Efficiency, Losses, Commutation.**

I. INTRODUCTION

This paper presents the implementation of an AC-AC Buck converter using analog control. The research intended to obtain a better efficiency through commutation of two bidirectional switches. Four-steps switching technique applied to unidirectional switches are proposed in [1,2]. The bidirectional switches are composed by MOSFETs connected in anti-parallel as shown in Figure 1.

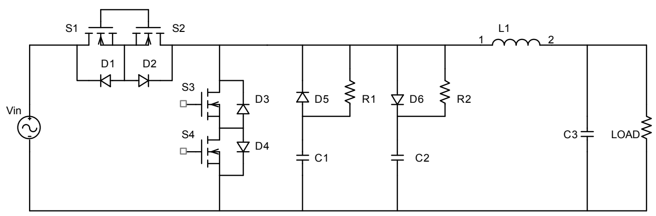

Fig. 1. Topology AC-AC Buck converter.

The step down AC-AC converter aims to decrease the output voltage by applying a Pulse Width Modulation (PWM) control signal. This technique enables the achievement of lower costs and smaller solutions [3] if compared to electromechanical solutions. The topology of AC-AC Buck converter shown in Figure 1 presents overvoltage on MOSFETs as the commutation of the switches occurs. This problem is caused by the energy stored in the inductor. The standard solution is to apply dissipative snubbers connected in parallel in order to absorb that energy suppressing the voltage peaks across the MOSFETs [3,4]. In this case, two dissipative snubbers were used, one in each line voltage half-cycle.

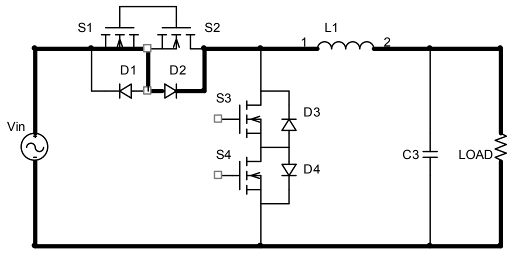

Fig. 2 – High frequency operation during positive semi-cycle ($0 < t \leq D.T$).

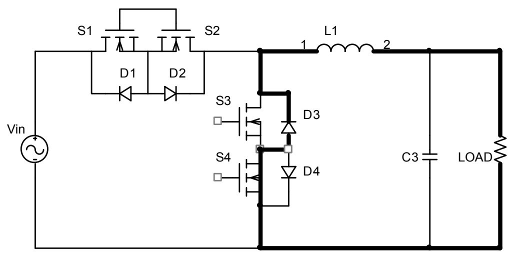

Fig. 3 – Low frequency free wheel operation during positive semi-cycle.

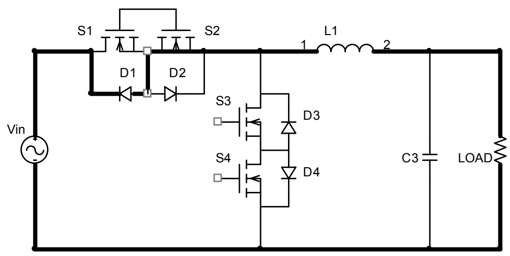

Fig. 4 – High frequency operation during negative semi-cycle ($0 < t \leq D.T$)..

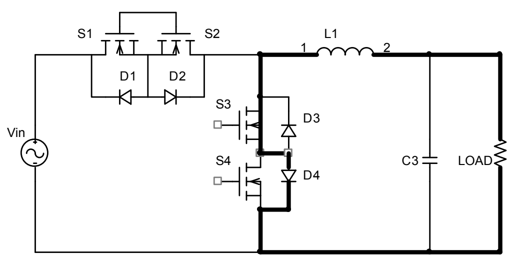

Fig. 5 – Low frequency free wheel operation during negative semi-cycle.

This study enabled the implementation of a modulation in function of the half-cycle of the grid to control one of the bi-directional switches so it creates a path for the current from the inductor [5]. The main difference when compared to a standard modulation technique is that only one of the bidirectional switches modulates at high frequency. The other switch is synchronized along with the line voltage. The decreasing of commutation losses is, therefore, the most significant impact presented by this technique.

II. DEVELOPMENT

This AC-AC converter operation can be summarized into four steps, two of them occur during the positive semi-cycle of the grid and the other two during the negative semi-cycle of the grid voltage.

Both Figures 2 and 4 represent the operation of the converter when the switch controlled by the PWM (S_1 and S_2) is conducting during the positive and negative semi-cycle respectively. Figures 3 and 5 show the converter operation when switches S_1 and S_2 are opened.

The high frequency control signal is implemented with the use of a Pulse Width Modulation (PWM). The signals from the switches S3 and S4, synchronized to the line voltage, are used to control each one of the MOSFETs.

The proposed topology for the AC-AC Buck converter was built and tested according to the electrical specifications shown in Table 1.

TABLE 1
Electrical Specifications

Parameters	Value
Input voltage	127 Vrms/60 Hz
Output voltage	0~127 Vrms/60 Hz
Output power	100 W
Line frequency	60 Hz
Switching frequency	25 kHz
MOSFET ($S_1 – S_4$)	IRF740
Diode ($D_5 – D_6$)	UF4007
C_1, C_2	10nF
C_3	5 µF / 250V
L_1	1 mH
R_1,R_2	330 kΩ

Output LC filter was designed considering a resonant frequency of 2 kHz applied to (1).

$$fc = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \tag{1}$$

Snubbers were calculated considering 200V peak voltage across switches, 300 Hz of resonant frequency and 0.25W total losses in both snubbers. Equation (2) and (3) were applied.

$$R_{snb} = \frac{V^2_{Peak}}{P_{losses}} \tag{2}$$

$$C_{snb} = \frac{1}{2 \cdot \pi \cdot R_{snb}} \tag{3}$$

III. EXPERIMENTAL RESULTS

A 100W prototype was built using UC3525A PWM controller. Control signals were isolated using HCPL316J driver boards shown in Figure 6.Two switches are controlled by a PWM and two are synchronized to the 60Hz line voltage by rectangular waves as shown in Figures 7 and 8.

Fig. 6 – Isolated drive at built prototype.

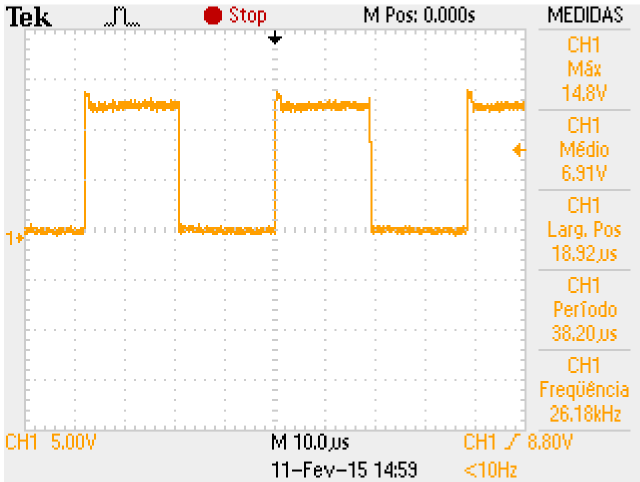

Fig. 7 – High frequency PWM control signal.

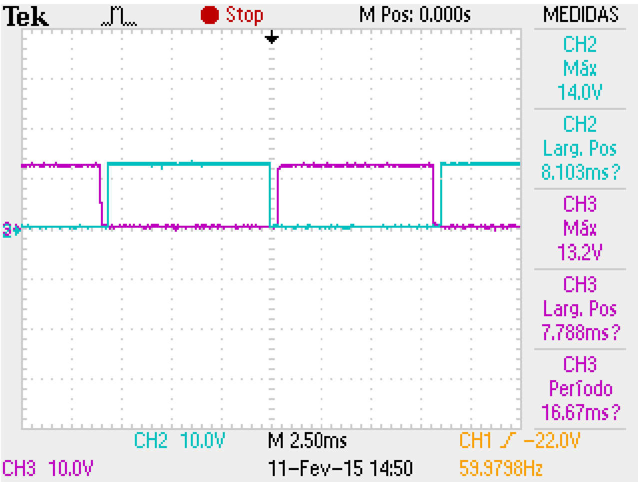

Fig. 8 – Low frequency free wheel control signals..

Switches S3 and S4 open as the line voltage is close to zero. As a result, there will be a dead time between each semi-cycle of the grid in order to ensure a safe operation. The dead times generated are about 400µs as shown in Figures 9 and 10.

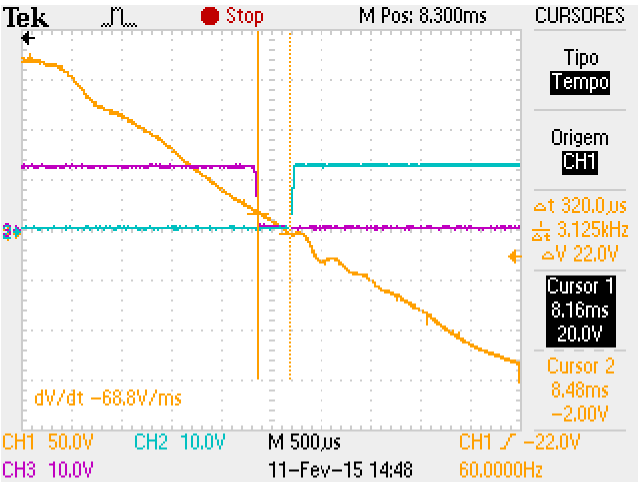

Fig. 9 – Low frequency signal transition from positive to negative semi-cycle.

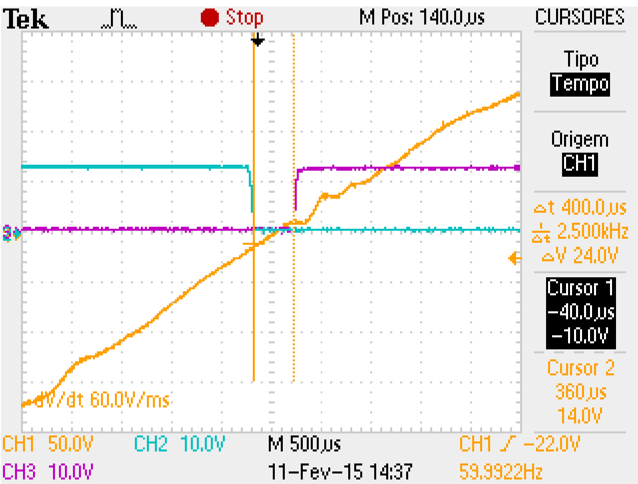

Fig. 10 – Low frequency signal transition from negative to positive semi-cycle.

Small snubbers are placed parallel to the MOSFETs in order to dissipate energy from the inductor, thus preventing an overvoltage across the switches.

Input line voltage and voltage across switches S3 and S4 as well as the snubbers are shown in the Figure 11. A detail of these voltage levels during the peak is also shown in Figure 12.

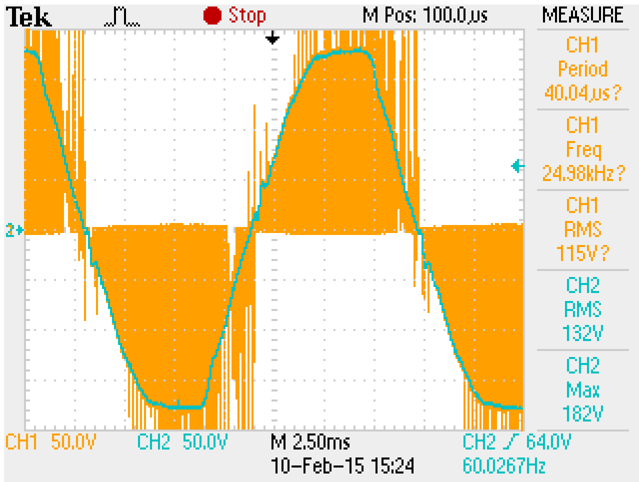

Fig. 11 – Input line voltage and voltage switches S_3 and S_4.

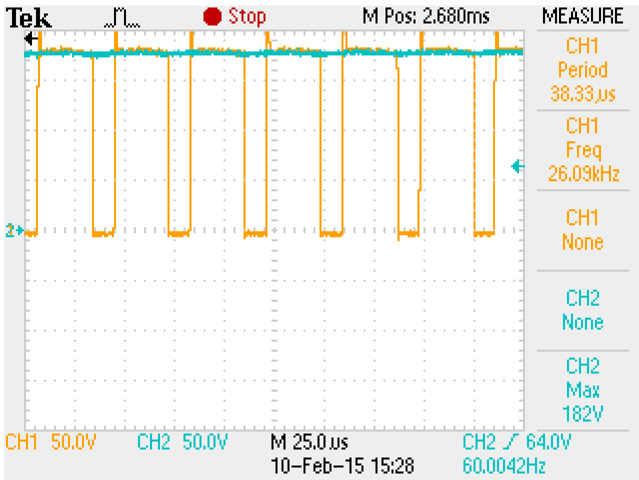

Fig. 12 – Detail of input line voltage and voltage switches S_3 and S_4 during positive peak.

The output voltage can reach levels from 0V to the nominal input voltage as the PWM duty-cycle is adjusted. Figures 13,14, 15 and 16 show the output voltage with the PWM set to different duty-cycles (10%, 50%, 90% and 100%).

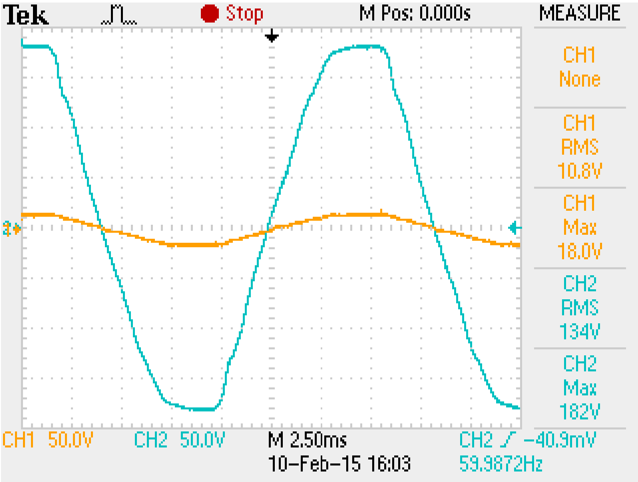

Fig. 13 – Input and output voltage at D=0.1

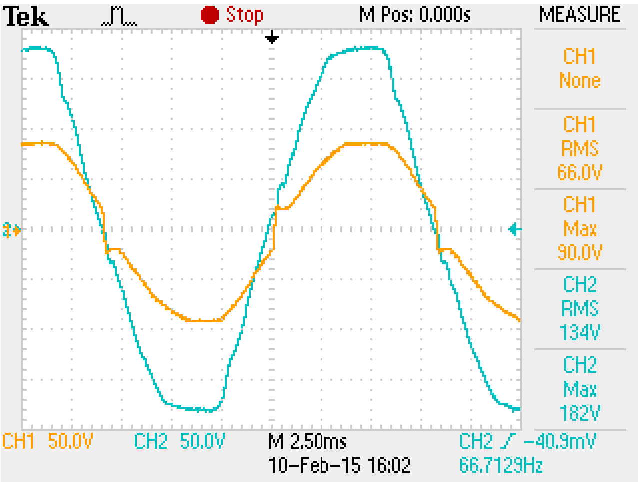

Fig. 14 – Input and output voltage at D=0.5

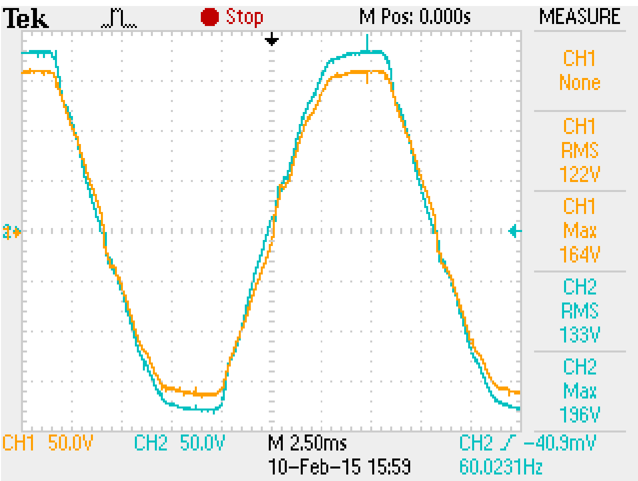

Fig. 15 – Input and output voltage at D=0.9

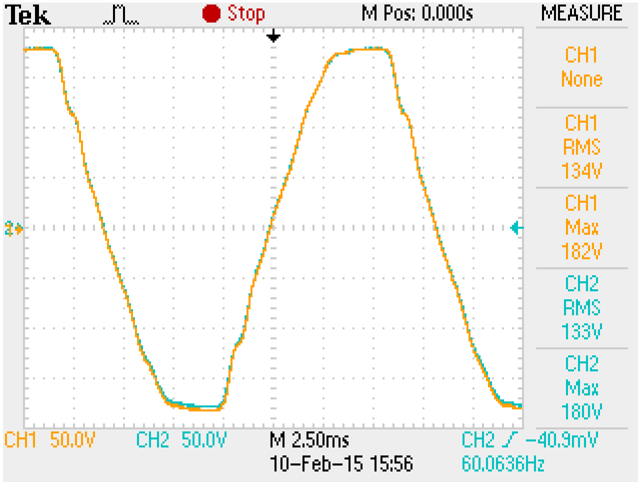

Fig. 16 – Input and output voltage at D=1

Figure 17 shows harmonic distribution of the output voltage when a 0.5 duty-cycle is applied.

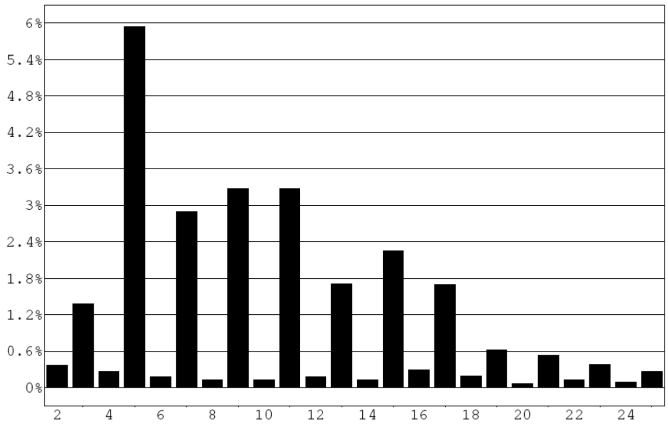

Fig. 17 – Harmonic magnitude as a percentage of the fundamental amplitude.

The efficiency curve was plotted with D=0.5 and D=0.8 as shown in Figure 18. Due to current limitations, D=0.5 curve haven't achieved 100W. In order to verify efficiency improvement, the circuit was also tested with complementary PWM control and redesigned snubbers. Efficiency curves can be seen on Figure 19. Efficiency improvement can be noticed due to the reduction of switching losses and the snubbers' losses with the use of the proposed technique.

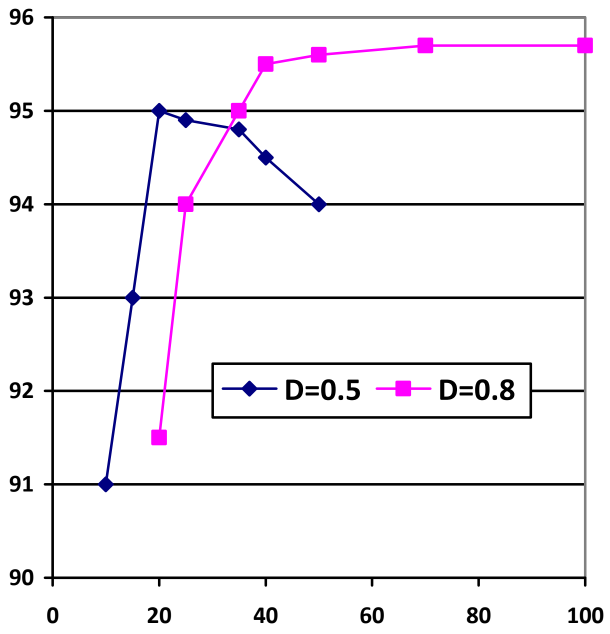

Figure 18 - Efficiency curves η[%] x P_O[W]

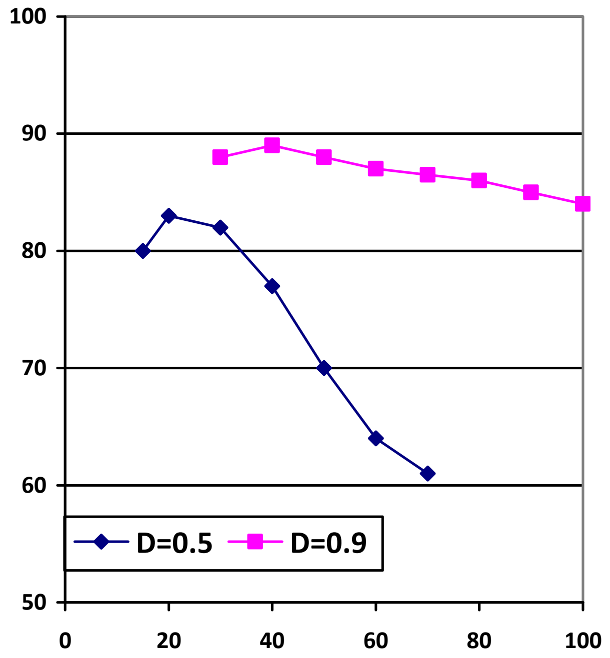

Figure 19 - Efficiency curves using bi-directional switches and with complementary command.
η[%] x P_O[W]

IV. CONCLUSIONS

High efficiency AC-AC conversion is obtained through the implementation of an AC-AC buck converter. Based on the results obtained from a 100W prototype, it is concluded that the converter can operate with high efficiency, slightly above 95%, when a simple control technique is applied. For future studies, higher efficiency can possibly be achieved if it is designed to operate at higher powers. The converter is suitable for applications such as temperature control, speed control and limitation of in-rush current in induction motors, voltage stabilizers, active filters and so on.

V. REFERENCES

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