**IEEE754 single precision floating point (f32) support Complex Adder**



f32_cpx_adder_0

| CLK | |
| RST | READY |
| Ar[31:0] | NAN |
| Ai[31:0] | INF |
| Br[31:0] | Rr[31:0] |
| Bi[31:0] | Ri[31:0] |
| EN | |

f32_cpx_adder_v1_0
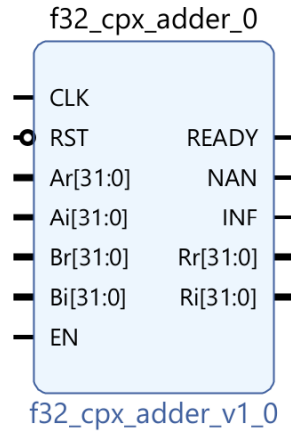
This IP computes addition of two complex inputs (Ar ± Ai) and (Br ± Bi) (in IEEE754 single precision floating point format). The result is also in the same format:

(Rr ± Ri) = (Ar ± Ai) ± (Br ± Bi)

Depending on the input value(s), the result can be NaN or Infinite. This case is shown by NAN and INF outputs.

All Input/Output descriptions can be found in the following table.

| Pin name | Description | Direction | Property |
|----------|-------------|-----------|----------|
| CLK | CLK input | IN | 1bit |
| RST | Reset input | IN | 1bit, active High |
| EN | Enable | IN | 1bit, active High |
| Ar | Real part of Addition operand-1 | IN | 32bit, IEEE754 single precision floating point format |
| Ai | Imaginary part of Addition operand-1 | IN | 32bit, IEEE754 single precision floating point format |
| Br | Real part of Addition operand-2 | IN | 32bit, IEEE754 single precision floating point format |
| Bi | Imaginary part of Addition operand-2 | IN | 32bit, IEEE754 single precision floating point format |
| Rr | Real part of Addition Result | OUT | 32bit, IEEE754 single precision floating point format |
| Ri | Imaginary part of Addition Result | OUT | 32bit, IEEE754 single precision floating point format |
| NAN | Result is not valid: NaN | OUT | 1bit, active High |
| INF | Result is not +/- Infinite | OUT | 1bit, active High |