Hw6

Sunday, November 1, 2015 4:32 PM

Instruction: AND Rd, Rs, Rt

Interpretation: Reg[Rd] = Reg[Rs] And Reg[Rt]

4.1.1

RegWrite	MemRead	ALU Mux	MemWrite	ALUop	RegMux	Branch
1	0	0	0	AND	1	0

4.1.2

PC, Register write port, Instruction Memory, Register Read port

Main ALU, PC Adder

4.1.3

Data Memory produces an output but is not used in this instruction

PC, Instruction Memory, Register read port, Main ALU, and PC Adder do not produce an output.

4.2

Instruction: LWI Rt, Rd(Rs)

Interpretation: Reg[Rt] = Mem[Reg[Rd] + Reg[Rs]]

4.2.1

PC, Instruction Memory, Register R Ports, Main ALU, Data Memory, Register Write PC Adder

4.2.2

None

4.2.3

None

4.3

4.3.1

I- Mem → Add → Mux → Regs → Control → ALU

400 + 100 + 30 + 200 + 100 + 120 = 95

I- mem → Add → ALU + MUX → Regs → Control →

400 + 100 + 300 + 200 + 100 = 1

4.3.2 $\frac{150}{1130} = .841$

4.3.3 I-mem → Add → 3 Mux → ALU → Regs → Control

1000 + 30 + 10 + 100 + 200 + 2000 + 500 = 3

$\frac{3,840}{4440} = .91 = 1.022$

It is more price effective with the improvement

Port

;0

Mux

;840

1,440