CS224

Lab 4

Section 5

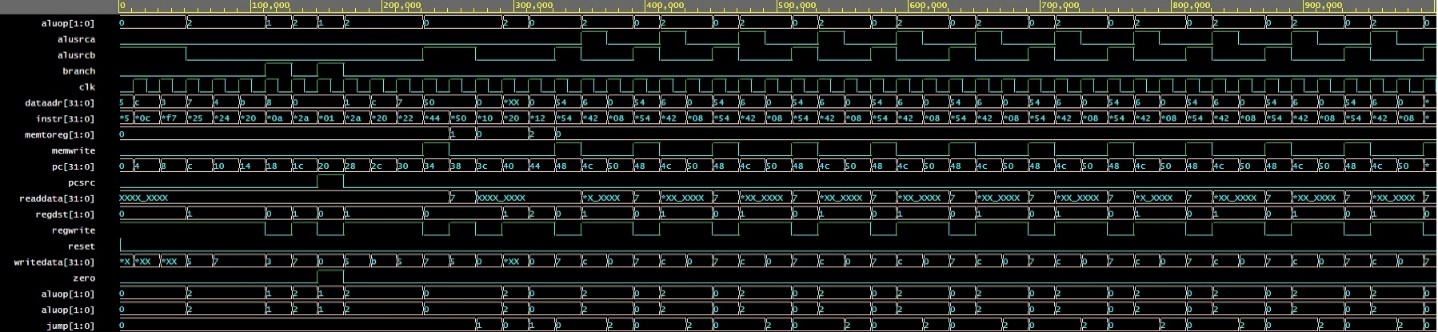
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a)

|  |  |  |
| --- | --- | --- |
| Location | Machine Instruction | Language Equivalent |
| 0x00400000 | 0x20020005 | addi $v0, $0, 5 |
| 0x00400004 | 0x2003000c | addi $v1, $0, 12 |
| 0x00400008 | 0x2067fff7 | addi $a3, $v1, -9 |
| 0x0040000c | 0x00e22025 | or $a0, $a3, $v0 |
| 0x00400010 | 0x00642824 | and $a1, $v1, $a0 |
| 0x00400014 | 0x00a42820 | add $a1, $a1, $a0 |
| 0x00400018 | 0x10a7000a | beq $a1, $a3, imem[17] |
| 0x0040001c | 0x0064202a | slt $a0, $v1, $a0 |
| 0x00400020 | 0x10800001 | beq $a0, $0, imem[0] |
| 0x00400024 | 0x20050000 | addi $a1, $0, 0 |
| 0x00400028 | 0x00e2202a | slt $a0, $a3, $v0 |
| 0x0040002c | 0x00853820 | add $a3, $a0, $a1 |
| 0x00400030 | 0x00e23822 | sub $a3, $a3, $v0 |
| 0x00400034 | 0xac670044 | sw $a3, 68($v1) |
| 0x00400038 | 0x8c020050 | lw $v0, 80($0) |
| 0x0040003c | 0x08000010 | j imem[16] |
| 0x00400040 | 0x001f6020 | add $t4, $0, $ra |
| 0x00400044 | 0x0c000012 | jal imem[18] |
| 0x00400048 | 0xac020054 | sw $v0, 84($0) |
| 0x0040004c | 0x00039042 | srl $s2, $v1, 1 |
| 0x00400050 | 0x03E00008 | jr $ra |

e)



f)

1- writedata corresponds to the register data of rt, which is instr[20:16]

2- Early parts of the program consists of only J-Type instructions and destination register is not available in these instructions.

3- Read data is available only when the reading from memory occurs and in these instruction set, reading only occurs when the lw is instructed.

4- Dataadr corresponds to the result of alu calculation.

5- When the instructions are over, the data memory are no longer getting new address.

g)

1- Since this code supports srl function, just the opcode of the function is needed to be added and alusrcA is needed to be changed.

2- The control unit is needed to be modified for sll function. Also, the shifter for left is needed to be added to datapath.

2)

a)

ble

IM[PC]

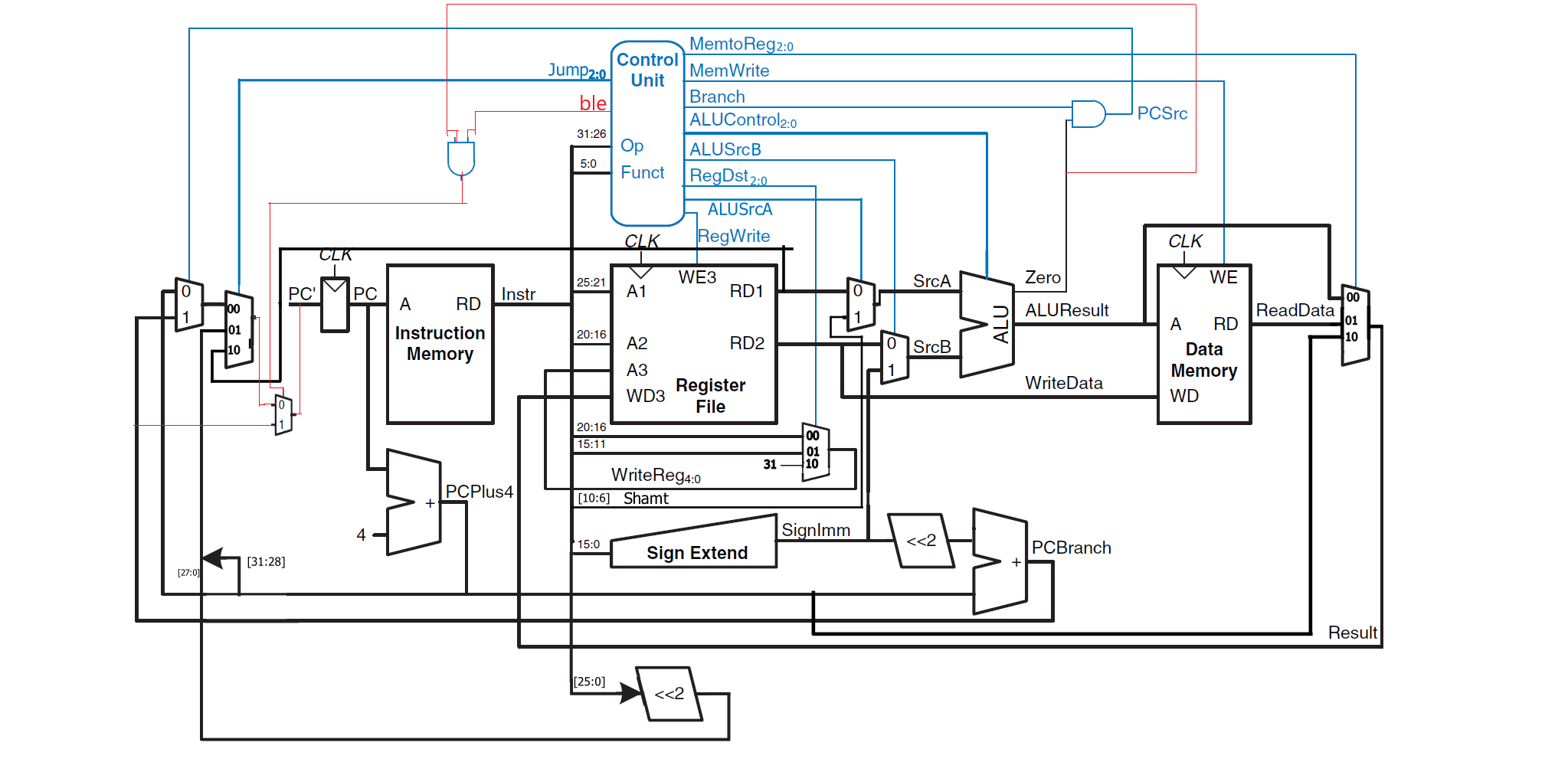
If (RF[rs] <= RF[rt])

PC <-PC + 4 + 4 \* SignExt (Address)

else

PC <-PC + 4

b)



Final Datapath with ble function

c)

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **Opcode** | **RegWrite** | **RegDst** | **ALUSrcA** | **ALUSrcB** | **Branch** | **MemWrite** | **MemToReg** | **ALUOp** | **Jump** | **Ble** |
| R-type | 000000 | 1 | 01 | 0 | 0 | 0 | 0 | 00 | 10 | 00 | 0 |
| srl | 000000 | 1 | 01 | 1 | 0 | 0 | 0 | 00 | 10 | 00 | 0 |
| lw | 100011 | 1 | 00 | 0 | 1 | 0 | 0 | 01 | 00 | 00 | 0 |
| sw | 101011 | 0 | X | 0 | 1 | 0 | 1 | XX | 00 | 00 | 0 |
| beq | 000100 | 0 | X | 0 | 0 | 1 | 0 | 01 | 01 | 00 | 0 |
| addi | 001000 | 1 | 00 | 0 | 1 | 0 | 0 | 00 | 00 | 00 | 0 |
| j | 000010 | 0 | X | X | X | X | 0 | XX | XX | 01 | 0 |
| jal | 000011 | 1 | 10 | X | X | X | 0 | 10 | XX | 01 | 0 |
| jr | 000000 | 1 | 01 | 0 | 0 | 0 | 0 | 00 | 10 | 10 | 0 |
| ble | 101100 | 0 | X | 0 | 0 | 0 | 0 | XX | 11 | 00 | 1 |

Main Decoder Table