

Practical Measurement of Voltage-Controlled Current Source Output Impedance for Applications in Transcranial Electrical Stimulation

Unabridged preprint

For the original paper and citation, please see Appendix

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Abstract

A voltage-controlled current source (VCCS) is a key component in the electrical stimulation of neuronal tissue. We present a method for the evaluation of output impedance across frequency, of VCCS circuits with applications in transcranial electrical stimulation (tES). Two VCCS circuit architectures, one with a single-ended, and one with a differential output, are theoretically analysed and simulated, and the method is validated by matching these results with empirical measurements. Monte Carlo simulation of the measurement method itself is used to predict its range of applicability under real-world conditions. Both circuits, as well as the method used to determine output impedance, are easy to reproduce, using generic hardware components at low cost. The method described has immediate practical application value in neuroscience research, where it can be used in the deployment and further development of VCCS circuit architectures.

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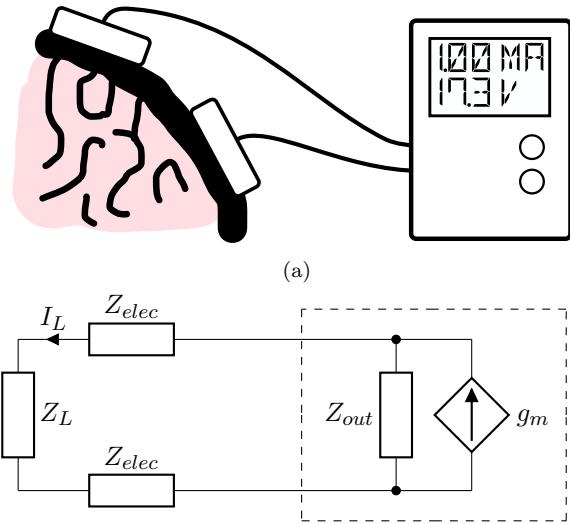


Figure 1: Situation sketch (top panel) and equivalent circuit (bottom panel). In a typical tES session, the device is adjusted to supply a given current I_L into a load Z_L via two electrodes, each with interfacial impedance Z_{elec} . We assume the device is battery powered or in any case galvanically isolated; the ground node is thus elided in the bottom panel.

1 Motivation

Transcranial electrical stimulation (tES) is a relatively non-invasive way of altering the excitability of the brain. A direct, alternating or noise current (tDCS, tACS or tRNS, respectively) is delivered between two electrodes that have been placed into conductive contact with the subject’s skin, on or near the scalp (Fig. 1, top). Bandwidth of the stimulation is typically below 1 kHz and currents are below 2 mA [1][2]. In addition to tES, voltage-controlled current sources are key components in other stimulation methods of the nervous system, such as Deep Brain Stimulation (DBS), where similar operating parameters are required [3].

There is a trend towards smaller electrodes in tES, which allow for controlling the stimulation at a higher spatial resolution [4]. Smaller electrodes have a higher electrode (electrode/electrolyte, or interfacial) impedance (Fig. 1, bottom), and thus in general need higher drive voltages to maintain the same current. Drive voltages can also be paradoxically high, even with common tES electrode sizes (on the order of 50 cm^2), for especially *low* currents. For tDCS at 2.5 mA, an extrapolated voltage swing of at least 18.3 V is required from the VCCS, “for the top 99th percentile” of subjects [5]; [6] report using values as high as 66.7 V.

To obtain larger output voltage swing, a VCCS with a differential output can be used. In a single-ended architecture, one of the electrodes is connected to ground, while the other is driven by the VCCS. In a differential design, instead, both sides are actively driven by the VCCS. This requires twice as many amplifiers or output drivers, but results in an effective doubling of the output voltage range when one side of the load is driven in antiphase with the

other. Further benefits include an improved signal bandwidth, immunity to changes in the load, and noise immunity [7].

Here, we present a universal, low-cost method to measure VCCS output impedance, to guide the design and empirical performance validation of any single-ended or differential output current source, in the operating regime that is typical for tES with human subjects. To improve the interpretability of obtained results, we selected two related circuits for evaluation, so that results may be compared on a relative basis. Each of these circuits is a variant of the well-known “improved Howland” current source, which can be built using commodity, off-the-shelf parts with low total cost, excellent performance, and large output voltage swing [8]. Howland sources require precise matching of resistor values to obtain good performance, which can be adequately addressed by trimming using a single potentiometer (or two in the case of the differential source). These features make them an excellent alternative to custom silicon where access to tooling, turnaround time, customisation or cost are of concern.

We begin with a mathematical analysis (Sec. 3) and simulation studies (Sec. 4), continue with empirical measurements (Sec. 5), and conclude in Sec. 6.

2 Previous work

A straightforward differential version of the Howland current source uses two of the exact same single-ended Howland current sources, one to drive the anode and one to drive the cathode. A common drive signal (the voltage indicating current setpoint) is connected to the positive-phase input of the anodal VCCS and the negative-phase input of the cathodal VCCS [9][10]. This configuration relies on the non-ideal (finite) output resistance of each current source to balance the two legs of the circuit, making it extremely sensitive to small variations in component values, causing an unacceptably large common-mode voltage.

A potential solution to the problem of imbalance is to use an active feedback circuit that nulls the common-mode voltage at the output [11]. This prevents one of the legs from floating to the supply rail. A disadvantage of this circuit is the large number of components used (7 op-amps and 14 precision resistors) and required matching.

The differential source in [7] is based on the single-ended improved Howland, but extends the circuit by two op-amps. A single-ended Howland source drives the anodal leg of the circuit as normal. A new pair of op-amps, configured as an inverting voltage follower, drive the cathode voltage to be equal and opposite to the anode voltage. This architecture was found to perform well in comparison to a normal, single-ended configuration, approximately doubling the differential output impedance over a wide frequency range. This design shows a differential but not symmetric output, which could affect noise rejection to external interference, because the cathode terminal output impedance will be different from the anode terminal output impedance. Frequency compensation of the voltage follower can introduce additional instabilities.

Another family of circuits is based around the use of a fully differential output op-amp [12][13], which have the advantage of very small common-mode output voltage.

A fully differential circuit similar to the improved Howland was described in [14]. One op-amp is connected to the anode of the load through a sense resistor, and a second op-amp connects to the cathode through a second sense resistor. The net negative feedback to one op-amp is then given by the voltage drop

over the sense resistor on the opposite leg. This circuit is fully symmetrical and requires only two standard op-amps and six precision resistors. In the remainder of this paper, we use this circuit as a benchmark.

3 Analysis

Throughout the analysis and results sections, we compare a single-ended with a differential VCCS using a common set of measurements. This allows us to distinguish the relative performance gained by changing to a differential architecture from the absolute performance, which is affected by implementation details such as selection of the op-amp IC.

In this section, we analytically determine the gain, compliance voltage and predicted output resistance for the single-ended version, followed by the differential circuit. Derivations were carried out with the help of Wolfram Mathematica [15].

3.1 Single-ended “improved” Howland VCCS

The improved Howland circuit is based on a standard op-amp and five precision resistors. It is a single-ended circuit, meaning one side of the load is connected to ground (Fig. 2). The operation of the circuit can be understood as follows: there is both negative feedback (via R_2) and positive feedback (via R_{4a}). The difference between positive and negative feedback is proportional to the load current (via the ratio R_2/R_{4b}). No current flows into the input terminals of the op-amp, so the same difference in current exists between R_1 and R_3 . But as $V_{pos} = V_{neg}$ in normal operation, these currents are in turn proportional to the input voltage $V_{in, pos} - V_{in, neg}$. Thus, overall, the load current is proportional to the input voltage.

3.1.1 DC analysis

Let A_{OL} be the (finite) gain of the op-amp. The input-output relationship of the op-amp can be written as

$$V_o = A_{OL} \cdot (V_{pos} - V_{neg}) \quad (1a)$$

To derive the gain of the VCCS, we start by applying Kirchhoff’s Current Law (KCL) to node V_{pos} and V_{neg} :

$$\frac{V_{in, pos} - V_{pos}}{R_3} - \frac{V_{pos} - V_L}{R_{4a}} = 0 \quad (1b)$$

$$\frac{V_o - V_{neg}}{R_2} - \frac{V_{neg} - V_{in, neg}}{R_1} = 0 \quad (1c)$$

Similarly we apply KCL to the output node V_L :

$$\frac{V_o - V_L}{R_{4b}} + \frac{V_{pos} - V_L}{R_{4a}} - I_L = 0 \quad (1d)$$

For a given load Z_L , and assuming $A_{OL} = \infty$, combining Eq. 1a—Eq. 1d yields the transfer function of the VCCS:

$$\frac{I_L}{V_{in, diff}} = \frac{1}{2} \cdot \frac{R_2(R_3 + 2R_{4a}) + R_1(R_{4a} + R_{4b})}{R_2R_3Z_L - R_1(R_3R_{4b} + R_{4b}Z_L + R_{4a}(R_{4b} + Z_L))} \quad (2)$$

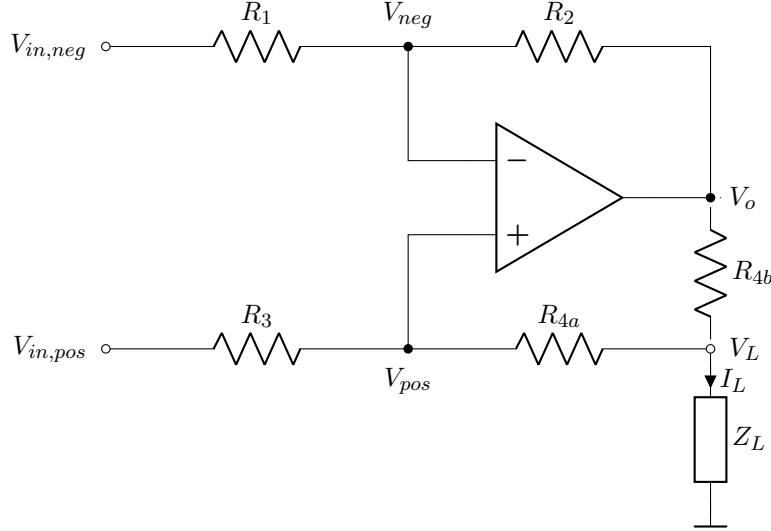


Figure 2: Circuit diagram of the single-ended “improved” Howland source. Z_L is the load impedance external to the VCCS.

with $V_{in,diff} = V_{in,pos} - V_{in,neg}$. Under the conditions that

$$A_{OL} = \infty \quad (3a)$$

$$R_1 = R_3 \quad (3b)$$

$$R_2 = R_{4a} + R_{4b} \quad (3c)$$

Eq. 1a—Eq. 1d simplify such that the output current does not depend on output voltage (i.e. the V_L -dependent term vanishes). The transfer function can then be written as:

$$I_L = g_m \cdot V_{in,diff} \quad (4a)$$

with

$$g_m = \frac{R_2}{R_3 R_{4b}} \quad (4b)$$

the transconductance of the VCCS in units of Ampère per Volt.

3.1.2 Output resistance

Ideally, the output resistance of a VCCS is infinite. In practice, it attains only a finite value, due to limitations of the op-amp, and imperfect matching of the resistors (violations of Eq. 3 and Eq. 12). An expression for output impedance can be obtained by taking the partial differential of the output voltage with respect to the output current:

$$\begin{aligned} Z_{out} &= \frac{\partial V_L}{\partial I_L} \\ &= -\frac{\alpha + A_{OL} \cdot \beta}{\gamma + A_{OL} \cdot \delta} \end{aligned} \quad (5)$$

with

$$\begin{aligned}\alpha &= (R_1 + R_2)(R_3 + R_{4a})R_{4b} \\ \beta &= R_1(R_3 + R_{4a})R_{4b} \\ \gamma &= (R_1 + R_2)(R_3 + R_{4a} + R_{4b}) \\ \delta &= R_1(R_{4a} + R_{4b}) - R_2R_3\end{aligned}$$

which is indeed infinite under the conditions given by Eq. 3.

Note that for certain combinations of values, the output resistance can exhibit a negative sign. In this case, load current will increase with increasing load resistance. Intuitively, it is a consequence of the positive feedback in the circuit (via R_{4a}) being too strong with respect to the negative feedback (via R_2). This situation, where positive feedback dominates, could theoretically cause instability. The magnitude of the effect is in the form of a transconductance with magnitude (“differential gain”) equal to $1/|Z_{out}|$. Thus, for a circuit where the resistors are reasonably well matched, Z_{out} is very high and this gain is infinitesimal.

3.1.3 Compliance voltage

The compliance voltage (maximum output voltage span) is in practice limited by the saturation voltage of the op-amp $V_{sat,pp}$ (e.g. 28 V for a ± 15 V op-amp), and the voltage drop across the series resistor R_{4b} caused by I_L , while the contribution of the positive feedback path (through R_{4a}) is negligible:

$$|V_L| \leq V_{sat,pp} - R_{4b}|I_{L,max}| \quad (6)$$

To obtain the largest output voltage swing, R_{4b} should be chosen as small as possible, taking other constraints on the circuit into account.

3.2 Differential version of the “improved” Howland VCCS

To actively drive both sides of the load, the differential version uses two op-amps and six precision resistors (Fig. 3). It operates in a manner analogous to the single-ended version, the voltages in the bottom half having equal magnitude but opposite sign from the top half at all times. For each of the halves, the positive part of the feedback is now obtained via the negative input terminal of the op-amp. This is achieved by obtaining the feedback voltage from the other side of the circuit, where it has an inverted sign (this is the X-shaped crossing in the circuit). R_1 and R_3 in the differential circuit are analog to R_2 in the single-ended version, conveying negative feedback. R_{2a} and R_{4a} are analogous to R_{4a} in the single-ended circuit and convey what is effectively positive feedback because of the sign inversion.

3.2.1 DC analysis

Starting again with the definition of an op-amp with finite gain A_{OL} :

$$V_a = A_{OL} \cdot (V_{in, pos} - V_{a, neg}) \quad (7a)$$

$$V_b = A_{OL} \cdot (V_{in, neg} - V_{b, neg}) \quad (7b)$$

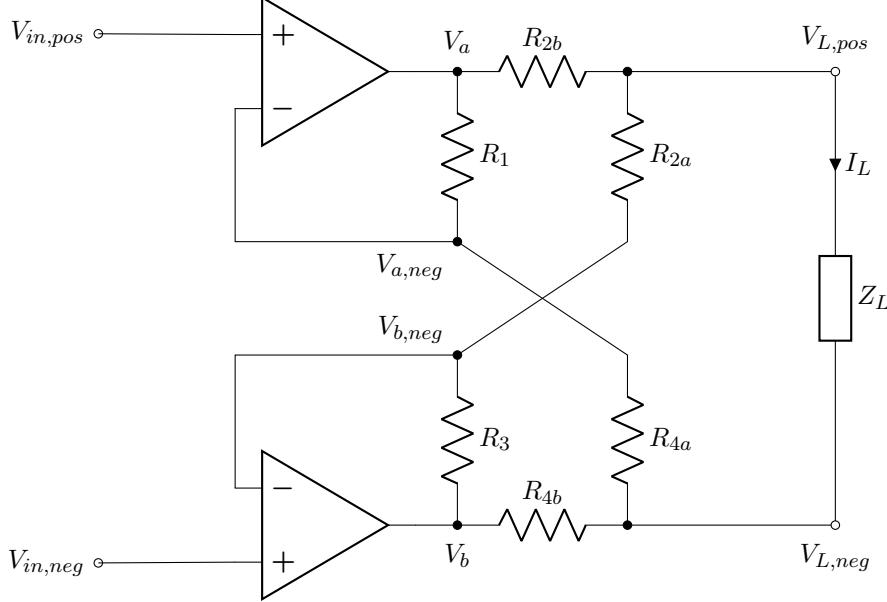


Figure 3: Circuit diagram of the fully differential “improved” Howland source. Z_L is the load impedance external to the VCCS.

Apply KCL to nodes $V_{L, pos}$ and $V_{L, neg}$:

$$\frac{V_a - V_{L, pos}}{R_{2b}} - \frac{V_{L, pos} - V_{b, neg}}{R_{2a}} - I_L = 0 \quad (8a)$$

$$\frac{V_b - V_{L, neg}}{R_{4b}} - \frac{V_{L, neg} - V_{a, neg}}{R_{4a}} + I_L = 0 \quad (8b)$$

Apply KCL to nodes $V_{a, neg}$ and $V_{b, neg}$:

$$\frac{V_a - V_{a, neg}}{R_1} + \frac{V_{L, neg} - V_{a, neg}}{R_{4a}} = 0 \quad (9a)$$

$$\frac{V_b - V_{b, neg}}{R_3} + \frac{V_{L, pos} - V_{b, neg}}{R_{2a}} = 0 \quad (9b)$$

In addition, we use the auxiliary equation for the differential output voltage V_L :

$$V_L = V_{L, pos} - V_{L, neg} \quad (10)$$

For a given load Z_L , and assuming $A_{OL} = \infty$, combining Eq. 7–Eq. 10 yields the transfer function:

$$\frac{I_L}{V_{in, diff}} = \frac{R_1(R_{2a} + R_3) + R_{4a}(R_{2a} + R_3) - R_{2b}R_{4b}}{\left(Z_L((R_{2a} + R_{2b})(R_{4a} + R_{4b}) - R_1R_3) + R_{2a}(R_{4b}(R_1 + R_{4a}) + R_{2b}(R_{4a} + R_{4b})) + R_{2b}R_{4a}(R_3 + R_{4b}) \right)} \quad (11)$$

Under the conditions that

$$R_{2b} = R_{4b} \quad (12a)$$

$$R_{2a} = R_{4a} \quad (12b)$$

$$R_1 = R_3 = R_{2b} + R_{2a} \quad (12c)$$

$$V_{in, pos} = -V_{in, neg} \quad (12d)$$

Eq. 7–Eq. 10 simplify such that the output current does not depend on output voltage (i.e. the V_L term vanishes). The transfer function can then be written as:

$$I_L = g_m \cdot V_{in, diff} \quad (13a)$$

with

$$g_m = \frac{1}{R_{2b}} \quad (13b)$$

3.2.2 Compliance voltage

The main limiting factor of the compliance voltage is, as before, the saturation voltage of the op-amp, and secondly, the voltage drop across (in this case not one but two) resistors R_{2b} and R_{4b} (with $R_{2b} = R_{4b}$). If resistor values are chosen to be equal (see Tbl. 1), this yields a compliance voltage twice that of the single-ended variant:

$$|V_L| \leq 2(V_{sat, pp} - R_{2b}|I_{L, max}|) \quad (14)$$

3.2.3 Output resistance

The differential output resistance:

$$\begin{aligned} R_{out} &= \frac{\partial V_L}{\partial I_L} \\ &= \frac{\alpha + A_{OL} \cdot \beta}{\gamma + A_{OL} \cdot \delta} \end{aligned} \quad (15)$$

with

$$\begin{aligned} \alpha &= (R_{4b} + R_{4a} + R_1)(R_{2b} + R_{2a} + R_3) \\ \beta &= (R_{2b} + R_{2a})(R_{4b} + R_{4a}) - R_1 R_3 \\ \gamma &= R_{4b}(R_{4a} + R_1)(R_{2a} + R_3) \\ &\quad + R_{2b}((R_{4a} + R_1)(R_{2a} + R_3) + R_{4b}(R_{4a} + R_{2a} + R_1 + R_3)) \\ \delta &= R_{4b}R_{2a}(R_{4a} + R_1) + R_{2b}(R_{4b}(R_{4a} + R_{2a}) + R_{4a}(R_{2a} + R_3)) \end{aligned}$$

which is indeed infinite under the conditions given by Eq. 12 and $A_{OL} = \infty$.

4 Simulation results

4.1 Monte Carlo simulation of DC output resistance

To compare the output resistance attainable by both designs, we run a Monte Carlo simulation of the effect of mismatches. For each iteration of the Monte Carlo algorithm, we sample resistance values for all resistors in the circuit from a uniform distribution, centered upon a mean and within a 0.1% tolerance range.

Single-ended		Differential	
R_1, R_2, R_3	10.25 kΩ	R_1, R_3	10.25 kΩ
R_{4a}	10 kΩ	R_{2a}, R_{4a}	10 kΩ
R_{4b}	250 Ω	R_{2b}, R_{4b}	250 Ω

Table 1: Component values used in all simulations and prototypes. The given combinations of values result in a gain $A = 4 \text{ mA/V}$ for both circuits.

The mean value for each resistor is given in Tbl. 1; these values are consistently used throughout simulations and prototyping. After sampling, output resistance is calculated according to Eq. 5 (single-ended) or Eq. 15 (differential). The open-loop gain of all op-amps is here assumed to be infinite ($A_{OL} = \infty$).

For approximately half of the resistor value permutations, the sign of the output resistance is positive, while in the other half it is negative (see discussion in Sec. 3.1.2). The resulting distribution is symmetric around 0. To allow for a more concise plot, we consider only the absolute value $|R_{out}|$.

A histogram of attained output resistance is plotted in Fig. 4. For ease of visual comparison, the output resistance of the differential VCCS is scaled by a factor $\frac{1}{2}$. The distributions for the single-ended and (scaled) differential output resistance are almost indistinguishable, demonstrating that for the same tolerance rating of the resistors, output resistance of the differential supply will be expected to be twice as high as that of the single-ended supply.

4.1.1 Tradeoff between VCCS gain and output impedance

Although it is not immediately clear from comparing the expressions for gain and output impedance (Eq. 4 and Eq. 5 for single-ended; Eq. 13 and Eq. 15 for differential), there is a negative relationship between achieved output impedance and VCCS gain. This can easily be demonstrated numerically, by running the Monte Carlo script of Fig. 4 for different values of gain, and measuring the

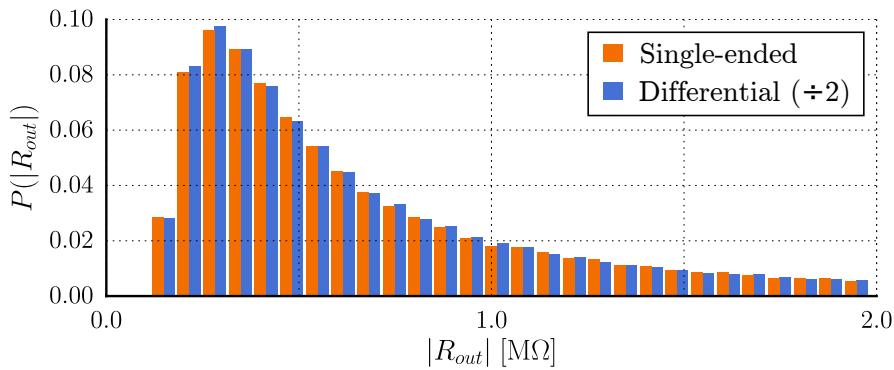


Figure 4: Monte Carlo simulation of absolute single-ended and differential DC output resistance for a resistor tolerance of 0.1% and $A_{OL} = \infty$. For each VCCS type, 10^5 samples were generated and it was assumed in both cases that the op-amp gain $A_{OL} = \infty$. Note that the output resistance of the differential VCCS is twice as high as the single-ended VCCS but is scaled by a factor $\frac{1}{2}$ in this plot to allow easier visual comparison.

location of the peak of the distribution. The resulting plot illustrates the tradeoff between gain and output impedance (Fig. 5). In the differential VCCS, gain can only be changed by changing the value of R_{2b} , so only one line is shown (blue diamonds). For the single-ended VCCS, gain can be changed in different ways: by changing the value of R_3 (orange circles, continuous line), or the value of R_{4b} (orange circles, dashed line).

In all further simulations and experiments, we use a constant set of resistor values (Tbl. 1) to obtain a gain of 4 mA/V for each VCCS, which yields practical voltage levels and places us in the middle range of the curves in Fig. 5.

4.2 A practical method for measuring output impedance

The output impedance of a current source can be measured by the following method [7]. A voltage $V_{in,diff}$ is applied to the VCCS corresponding to a current of 1 mA AC peak, that is, $I_L = 1 \text{ mA} \cdot \sin(2\pi ft)$. We then measure the load voltage $V_L = V_{L,pos} - V_{L,neg}$ and actual current delivered to the load I_L , under two conditions. Initially, a load $R_{L,a}$ is connected (Fig. 6). The corresponding load voltage and current are denoted $V_{L,a}$ and $I_{L,a}$, respectively. The load is then changed to $R_{L,b}$, and again the load voltage $V_{L,b}$ and current $I_{L,b}$ are measured. The output impedance Z_{out} can then be derived by circuit analysis:

$$Z_{out} = \frac{R_{L,a}R_{L,b}(V_{L,b} - V_{L,a})}{V_{L,a}R_{L,b} - V_{L,b}R_{L,a}} \quad (16a)$$

$$= \frac{I_{L,b}R_{L,b} - I_{L,a}R_{L,a}}{I_{L,a} - I_{L,b}} \quad (16b)$$

The voltage-based (Eq. 16a) and current-based (Eq. 16b) forms are mathematically equivalent. However, when performing empirical measurements, the practical measurement of V_L or I_L (Sec. 4.2.1) needs to be taken into consideration, as well as the tolerance in probe resistor values (Sec. 4.2.2).

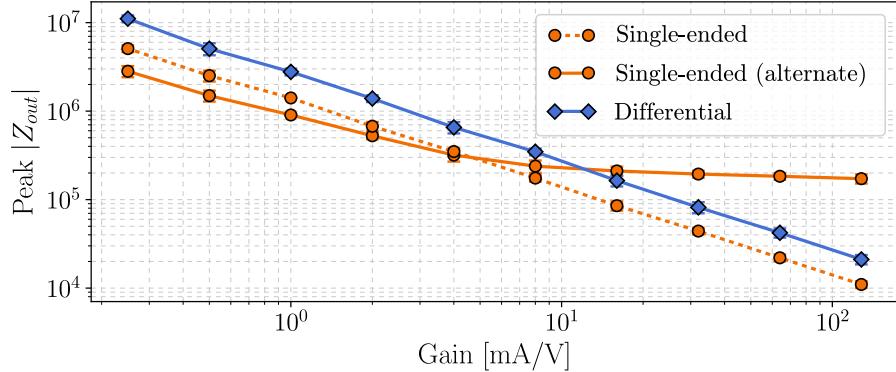


Figure 5: A doubling of VCCS gain reduces the attained output impedance by half. Vertical axis shows the location of the peak of the distribution in Fig. 4 for different values of VCCS gain (horizontal axis). The base values were picked for a gain of 4 mA/V.

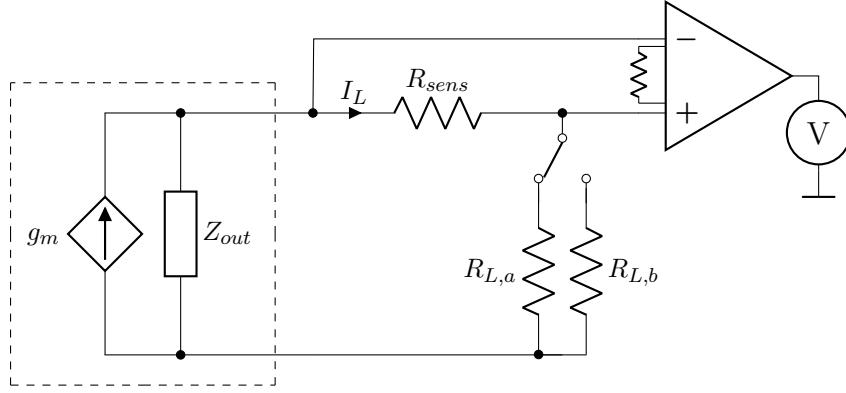


Figure 6: Method for determining the output impedance of the VCCS. The dashed box indicates the non-ideal VCCS, which has a finite output impedance Z_{out} . As in Fig. 1, the ground node is assumed internal to g_m .

4.2.1 Proxy measurement of output impedance

When the output impedance of the VCCS reaches into the dozens of $M\Omega$, high precision instrumentation is required to obtain enough significant digits. In addition, the measurement is affected by the non-ideal behaviour of the opamps, which causes Z_{out} to be a finite, complex and frequency-dependent value.

Although either form of Eq. 16 thus requires the measurement of a complex load voltage (or current), in practice only the (scalar) magnitude is available with sufficient accuracy and precision. If we substitute magnitudes into Eq. 16, we obtain an expression for a new, real-valued quantity \hat{Z}_{out} (Eq. 17), which is equal to the true magnitude $|Z_{out}|$ at DC, but begins to diverge for increasing frequency:

$$\hat{Z}_{out} = \frac{R_{L,a}R_{L,b}(|V_{L,b}| - |V_{L,a}|)}{|V_{L,a}|R_{L,b} - |V_{L,b}|R_{L,a}} \quad (17a)$$

$$= \frac{|I_{L,b}|R_{L,b} - |I_{L,a}|R_{L,a}}{|I_{L,a}| - |I_{L,b}|} \quad (17b)$$

The quantity \hat{Z}_{out} can be used to determine the full, complex output impedance Z_{out} , under the assumption that Z_{out} can be modeled as a resistor R_{out} in parallel with a capacitor C_{out} . In this case, $|V_L|$ can be written as:

$$|V_L| = g_m V_{in,diff} \frac{R_L \| R_{out}}{\sqrt{1 + (\omega(R_L \| R_{out})C_{out})^2}} \quad (18)$$

This expression is substituted into Eq. 17a, yielding a theoretical prediction for \hat{Z}_{out} as a function of frequency, parameterised by R_{out} and C_{out} . The resulting curves exhibit a typical RC lowpass filter shape, with plateau and roll-off (see solid lines in Fig. 13 for examples).

4.2.2 Effects of probe resistor tolerance

Measurement artefacts may be introduced as a consequence of tolerance in the component values of $R_{L,a}$ and $R_{L,b}$. For example, at DC, let $R_{L,a} = 10\text{ k}\Omega$.

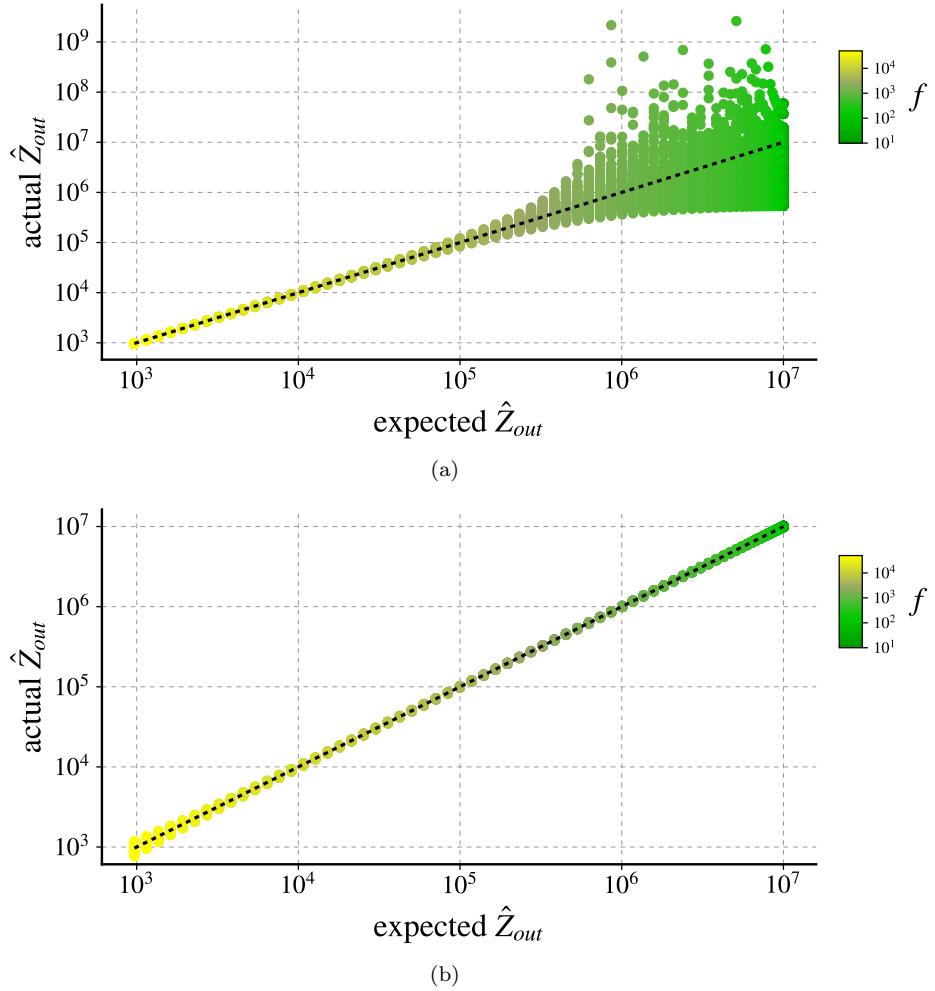


Figure 7: Sensitivity of the measured \hat{Z}_{out} to tolerance of the probe resistors $R_{L,a}$ and $R_{L,b}$, for voltage-based method (top) and current-based method (bottom). For each point, colour indicates the frequency at which it was measured; impedance drops at higher frequencies due to the presence of C_{out} .

If $R_{L,b}$ is assumed to be 11 k Ω , but its actual in-circuit value is 15 Ω larger, then a 1 M Ω output resistance will be reported as 2.8 M Ω by the voltage-based method (a relative error of 280%), but as 0.985 M Ω by the current-based method (a relative error of only 1.5%).

To quantify the artefact magnitude across frequency f , we sample values for $R_{L,a}$ and $R_{L,b}$ from a uniform distribution, centered upon a mean of 10 k Ω resp. 11 k Ω , and within a 0.1% tolerance range. An output capacitance of 1 nF is assumed. We compute an ‘‘expected’’ \hat{Z}_{out} , on the basis of ideal load resistors, and an ‘‘actual’’ \hat{Z}_{out} , based on the samples. The actual value (vertical axis) is then plotted with respect to the expected value (horizontal axis). If the measurement were completely insensitive to tolerance in the resistors, the actual value would be precisely the same as the expected value, causing all points to fall exactly on the diagonal, indicated by the dashed black lines in Fig. 7. Any vertical offset between a point and the diagonal corresponds to the measurement

artefact introduced by tolerance in the probe resistors.

The voltage-based method (Fig. 7, top panel) is most sensitive to variations in probe resistor values there where it matters most: in the region of highest output impedance. This makes it an unsuitable method for measuring the output impedance of a current source, which is generally characterised by high output impedance. The current-based method (Fig. 7, bottom panel) also suffers from sensitivity to probe resistance, but this occurs at higher frequency and consequently at values of \hat{Z}_{out} that are so low as to be outside the range of interest for a VCCS.

4.3 SPICE simulation of output impedance

We used LTSPICE [16] to simulate the three circuits, and calculate complex output impedance by Eq. 16b. An op-amp model was used that characterises the op-amp by a few key parameters (Sec. A), listed in Tbl. 2. Model parameter values were chosen to match real-world values in order of magnitude. Some parameters were ignored or assumed infinite (e.g. maximum output current, slew rate).

Results are shown in Fig. 8. Below 1 MHz, the differential VCCS outperforms the single-ended version by a factor of 2. This is in line with the results of the Monte Carlo simulation.

Note that there is a tradeoff between output impedance and VCCS gain: in general, increasing the gain (by picking different resistor values) yields a lower (worse) $|R_{out}|$, and vice versa. For example, if the gain of the differential (but not the single-ended) VCCS is doubled (by picking its $R_{2b} = R_{4b} = 500 \Omega$ and re-dimensioning remaining resistors to satisfy the conditions in Eq. 12), then it will achieve the same R_{out} as the single-ended version, across all frequencies and for all conditions shown in Fig. 8.

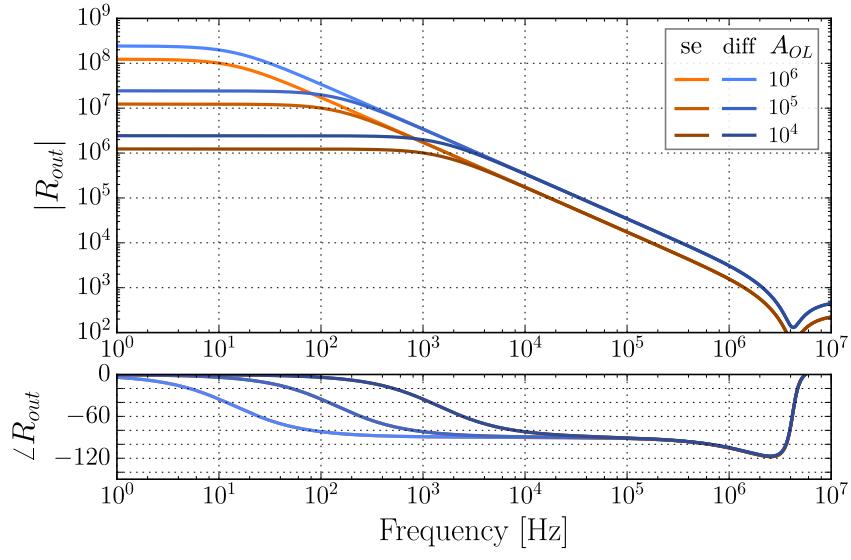
4.4 Loop stability and compensation

4.4.1 Preliminaries

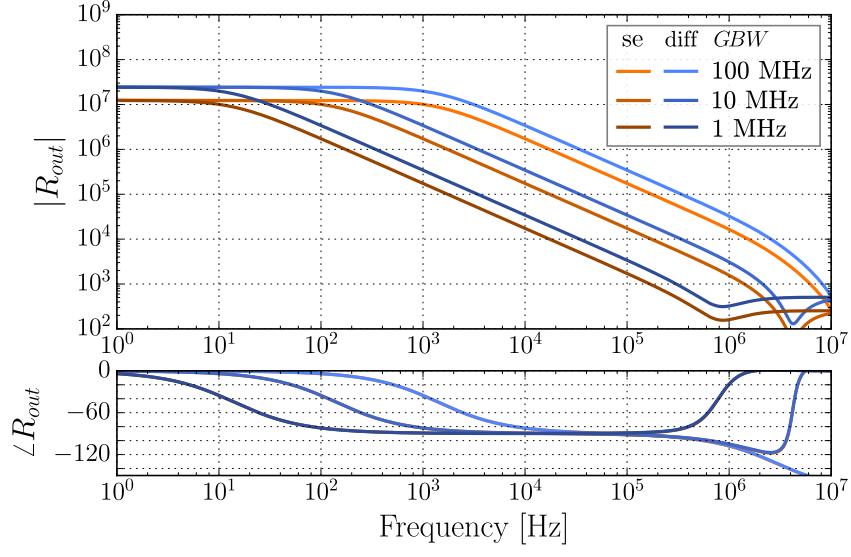
Loop stability refers to the propensity of the VCCS to oscillate, overshoot or otherwise respond poorly to transients in load impedance or input voltage. A medical or research setting where a human subject is connected to the VCCS

Symbol	Name	Value (LT1211)	Value (simulation)
A_{OL}	open-loop gain	1200 V/mV	1000 V/mV
GBW	gain-bandwidth product	14 MHz	10 MHz
SR	slew rate	7 V/ μ s	∞
R_{in}	input resistance	40 M Ω	100 M Ω
C_{in}	input capacitance	10 pF	10 pF
R_{out}	output resistance	75 Ω	10 Ω
PM	phase margin	60°	55°

Table 2: Op-amp parameters used for all LTSPICE simulations, unless stated otherwise. Values pertaining to the LT1211 were extracted from the datasheet [17].



(a)



(b)

Figure 8: Output impedance (plotted as magnitude $|R_{out}|$ and phase $\angle R_{out}$) of the single-ended (“se”) and differential (“diff”) VCCS. LTSPICE simulation. **Top:** parameter sweep across op amp open-loop gain A_{OL} (between 10 V/mV and 1000 V/mV). **Bottom:** parameter sweep across op amp gain-bandwidth product GBW (between 1 MHz and 100 MHz).

places very high demands on stability. At the same time, the human subject presents a challenging load. In circuit terms, interfaces between the electrodes and skin, as well as biological processes in the living tissue, yield a potentially very large capacitive effect, the magnitude of which depends on current frequency and amplitude [18][19][20]. Furthermore, when DC stimulation is

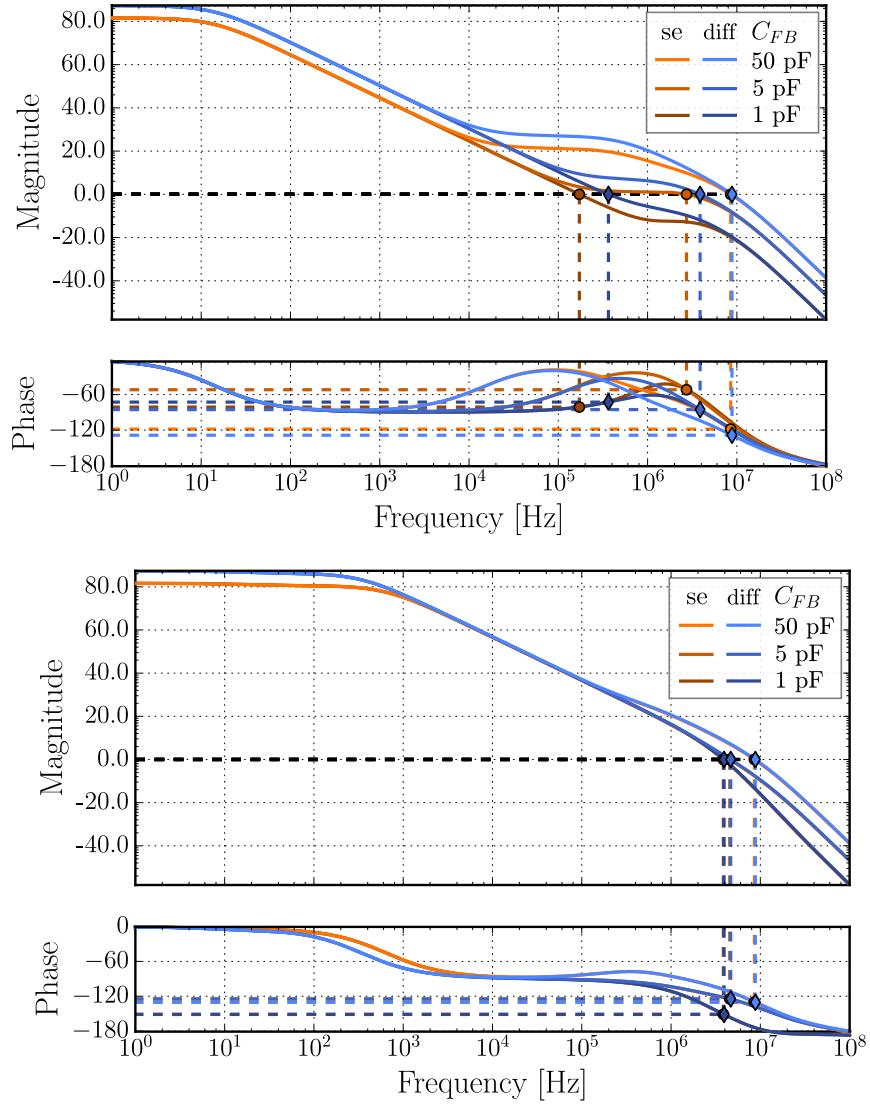


Figure 9: Loop gain of the single-ended (“se”) and differential (“diff”) VCCS. **Top:** purely resistive load ($R_L = 10 \text{ k}\Omega$). **Bottom:** capacitive load ($Z_L = 10 \text{ k}\Omega \parallel 1 \mu\text{F}$). Dashed lines indicate the method for reading off phase margin (see main text for details).

applied, galvanic processes can occur [18] that change the electrical properties of the interface as a function of stimulation parameters such as current direction (cathodic vs. anodic) and amplitude. These processes are typically highly nonlinear. An ideal VCCS will remain stable under all load conditions.

Loop stability is often expressed in terms of *phase margin*, which refers to the following oscillation criterion for any feedback circuit: the loop gain has to have a magnitude of 1 and a phase shift of 360° in order for the circuit to (potentially) oscillate. The phase margin, then, is defined as the difference between the actual loop phase and 360° , at the frequency where the loop gain

equals 0 dB. A typical minimum acceptable phase margin is 60°, with a higher number indicating better stability. The relationship between phase margin and time-domain phenomena such as overshoot and ringing are only well-defined for second-order systems, and become an approximation for higher order systems. We therefore validate the frequency-domain simulations with time-domain transient simulations (Sec. 4.4.5).

4.4.2 ‘Lead’ compensation method

Lead compensation introduces a zero into the transfer function of the feedback circuit. Typically, the op-amp is modeled by means of two poles, each of which introduces 90° of phase lag. The zero due to the compensation circuit is then placed near the highest pole, cancelling part of the lag—hence the name lead compensation. Lead compensation is simple (it introduces only one extra parameter in the circuit) but considerably reduces the circuit bandwidth.

In the single-ended VCCS, lead compensation is implemented by placing a feedback capacitor C_{FB} parallel to R_2 (see Fig. 2). In the differential VCCS, two feedback capacitors $C_{FB,1} = C_{FB,2} = C_{FB}$ are placed in parallel with R_1 and R_3 , respectively (see Fig. 3).

4.4.3 Simulation method

To evaluate the performance of the VCCS circuits with and without compensation, we use the Middlebrook method in LTSPICE. Briefly, this involves alternately inserting a voltage source and a current source into the feedback loop, each with a very small AC magnitude, so as to not disturb the DC setpoint of the circuit. The Middlebrook technique maintains a closed loop, thereby minimally disturbing normal circuit operation. The purpose of the inserted sources is to probe the response of the circuit to the injected voltages and currents. For this purpose, voltages and currents are measured on all ports of the inserted sources. The loop gain can then be derived by means of a simple algebraic expression [21].

For differential-output VCCS, we are interested in the differential-mode loop response, and use two ideal baluns [22] to convert between balanced and unbalanced signals. The baluns are inserted back-to-back at the place where we wish to insert the Middlebrook sources; here, immediately following the output of each op-amp. The first balun converts the balanced VCCS output to an unbalanced output, i.e. a separate differential-mode and a common-mode path. Middlebrook sources are then inserted into the differential path, and a second balun converts back to balanced output.

4.4.4 Simulation results: loop gain

To understand how lead compensation affects stability, we run our simulations with a range of values for C_{FB} between 1 and 100 pF. Additionally, to study the effect of different load conditions, the load capacitance C_L is made to vary between 0 (purely resistive load) and 1 μF . Load capacitance is presented in parallel with a constant 10 k Ω resistor, so that $Z_L = C_L \parallel R_L$.

In Fig. 9, the simulated loop gain is plotted in terms of magnitude and phase, for two load conditions (top panel: purely resistive; bottom panel: $C_L = 1 \mu\text{F}$). The method for reading off phase margin (of the circuit, not the op-amp property) is indicated by dashed lines: first, find the frequency at which the loop gain magnitude equals one (black horizontal line). At this frequency, read off

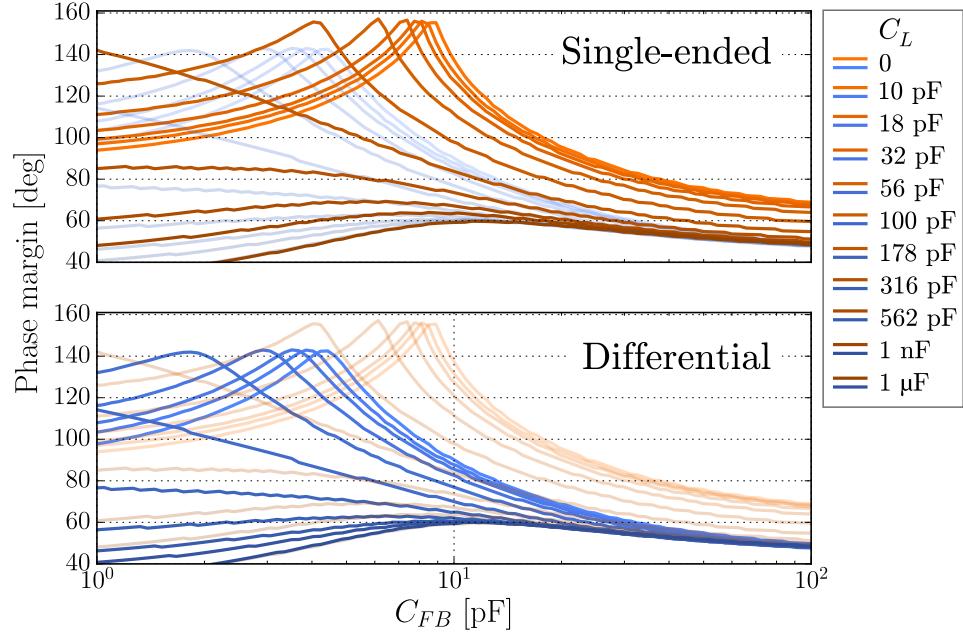


Figure 10: Phase margin (PM) obtained for an op-amp with parameters as given in Tbl. 2, with the exception of $GBW = 5$ MHz. To find the optimal C_{FB} , we simulate the PM for various loading conditions: R_L is a constant $10\text{ k}\Omega$, while C_L varies between zero and $1\text{ }\mu\text{F}$. The optimal C_{FB} can then be read from the diagram by finding the point on the horizontal axis where the PM is maximal.

the loop gain phase (horizontal coloured lines); the phase margin PM is then -180° minus this number. Intersections are marked for convenience (circles: single-ended; diamonds: differential).

At DC, the loop gain of the differential supply is twice that of the single-ended supply (≈ 87 and 81 dB, respectively). We note that this will, generally speaking, make compensation easier for the single-ended supply, because lower gain tends to shift the 0 dB point to lower frequencies, where, in the absence of compensation, the phase margin is larger.

The two lowest-frequency poles of the op-amp are responsible for two inflection points around 10 Hz and 10 MHz . The effect of increasing C_{FB} is seen as an increase in the 0 dB -frequency, and an associated boost in phase. Adding a substantial load capacitance (bottom panel) worsens the phase margins across the board, as expected. The obtained phase margins indicate that under some conditions, the differential VCCS outperforms the single-ended supply, whereas in other conditions, the situation might be reversed.

In general, we wish to pick the optimal C_{FB} , that leads to the best (highest) PM . The existence of a particular “optimal” C_{FB} is suggested by the non-monotonic relationship between C_{FB} and PM (see e.g.: Fig. 9, bottom panel: the best PM is achieved by the intermediate value of the feedback capacitor).

To investigate this relationship in more detail, we performed a parameter sweep across C_{FB} and plotted the phase margin obtained in each case (Fig. 10). These curves indeed show a clear optimum, which for the differential supply occurs at approximately half the capacitance compared to the single-ended sup-

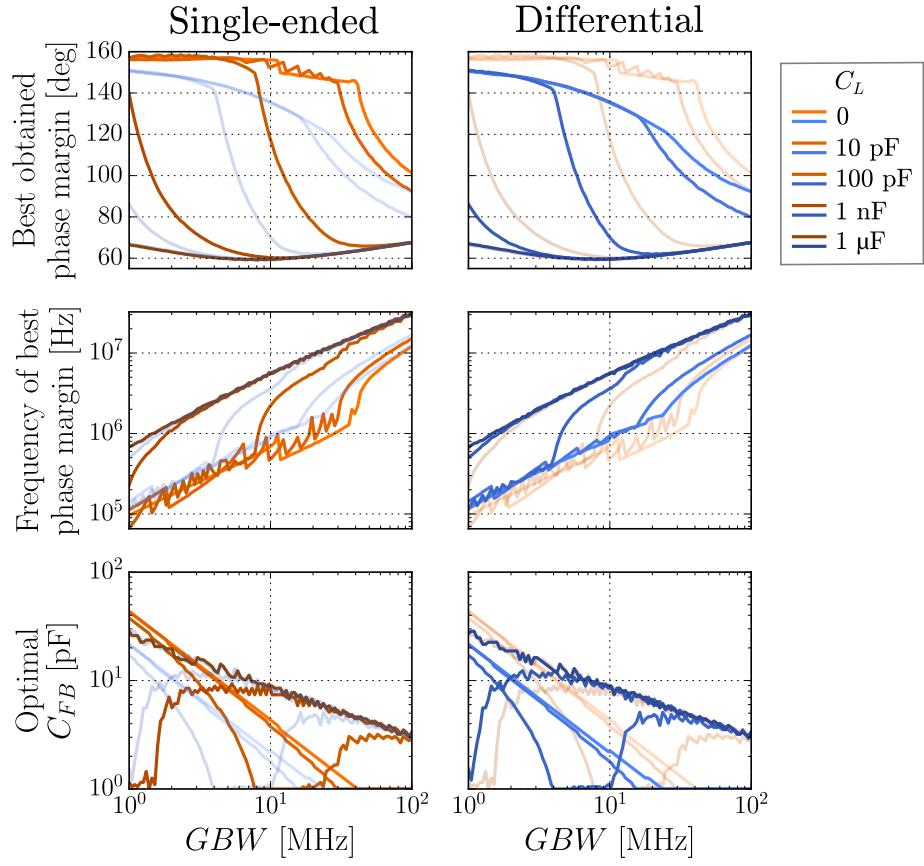


Figure 11: Phase margins versus the op-amp GBW parameter, for various values of C_L .

ply. For the same op-amp parameters and load, the differential supply can thus achieve a higher bandwidth. As the load capacitance increases, however, the optima of both circuits converge to approximately 10 pF.

The plots in Fig. 10 were made for a fixed GBW . To better understand the relationship between GBW and phase margin, we perform peak detection to identify the optimal C_{FB} for each loading condition in Fig. 10. We then sweep GBW and plot, again for various load conditions, the best system performance that can be achieved (i.e. by picking the optimal C_{FB}).

Results are shown in Fig. 11. The general trend is that a higher GBW increases the frequency of the best achieved phase margin, and decreases the optimal C_{FB} . A higher VCCS bandwidth can thus indeed be achieved by picking an op-amp with higher GBW . Loop stability, however, suffers, as the achieved phase margins tend to be lower for higher GBW . It is thus in general easier to achieve stable operation for lower GBW , especially in the face of capacitive loading. For loads where the capacitance does not dominate the resistance, the differential supply outperforms the single-ended supply by offering more bandwidth.

4.4.5 Time-domain transient validation

Predictions on the basis of loop gain should always be validated by time-domain transient testing. The transient should, ideally, not perturb the DC setpoint of the circuit. We apply a small-signal pulse to $V_{in,diff}$ so that a step occurs from 0.2475 V to 0.25 V, corresponding to a change in requested current from 0.99 mA to 1 mA. The corresponding transient in actual delivered output current is simultaneously measured, and inspected for signs of overshoot and ringing.

The transient response test is performed for a range of load capacitance values between zero and 1 μF . As before, the load capacitor is in parallel with a load resistor of 10 $\text{k}\Omega$. All op-amp parameters are as in Tbl. 2. Under these conditions, we can read off the optimal C_{FB} from the bottom two panels in Fig. 11 as 9 pF in both cases (single-ended and differential). We round the value to the nearest whole number, befitting the magnitude of numerical noise (e.g. discretisation errors, finite sweep resolution). According to formulas Eq. 2 and Eq. 11, this places the -3 dB point around 80 kHz for both circuits under resistive load, well above the maximum frequencies typically used in tES.

The time-domain response is shown in Fig. 12 (left panel). The output current magnitude exhibits considerable overshoot for the differential, but not the single-ended circuit, in spite of the compensation. The underlying cause is the imbalance in driving impedance between the op-amp inverting and noninverting inputs. In the differential circuit, the non-inverting op-amp inputs are both driven by ideal voltage sources, whereas the inverting inputs are connected to the rest of the circuit via resistors on the order of 10 $\text{k}\Omega$. Combined with stray capacitance at the op-amp inputs, this results in a low-pass RC filter for the inverting but not the non-inverting inputs.

To compensate for this effect, we add a 10 $\text{k}\Omega$ resistor in series with each non-inverting input. The right panel of Fig. 12 shows that the inclusion of these resistors indeed eliminates the overshoot. Note that the steady-state curves for single-ended and differential circuits no longer precisely overlap, indicating a slight DC offset due to the interaction between the added resistors and the finite input resistance at each op-amp input (here, 10 $\text{M}\Omega$; see Tbl. 2).

4.4.6 Out-of-the-loop compensation method

Initial simulations showed that the best achieved phase margin at the most demanding loading condition is below the minimum acceptable. A simple and robust way to improve PM is to isolate the VCCS from capacitive loading by inserting one (for single-ended) or two resistors (for differential) in series with the load. These resistors are inserted between the output terminal(s) of the VCCS and the load.

The downside of this method is that we incur an extra (Ohmic) voltage drop. As an example, say that we pick a value of 100 Ω for the series resistors. The voltage drop will be 0.5 and 1 V for the single-ended and differential supplies, respectively, at the maximum output current $I_L = 5$ mA. The phase margin is considerably improved, by approximately 15° , and is achieved at a lower value of C_{FB} , thereby improving bandwidth. These series resistors were not included in any of the reported results, but their inclusion in the final tES application circuit is strongly recommended to provide an additional safety margin.

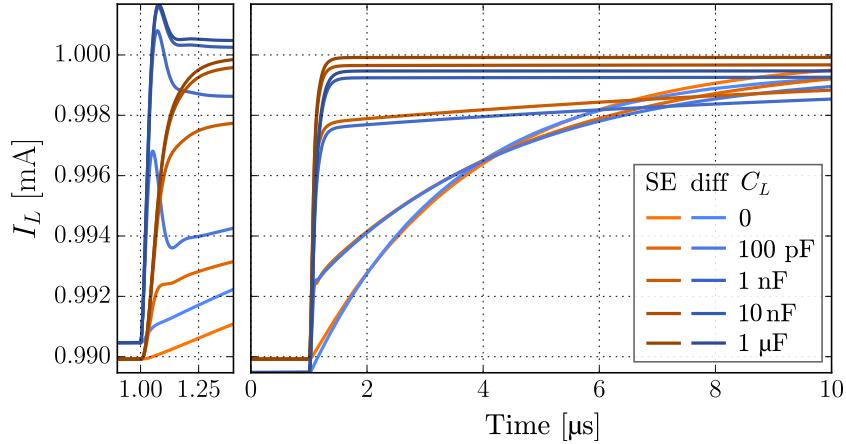


Figure 12: Transient response to a step function at $t = 1 \mu\text{s}$ corresponding to a change in requested current from 0.99 mA to 1 mA. The trend is that higher load capacitance leads to a faster response in actual delivered current. **Left:** detailed view showing overshoot and ringing (mostly) for the differential but not the single-ended VCCS, in the case that no extra precautions are taken. **Right:** overview of response demonstrating that additional input resistors eliminate the overshoot (see discussion in Sec. 4.4.5).

5 Empirical results

5.1 Description of the prototypes

Two prototype circuits were built to validate predictions from theory and simulation with empirical measurements. Circuits were constructed using surface-mount devices in SOIC-8 and 1206 ($3.2 \times 1.6 \text{ mm}$) packages on a 1.6 mm dual layer FR-4 PCB with a ground plane on the bottom layer. Devices were battery-powered with a linearly regulated bipolar supply of $\pm 15 \text{ V}$.

5.1.1 Component selection

Selection criteria for the op-amp include wide output voltage swing, high current drive capability, a high gain-bandwidth product and otherwise excellent characteristics (offset voltages and currents, distortion, noise, etc.) The op-amp used in the prototypes is the Linear Technology LT1211 (dual op-amp in a SOIC-8 package) [17]. In the single-ended circuit, the second op-amp in the package is not used, and is wired as a voltage follower with its noninverting input tied to ground. This was done in order to obtain the best possible match between the testing conditions of each circuit.

All fixed resistors used in the circuit were rated at a tolerance of 0.1%. Some of the resistors were implemented as the series connection of a fixed resistance and a potentiometer to allow for trimming (see Sec. 5.2). The 250Ω fixed resistors were implemented as the parallel connection of a 300Ω and $1.5 \text{ k}\Omega$ resistor. The $10.25 \text{ k}\Omega$ fixed resistors were implemented as the parallel connection of two $20.5 \text{ k}\Omega$ resistors.

Feedback capacitors were picked according to the methods of Sec. 4.4. When the parameters of the LT1211 are entered, the optimum values returned by the simulation are approximately 5.5 pF for the single-ended, and 3.0 pF for

the differential circuit. We round these to the standard component values of $C_{FB} = 3.3$ pF (for the differential circuit) and $C_{FB} = 6.6$ pF (for the single-ended circuit: implemented as the parallel connection of two 3.3 pF capacitors).

5.1.2 Input drive signal

The inputs of each VCCS were driven in antiphase, such that $V_{in,neg} = -V_{in,pos}$ at all times.

Note that the single-ended VCCS presents a more demanding load to the circuit driving its input terminals, because the input driver needs to supply the nonzero current that flows through resistors R_1 and R_3 . The output impedance of the driver appears in series with these (precision) resistors and can cause Eq. 3 to be violated. For this reason, an additional dual op-amp (LT1211) was used in the single-ended VCCS as a unity gain input buffer. Numerical simulation confirmed that the impact of the buffer on the overall AC response of the (combined) circuit is negligible. The differential VCCS does not present the disadvantage of needing an additional input buffer; its input impedance is already very high, equal to twice the impedance at the noninverting op-amp input.

5.1.3 Measuring output current

To measure actual delivered current, an instrumentation amplifier (INA128U, Texas Instruments, USA) was set up to measure voltage drop across a $10\ \Omega$ resistor R_{sens} placed in series with the load (Fig. 6). The instrumentation amplifier was configured for a gain of 51, so a current of 1 mA yields a measured voltage of 0.51 V. For a 6-digit multimeter, this in turn yields a maximum theoretical measurable output impedance of $510\ M\Omega$. Higher gain will improve the highest measurable impedance, but reduces the highest measurable frequency (here, 100 kHz) due to the finite gain-bandwidth product of the instrumentation amplifier.

5.2 Trimming procedure

To trim output resistance, R_2 in the single-ended, and R_1 and R_3 in the differential circuit were implemented as the series connection of a fixed resistor and a trimmer potentiometer. Trimming was performed as follows. The VCCS was set for a DC current of 1 mA. Two loads were alternately applied to the source: a short circuit, and a $10\ k\Omega$ resistor. The actual delivered current was measured, and the trimmer potentiometer was adjusted until these values converged. For the differential source, the trimming potentiometers were alternately adjusted in small increments until convergence.

All reported values throughout this paper were obtained using the same, fixed trim.

5.3 Measurement of output impedance

To measure output impedance, the current-based method (Eq. 17b) was used as described in Sec. 4.2. Resistor values $R_{L,a} = 10\ k\Omega$ and $R_{L,b} = 11\ k\Omega$ were selected to obtain an output voltage close to the compliance voltage, and for having a relatively small difference between them while taking finite measurement precision into account.

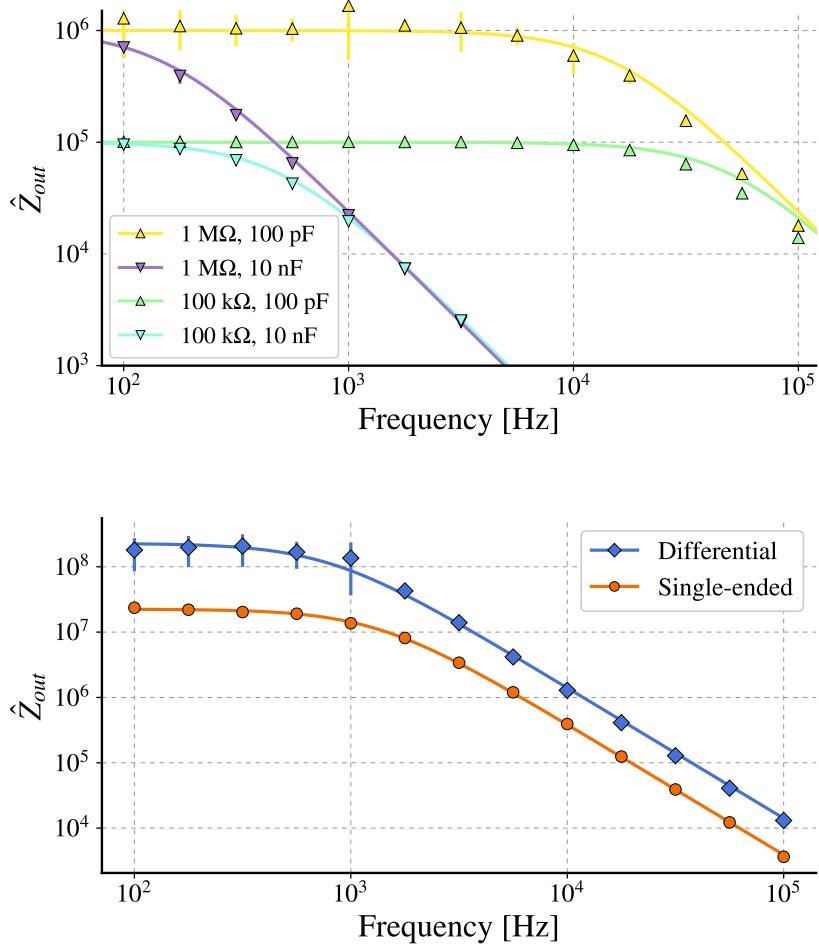


Figure 13: Empirical output resistance measurements for reference loads (top panel) and single-ended and differential VCCS circuits (bottom panel). Error bars due to measurement noise are plotted for each datapoint, but are visible only for the highest impedances.

A Hewlett-Packard 33120A function generator generates the input drive signal $V_{in,diff}$. To convert the single-ended output voltage into a differential voltage for driving the VCCS, a battery-powered unity gain buffer using a fully differential output op-amp was used.

A Hewlett-Packard 3456A 6-digit digital voltmeter was used for data acquisition. Samples were acquired at a rate of 1 Hz via GPIB interface on a GNU/Linux host computer. The voltmeter was connected to the output of an instrumentation amplifier as described in Sec. 5.1 to acquire readings for I_L . Samples which resulted in $\hat{Z}_{out} = \infty$ were discarded. This setup allowed us to reliably measure output resistance up to about 100 MΩ (see variance bars in Fig. 13).

The function generator and voltmeter were set up for automated data acquisition via the IEEE 488 (“GPIB”) instrument bus. To allow easy switching between load resistances, R_L was implemented as the series connection of a

	Single-ended	Differential
R_{out}	22.5 MΩ	249 MΩ
C_{out}	245 pF	131 pF

Table 3: Fitted values for resistive and capacitive components of the output impedance.

10 kΩ and 1 kΩ resistor, both with a tolerance of 0.1%, and a relay that short-circuits the 1 kΩ resistor when activated.

The method was first validated using a reference circuit with known values. A function generator (sinusoidal voltage source) with 50 Ω output impedance was connected in series with a resistor of known value: 100 kΩ or 1 MΩ. This is the Thévenin equivalent of a current source with an output resistance of the same value. Simultaneously, this “current source” was loaded with a load capacitance $C_L = 100 \text{ pF}$ or 10 nF , simulating the output capacitance C_{out} . This “current source” was then characterised using the same method. Results are shown in the top panel of Fig. 13. In this figure, empirical data is represented as points, while predicted values, based on the known R_{out} and C_{out} , are plotted as solid lines. The limit of voltmeter resolution is especially visible in the 1 MΩ condition, due to the large Ohmic voltage drop resulting in a very small load current. Overall, a good match between the empirical data and theoretical predictions can be observed, validating the accuracy and precision of our methodology.

Next, the VCCS prototypes were characterised. The bottom panel of Fig. 13 shows both the empirical measurements (as points), and the theoretical prediction based on curve fitting (as solid lines). To perform curve fitting, the Nelder-Mead algorithm [23] was used to find the R_{out} and C_{out} that minimise an error measure, defined as the squared difference between the (base 10) logarithm of the predicted, and logarithm of the empirical $\hat{Z}_{out}(f)$, summed over all measured frequencies f . Fitting was done independently for each circuit. Overall, good agreement between empirical data and the fitted curves is observed in Fig. 13, supporting the resistive-capacitive model of VCCS output impedance. Results of the fit are repeated in Tbl. 3 to allow a more precise quantitative comparison. The DC output resistance of the differential source is seen to outperform the single-ended source by a factor of more than 2, exceeding the improvement that was predicted based on theory in Sec. 4.1. Because we trim each circuit towards the singularity point where R_{out} approaches infinity, sensitivity to trim near this point is extremely high, explaining the variance. In contrast, the capacitive part of the output impedance C_{out} comes much closer to a factor 2 improvement from the single-ended to the differential circuit. This can be attributed to the high-frequency behaviour being dominated by the C_{FB} capacitors, which were chosen a factor of 2 different in value.

5.4 Transfer function and bandwidth

The transfer function (Fig. 14) is plotted on the basis of three data sources for comparison: the analytic formulas (Eq. 2, Eq. 11), numeric (LTSPICE) simulation, and empirical data. Simulations were run using the op-amp parameters in Tbl. 2; differences caused by switching to the built-in LTSPICE LT1211 model were negligible. Note that the analytic formulas assume an ideal op-amp and consequently overestimate the frequency response. When an ideal op-amp

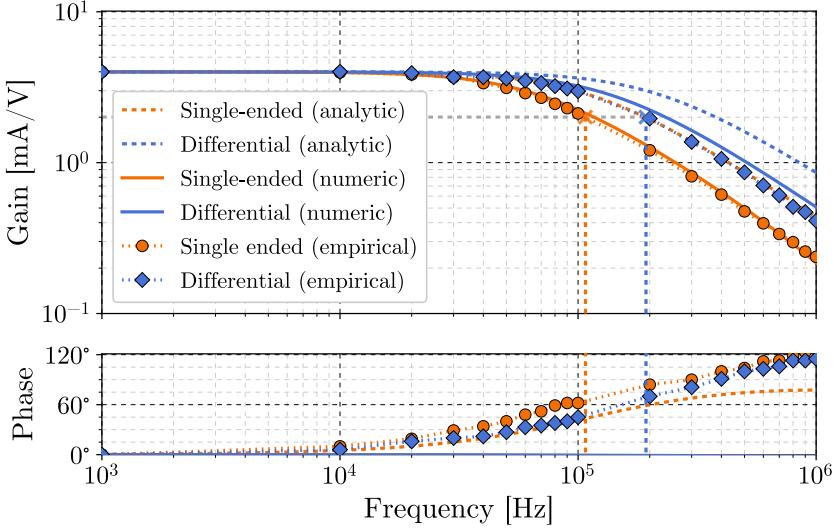


Figure 14: Bode plot. $R_L = 10 \text{ k}\Omega$

is used in simulation, the analytic curves overlap precisely with the numeric curves.

Overall, the data shows a factor two improvement in cutoff frequency in the differential VCCS compared to the single-ended version. This corresponds to the choice of a C_{FB} twice as high for the single-ended circuit compared to the differential circuit (see Sec. 5.1). We additionally verified the factor two improvement in marginally stable circuits with $C_{FB} = 0$ (data not shown).

5.5 Harmonic distortion

The output spectra were measured while applying a sinusoidal input voltage at 100 Hz to $V_{in,diff}$, such that $I_{L,peak} = 1 \text{ mA}$. The actual delivered current was measured at the output of one of the instrumentation amplifiers, acquired for 300 seconds, and saved as a 32 bit float uncompressed wave file. After windowing with a 4-term Blackman-Harris window, the Fourier transform of the signal was obtained and normalised to precisely 1 mA at 100 Hz.

If the output of a nonlinear system, such as a non-ideal VCCS, is differential rather than single-ended, all even harmonic terms (at even multiples of 100 Hz) cancel out. The second harmonic (at 200 Hz) was indeed found to be approximately 6 dB smaller in the differential than in the single-ended circuit (Fig. 15). The third harmonic (odd, at 300 Hz) and higher harmonics are also visible, and appear of approximately equal magnitude in both circuits.

The total harmonic distortion (THD) of an amplifier is defined as a magnitude ratio between the load current $I_{L,fund}$ at the fundamental, and the load current $I_{L,n}$ at each harmonic (for $n \geq 2$):

$$THD = \frac{\sqrt{(\sum_{n=2}^{\infty} I_{L,n})}}{I_{L,fund}}$$

Data was acquired using a U24XL 24-bit USB DAC/ADC at a sampling

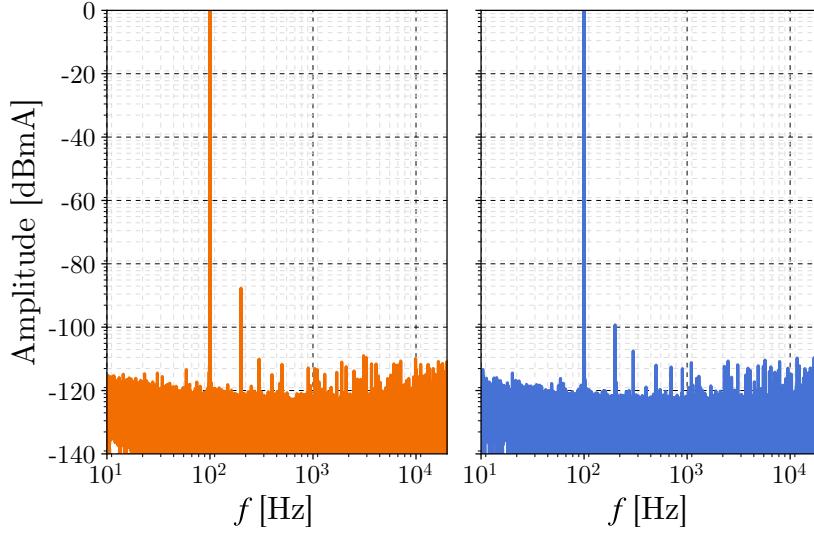


Figure 15: Spectrum of I_L for a 100 Hz sine input at $V_{in,diff}$ such that $I_L = 1$ mA.

rate of 48 kHz. Harmonics beyond the third are close to the noise floor of the experimental setup, and do not contribute significantly to the THD value (see Fig. 15). THD was therefore calculated based on the second and third harmonics (Tbl. 4). The differential supply improves over the single-ended circuit by a factor of more than three.

5.6 Common-mode rejection ratio (CMRR)

Common-mode rejection ratio (CMRR) is a measure of the immunity of the VCCS to a signal that appears simultaneously on the positive and negative input terminals. To account for a CMRR less than infinity, an extra term is added to Eq. 13 to account for common-mode gain A_{cm} in addition to the differential gain A_d (corresponding to A in the original equation):

$$I_L = A_d \cdot (V_{in,pos} - V_{in,neg}) + A_{cm} \cdot \frac{V_{in,pos} + V_{in,neg}}{2} \quad (19)$$

The CMRR is then defined as (in units of decibel):

$$\text{CMRR} = 20 \cdot \log_{10} \left(\frac{A_d}{|A_{cm}|} \right) \quad (20)$$

A sinusoidal common-mode signal was applied to both positive and negative phase inputs, with an amplitude such that, if one of the inputs were shifted in phase by 180°, the output current would be $I_L = 1$ mA (peak).

The CMRR achieved was similar across circuits and across frequencies (Tbl. 5).

Single-ended	Differential
$4.1 \cdot 10^{-5}$	$1.2 \cdot 10^{-5}$

Table 4: Total Harmonic Distortion (THD) based on second and third harmonics.

f	Single-ended	Differential
100 Hz	54 dB	53 dB
10 kHz	51 dB	53 dB

Table 5: Common-mode rejection ratio achieved by each VCCS, at two tested frequencies.

5.7 Input transient response

To validate stability under real-world conditions, we performed a test using a square wave profile for the input voltage, corresponding to a current of $I_{L,peak} = 1 \text{ mA}$ into a $10 \text{ k}\Omega$ load. Measurements show a stable response without overshoot or ringing (Fig. 16). Adding a capacitor in parallel to the load resistor causes faster fall and rise times in I_L , because the output voltage does not need to swing as high to achieve the same load current, but no overshoot or ringing was observed (data not shown).

5.8 Load transient response

A second transient test was carried out to evaluate VCCS stability, by changing the load resistance while the input voltage $V_{in,diff}$ was kept constant, corresponding to $I_L = 1 \text{ mA}$. A $10 \text{ k}\Omega$ resistor was used as load, while a second 100Ω resistor was electrically inserted and removed, in parallel with the other resistor. The electrical switching was carried out by driving an opto-isolator (International Rectifier PVT412S [24]) with a square wave input and placing it series with the second resistor. When the opto-isolator is switched off (for low V_{ctrl} , see lower panel of Fig. 17), the total load resistance is $10 \text{ k}\Omega$, whereas for high V_{ctrl} , the load resistance drops to approximately 100Ω . These resistances were chosen so that the output voltage spans the full scale from $V_L = 10 \text{ V}$ to almost zero (Fig. 17, middle panel).

A step change in load resistance requires a step change in output voltage to maintain the same current. Because the voltage cannot change instantaneously, a momentary transient is observed in actual delivered output current (Fig. 17, top panel). When the load resistance decreases, the voltage is momentarily too low (for the given input voltage) and a transient undervoltage occurs around $t = 300 \mu\text{s}$. The delay between the change in V_{ctrl} (at $t = 100 \mu\text{s}$) and the

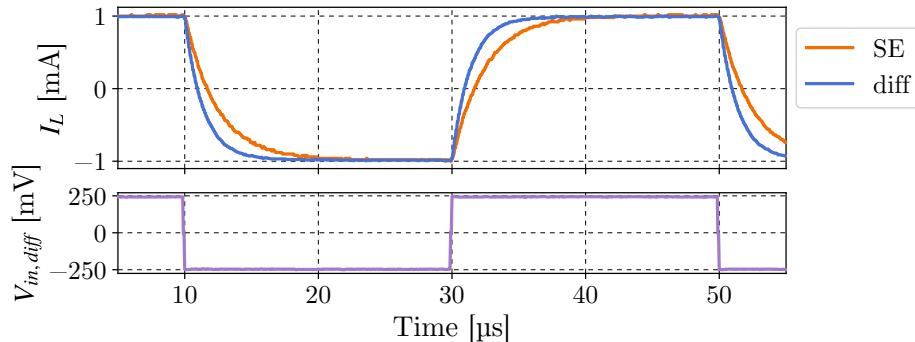


Figure 16: Transient response to a $f = 25 \text{ kHz}$ square wave at $V_{in,diff}$ with a $10 \text{ k}\Omega$ resistive load.

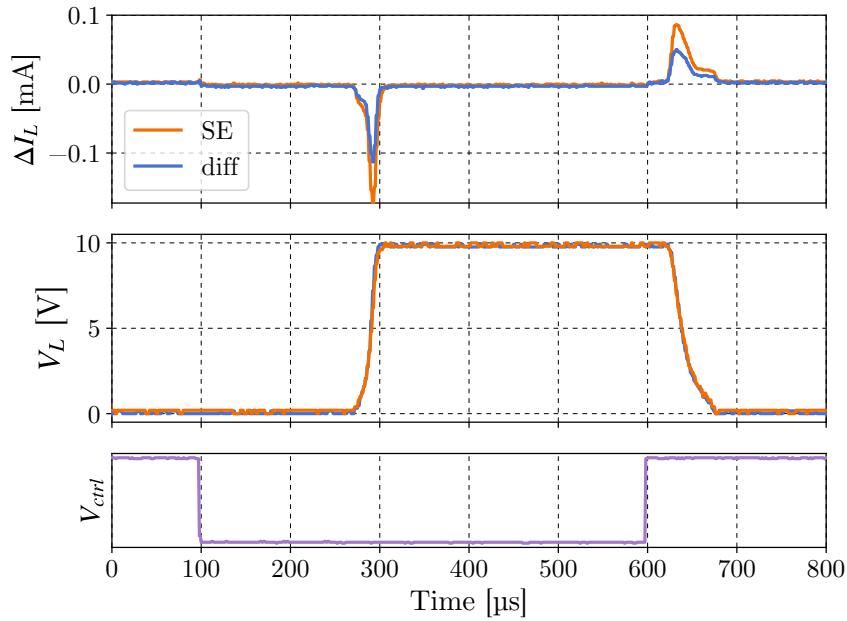


Figure 17: Transient response to a change in load resistance. Load resistance was alternated between $10\text{ k}\Omega$ (V_{ctrl} low) and 100Ω (V_{ctrl} high).

first observable response (around $t = 275\text{ }\mu\text{s}$) can be attributed to turn-off delay of the opto-coupler [24] (and likewise for the turn-on delay starting at $t = 600\text{ }\mu\text{s}$). The differential VCCS shows a roughly twofold improvement over the single-ended supply.

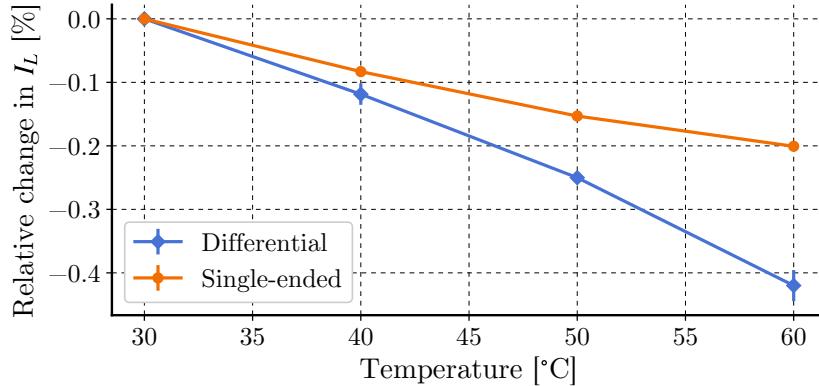


Figure 18: Temperature dependence of output current for a given input voltage. The temperature dependence was measured relative to a 1 mA current into a $10\text{ k}\Omega$ load at $30\text{ }^\circ\text{C}$. Error bars indicate standard deviation over 5 heating/cooling cycles.

5.9 Temperature sensitivity

Thermal drift is an undesirable property of a VCCS, where, in spite of a constant $V_{in,diff}$, the actual delivered current changes as a function of temperature.

The prototype, including the single-ended input buffer and current measuring instrumentation amplifiers, but not the load resistor, was heated from 30 °C up to 60 °C, while the actual current delivered was measured for a setlevel corresponding to $I_L = 1$ mA at the lowest temperature. All resistors used in the prototype have a temperature coefficient of 25 ppm.

LTSPICE simulation with ideal op-amps, but 25 ppm resistors, suggests that the temperature coefficient of the single-ended and differential circuits should be almost indistinguishable. Empirical results instead show a temperature coefficient about twice as large for the differential compared to the single-ended circuit (Fig. 18). The difference is attributable to non-ideal op-amp behaviour, such as input bias currents that are a function of temperature [17].

6 Conclusion

On the basis of analysis and simulation, we conclude that only the current-based method for measuring VCCS output impedance has practical application value (Sec. 4.2.2). In addition, we find empirically that we can infer the full, complex-valued Z_{out} on the basis of the proxy measurement of \hat{Z}_{out} (Sec. 4.2.1). Our method is suitable for VCCS circuits with a fully differential output, and was able to provide reliable data up to about 100 MΩ at frequencies up to 100 kHz.

The differential VCCS requires two potentiometers to be trimmed instead of one. Although the trimming process is relatively simple and only needs to be carried out once, we note that [25] use a digital potentiometer to automate the trimming process. The absence of resistors connected with one terminal to ground in the differential version complicates this method, but an analogous approach could in principle be used to avoid manual trimming.

In general, for electronics that is used *in vivo* in medicine or research, an abundance of caution should be exercised. A higher voltage range should be used with care; depending on operating conditions, keeping the voltage low can contribute to safety [26]. Output impedance measurement of the VCCS should be complemented by time-domain transient validation, temperature stability testing, common-mode output voltage measurements, and so on. Additional safety margins (such as on loop stability), low-current fuses and other passive and active protection mechanisms are crucial steps in going from the core VCCS circuit to a ready-to-use, clinical or research tES device, and indicate potential directions for future research.

A Op-amp model

We use a simple op-amp model with 7 parameters: input resistance R_{in} and capacitance C_{in} , open-loop voltage gain A_{OL} , output resistance R_{out} , and three poles with frequencies f_1, f_2 and f_3 (Fig. 19).

We find it convenient to define the gain-bandwidth product GBW as the frequency at which the open-loop op-amp gain equals 1. Most of the loss in gain at GBW (compared to A_{OL} at DC) is due to the first, low-frequency pole. We pick $f_2 = GBW$, which means that the gain is reduced by an additional

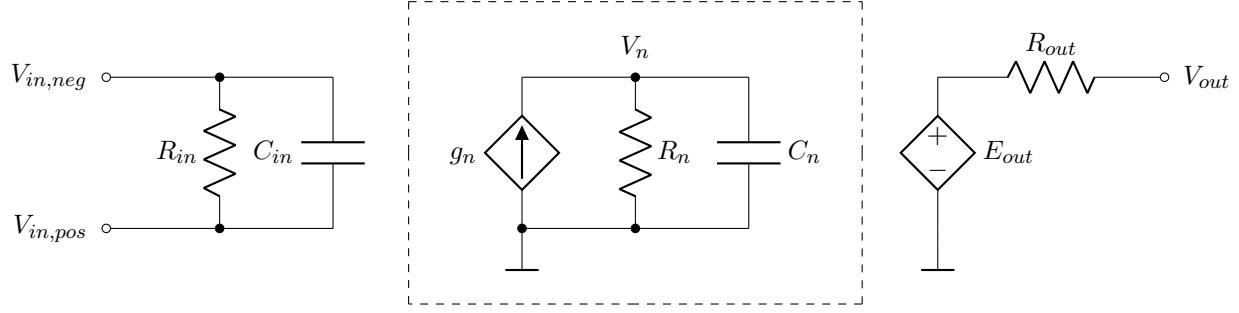


Figure 19: Circuit model for op-amps used in the LTSPICE simulations. The dashed box indicates a single pole stage and is replicated once for each pole in the model.

3 dB at GBW due to the second pole. It is then easy to calculate f_1 such that the overall gain equals 1 at GBW :

$$f_1 = \frac{GBW}{\sqrt{\left(\frac{A_{OL}}{1.413}\right)^2 - 1}} \quad (21)$$

The constant 1.413 is equal to -3 dB of voltage gain. Note that with this choice of pole frequencies, the phase margin of the op-amp is always $180^\circ - 135^\circ = 55^\circ$, due to a 90° contribution of the first pole, and 45° from the second. The third pole is present in order to improve high-frequency rolloff, and we always choose $f_3 = 100 \cdot GBW$.

Each pole stage n (for $1 \leq n \leq 3$) is implemented by the parallel combination of a resistor and a capacitor (Fig. 19, dashed box). We pick $R_n = 1 \text{ k}\Omega$ and calculate $C_n = 1/(2\pi f_n R_n)$. Each RC circuit is coupled to the previous stage by means of a voltage-controlled current source g_n with gain $1/R_n$ and control voltage $V_{in, pos} - V_{in, neg}$ for the first stage, and V_{n-1} for stage $n > 1$.

The DC gain of the op-amp is modeled by the output buffer E_{out} , a voltage-controlled voltage source with gain A_{OL} , and control voltage that of the final pole stage V_N .

B Repository

All simulations, analysis and plotting scripts, prototype PCB designs and empirical measurement data, are available as supplementary material at:
https://github.com/turingbirds/howland_vccs.

C Citation

This unabridged preprint, which was not peer reviewed, contains additional background information such as loop stability simulations, that could be helpful in reproducing and iterating upon the results in the paper published as

C. Linssen and P. Harpe, “Practical Measurement of Voltage-Controlled Current Source Output Impedance for Applications in Transcranial Electrical Stimulation,” 2021 IEEE Biomedical Circuits and Systems

Conference (BioCAS), 6–9 Oct 2021, pp. 1-6,doi: 10.1109/BioCAS49922.2021.9644974.

Please find the final accepted peer-reviewed paper in the repository (App. B).

References

- [1] A. J. Woods, A. Antal, M. Bikson, P. S. Boggio, A. R. Brunoni, P. Celnik, L. G. Cohen, F. Fregni, C. S. Herrmann, E. S. Kappenman, H. Knotkova, D. Liebetanz, C. Miniussi, P. C. Miranda, W. Paulus, A. Priori, D. Reato, C. Stagg, N. Wenderoth, and M. A. Nitsche, “A technical guide to tDCS, and related non-invasive brain stimulation tools,” *Clin Neurophysiol*, vol. 127, no. 2, pp. 1031–1048, Feb 2016.
- [2] D. Terney, L. Chaieb, V. Moliaidze, A. Antal, and W. Paulus, “Increasing human brain excitability by transcranial high-frequency random noise stimulation,” *J. Neurosci.*, vol. 28, no. 52, pp. 14 147–14 155, Dec 2008.
- [3] Medtronic, “Activa PC, Activa RC, and Activa neurostimulation systems for deep brain stimulation. 10/10 programmer guide for software version B. Minneapolis: Medtronic, Inc; N’Vision Clinician Programmer with Software,” pp. 8840–8870, 2010.
- [4] C. Hahn, J. Rice, S. Macuff, P. Minhas, A. Rahman, and M. Bikson, “Methods for extra-low voltage transcranial direct current stimulation: current and time dependent impedance decreases,” *Clin Neurophysiol*, vol. 124, no. 3, pp. 551–556, Mar 2013.
- [5] U. Palm, K. B. Feichtner, A. Hasan, G. Gauglitz, B. Langguth, M. A. Nitsche, D. Keeser, and F. Padberg, “The role of contact media at the skin-electrode interface during transcranial direct current stimulation (tDCS),” *Brain Stimul*, vol. 7, no. 5, pp. 762–764, 2014.
- [6] P. Minhas, V. Bansal, J. Patel, J. S. Ho, J. Diaz, A. Datta, and M. Bikson, “Electrodes for high-definition transcutaneous DC stimulation for applications in drug delivery and electrotherapy, including tDCS,” *J Neurosci Methods*, vol. 190, no. 2, pp. 188–197, Jul 2010.
- [7] J. Liu, X. Qiao, M. Wang, W. Zhang, G. Li, and L. Lin, “The differential Howland current source with high signal to noise ratio for bioimpedance measurement system,” *Rev Sci Instrum*, vol. 85, no. 5, p. 055111, May 2014.
- [8] S. Franco, *Design with operational amplifiers and analog integrated circuits*. McGraw-Hill Education, 1988.
- [9] P. Bertemes-Filho, L. H. Negri, A. Felipe, and V. C. Vincence, “Mirrored modified howland circuit for bioimpedance applications: Analytical analysis,” *Journal of Physics: Conference Series*, vol. 407, no. 1, p. 012030, 2012.
- [10] H. Hong, M. Rahal, A. Demosthenous, and R. H. Bayford, “Comparison of a new integrated current source with the modified Howland circuit for EIT applications,” *Physiol Meas*, vol. 30, no. 10, pp. 999–1007, Oct 2009.
- [11] G. S. Pomeroy, “Differential current source with active common mode reduction,” US Patent US 20 020 060 915 A1, May 23, 2002.
- [12] U. Pliquett, M. Schönfeldt, A. Barthel, D. Frense, and T. Nacke, “Offset-free bidirectional current source for impedance measurement,” *Journal of Physics: Conference Series*, vol. 224, 04 2010.
- [13] V. G. Sirtoli, K. F. Morcelles, and V. C. Vincence, “Design of current sources for load common mode optimization,” *Journal of Electrical Bioimpedance*, vol. 9, no. 1, pp. 59–71, 2018. [Online]. Available: <https://doi.org/10.2478/joeb-2018-0011>
- [14] M. Simmonds and P. Alesu, “Differential and symmetrical current source,” US Patent US 20 090 243 723 A1, Oct 1, 2009.
- [15] Wolfram Research, Inc., “Mathematica (version 11.1),” 2017.
- [16] Linear Technology, Inc., “LTSPICE (version XVII, Nov 18th, 2015).”

- [17] ——, “LT1211 datasheet,” Retrieved July 1st, 2020.
- [18] J. Lyklema, *Fundamentals of Interface and Colloid Science*. Academic Press, 1995, vol. 2.
- [19] P. F. Grant and M. M. Lowery, “Effect of dispersive conductivity and permittivity in volume conductor models of deep brain stimulation,” *IEEE Transactions on Biomedical Engineering*, vol. 57, no. 10, pp. 2386–2393, 2010.
- [20] S. Grimnes and Ø. G. Martinsen, *Bioimpedance and Bioelectricity Basics (3rd ed.)*. Academic Press, 1995.
- [21] R. D. Middlebrook, “Measurement of loop gain in feedback systems,” *Int. J. Electronics*, vol. 38, pp. 485–512, 1975.
- [22] K. Kundert, “A test bench for differential circuits,” *The Designer’s Guide Community*, <http://www.designers-guide.org/>, Version 1d, 12 September 2006.
- [23] J. A. Nelder and R. Mead, “A simplex method for function minimization,” *Computer Journal*, vol. 7, pp. 308–313, 1965.
- [24] International Rectifier, “PVT412 datasheet,” Retrieved July 1st, 2020.
- [25] J. W. Lee, T. I. Oh, S. M. Paek, J. S. Lee, and E. J. Woo, “Precision constant current source for electrical impedance tomography,” in *Engineering in Medicine and Biology Society, 2003. Proceedings of the 25th Annual International Conference of the IEEE*, vol. 2. IEEE, 2003, pp. 1066–1069.
- [26] D. R. Merrill, M. Bikson, and J. G. Jefferys, “Electrical stimulation of excitable tissue: design of efficacious and safe protocols,” *J Neurosci Methods*, vol. 141, no. 2, pp. 171–198, Feb 2005.