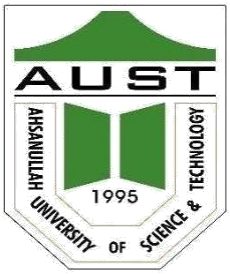

Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Course No: CSE 3110
Course Title: Digital System Design Lab
Assignment No: 01

Submitted By-

Section: C
Lab group: C1
Group: 07
Id: 18.01.04.103

18.01.04.104

18.01.04.117

Introduction:

An arithmetic and logic unit (ALU) is a combinational digital electronics circuit that performs arithmetical and logical operations on integer binary numbers. In this given experiment, we have built a 4-bit ALU. We have to implement a 4bit ALU that takes 4bit (A4,A3,A2,A1) , (B4,B3,B2,B1)with 1 bit Zin and perform given operation on them.

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Problem Statement :

Designing the following 4-bit ALU(Arithmetic Logic Unit):

S2	S1	S0	Output	Functions
1	0	0	Ai - 1	Decrement A
0	0	1	Ai + Bi + 1	Add with carry
1	0	1	Ai + 1	Increment A
0	0	0	Ai - Bi - 1	Substract with borrow
0	1	X	Ai . Bi	AND
1	1	X	Ai | Bi	OR

Function Generation:

S2	S1	S0	Zi	Xi	Yi	Function
1	0	0	0	Ai	All 1	Ai - 1
0	0	1	1	Ai	Bi	Ai + Bi + 1
1	0	1	1	Ai	0	Ai + 1
0	0	0	0	Ai	Bi'	Ai - Bi – 1 = Ai + Bi'
0	1	X	0	Ai . Bi	0	Ai . Bi
1	1	X	0	Ai | Bi	0	Ai | Bi

From the table, we can get:

Xi = S1' Ai + S2' S1 (Ai . Bi) + S2 S1 (Ai | Bi)

Yi = S2 S1' S0' . 1 + S2' S1' S0 Bi + S2' S1' S0' Bi'

= S2 S1' S0' + S2' S1' S0 Bi + S2' S1' S0' Bi'

For Z : Using K-Map we get ,

S2 \S1S0	00	01	11	10
0	0	**1**	3	2
1	4	5	7	6

Zi = S1' S0 (Bold and Underlined cell should be taken for grouping).

Equipment and Budget Comparison:

For this project required equipment are:
Total IC-48

1. 4073 (3 input AND gate) - 11 pieces, each one 25.47 BDT.
2. 4075 (3 input OR gate) - 8 pieces, each one 22.67 BDT.
3. 7483 (4-Bit Binary Full Adder) - 1 piece, each one 45.7 BDT.
4. 4081 (2 input AND gate) – 17 pieces, each one 23.59 BDT.
5. 7404 (NOT gate) – 7 pieces, each one 25.59 BDT.
6. 4071 (2 input OR gate) – 4 pieces, each one 27.59 BDT.
7. LOGGICTOGGLE - 11 pieces , 0.9 BDT.
8. LOGICPROBE - 5 pieces , each one 7.4 BD.
9. Bread Board – 4 Pieces, each one 94 BDT(Real life use).
10. Jumper wire - 150 pieces, each bundle(50 pieces) 50BDT(Real life use).

Total estimated budget: 1770.65 bdt

Simulation :

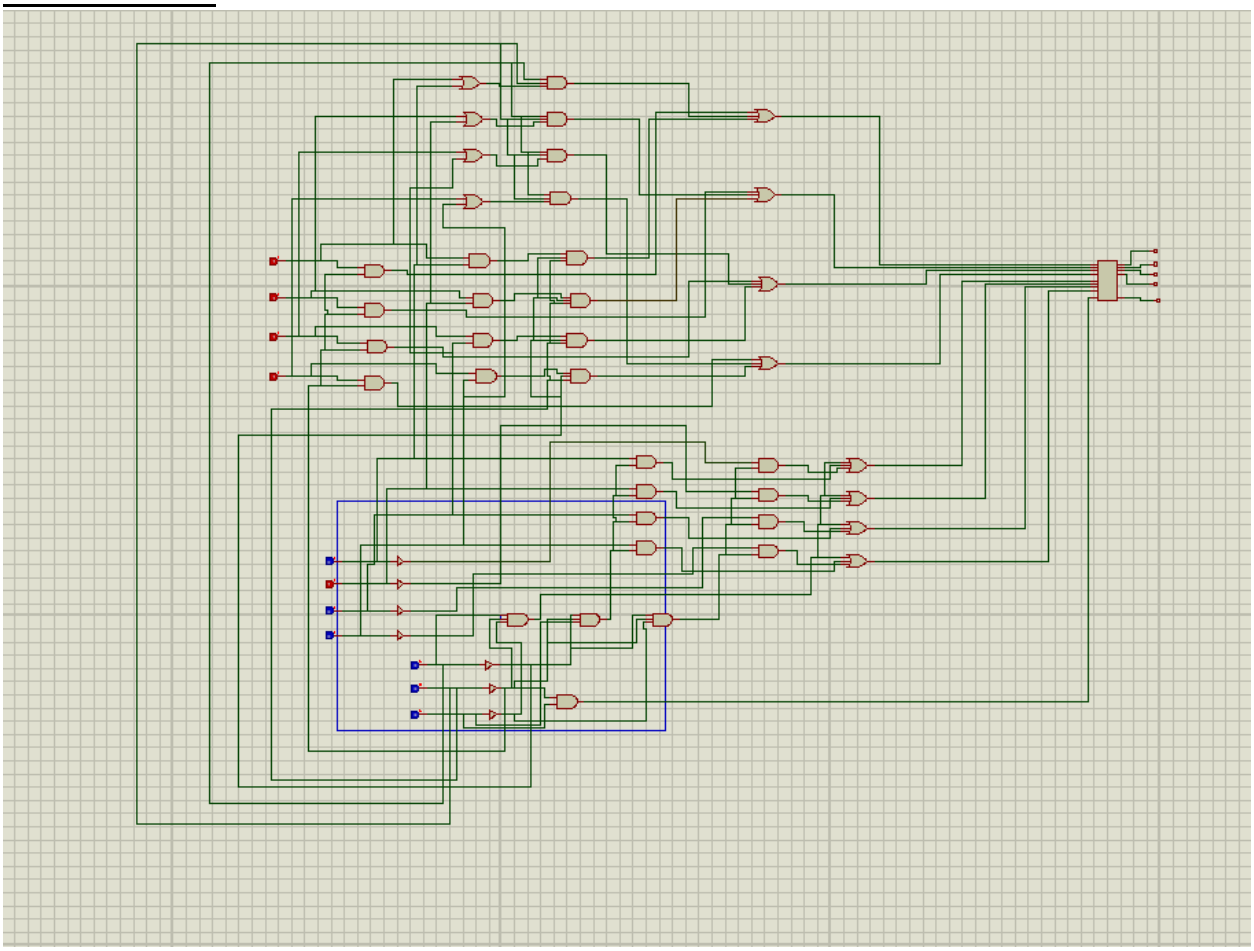

Figure: Circuit Implementation and Simulation Using Proteus

Result:

So our final example input and output results from the circuit:

S2	S1	S0	Zi	Xi	Yi	Output	Final	Cout	Result	Target
1	0	0	0	1000	1111	Ai -1	0111	1	Decrement A	Decrement A
0	0	1	1	1010	1111	Ai+ Bi + 1	1010	1	Add with carry	Add with carry
1	0	1	1	0101	0	Ai+1	0110	0	Increment A	Increment A
0	0	0	0	1010	1010	Ai - Bi - 1	0100	1	Substract with borrow	Substract with borrow
0	1	X	0	0001	0	Ai . Bi	0001	0	AND	AND
1	1	X	0	1111	0	Ai | Bi	1111	0	OR	OR

Conclusion:

Though we have proved our result successfully for all outputs, but we might face problem as-

1. Used equipment can be damaged if carefully not handled.
2. Using unnecessary wire can cause of short circuit.
3. Use of unnecessary gates may make implementation difficult.