Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Course No : CSE3110
Course Title : Digital System Design Lab
Assignment No : 03

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Submitted By-

Group : G7
Id : 18.01.04.103
18.01.04.104
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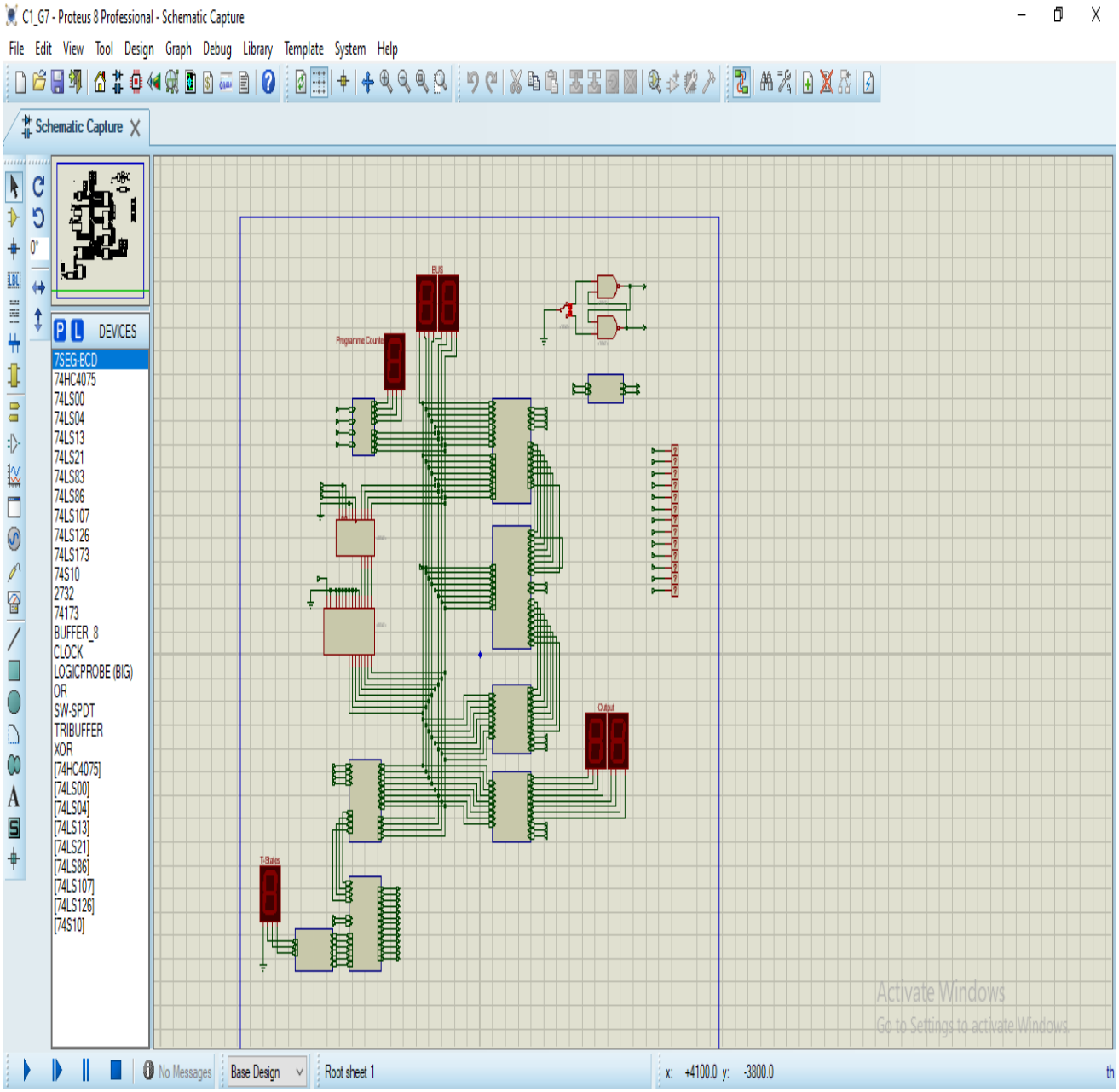
Section : C1

1. Introduction:

The Simple-As-Possible (SAP)-1 is a very basic model of a microprocessor explained by Albert Paul Malvino. The SAP-1 design contains the basic necessities for a functional Microprocessor. Its primary purpose is to develop a basic understanding of a microprocessor, how it works, interacts with memory and other parts of the system like input and output. The instruction set is very limited and simple.

2. Problem Statement:

SAP-1 Simulation.


C1_G7 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Schematic Capture
DEVICES
7SEG-BCD
74HC4075
74LS00
74LS04
74LS13
74LS21
74LS83
74LS86
74LS107
74LS126
74LS173
74S10
2732
74173
BUFFER_8
CLOCK
LOGICPROBE (BIG)
OR
SW-SPDT
TRIBUFFER
XOR
[74HC4075]
[74LS00]
[74LS04]
[74LS13]
[74LS21]
[74LS86]
[74LS107]
[74LS126]
[74S10]
BUS
Programme Counter
Output
T-States
No Messages
Base Design
Root sheet 1
x: +4100.0 y: -3800.0
Activate Windows
Go to Settings to activate Windows.

4. Equipment and Budget:

Equipment	Estimated Cost (per unit)
7SEG-BCD	250
74LS00	283
74LS04	700
74LS83	244
74LS86	290
74LS173	300
74173	200
BUFFER_8	173
LOGICPROBE	145
OR	180
SW_SPDT	200
XOR	200

5. Result:

We take the following Example:

Address	Code	in Hex
0H	LDA 5H	05
1H	ADD 6H	16
2H	SUB 7H	27
3H	OUT	EF
4H	HLT	FF
5H	55H	55
6H	33H	33
7H	11H	11

(I) LDA 5H: content of memory location 55H is copied in accumulator.

(II) ADD 6H: Value of memory location 33H is added with 55H, So, output now (55+33)H = 88H

(III) SUB 7H: 11H is substracted from 88H

(IV) OUTPUT: final output is 77 for this operation.

(V) HLT: Halts the microprocessor:

6. Conclusion:

Jumping into a project without considering similar, past projects is never an easy task. We have faced many difficulties. Our understanding of the implementation is still not very clear in couple of places. But we successfully implemented this SAP-1 circuit in Proteus despite the difficulties.