ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY HOMEWORK REPORT

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1 PRELIMINARIES

1.1 PRELIMINARY 1

There are different types of flip-flops but they are all mainly used for storing data in the form of bits for further use. They may have one or two outputs with the second being the complement of the first. Flip-flops work with clock signals. When a rising-edge signal comes, the data gets transferred into the flip-flop and a state change occurs. Different flip-flops behave differently to different inputs.

1.2 PRELIMINARY 2

Flip-flops make use of clock signals whereas latches don't have clock inputs. This way, flip-flops work synchronously but latches work asynchronously. This means that the input change in a flip-flop is only meaningful when a rising-edge comes but latches change their output immediately.

1.3 PRELIMINARY 3

An SR-Latch has two inputs - S and R. S stands for "Set" which sets the output to '1'. and R stands for "Reset" which resets the output to '0'. '1-1' is an illegal input. SR-Latch has two outputs. One of them is decided by the input and the other is just the complemented version of the first output.

1.4 PRELIMINARY 4

SR Latch and its truth table is given in Figure 1.

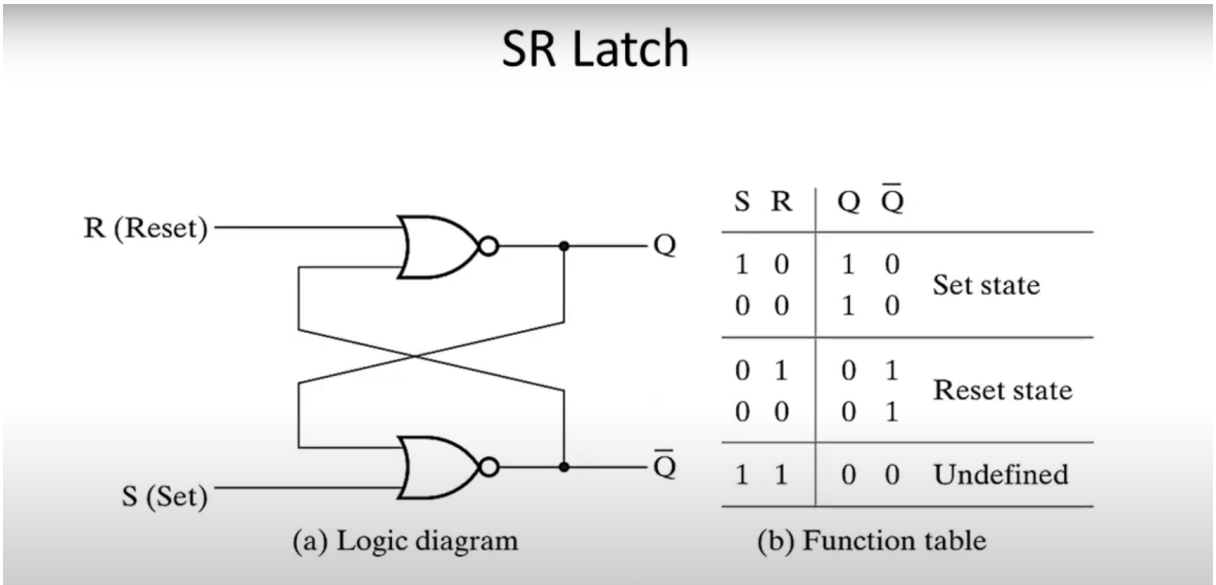

Figure 1: SR-Latch and Truth Table

1.5 PRELIMINARY 5

SR Latch with Control(Enable) input is given in Figure 2.

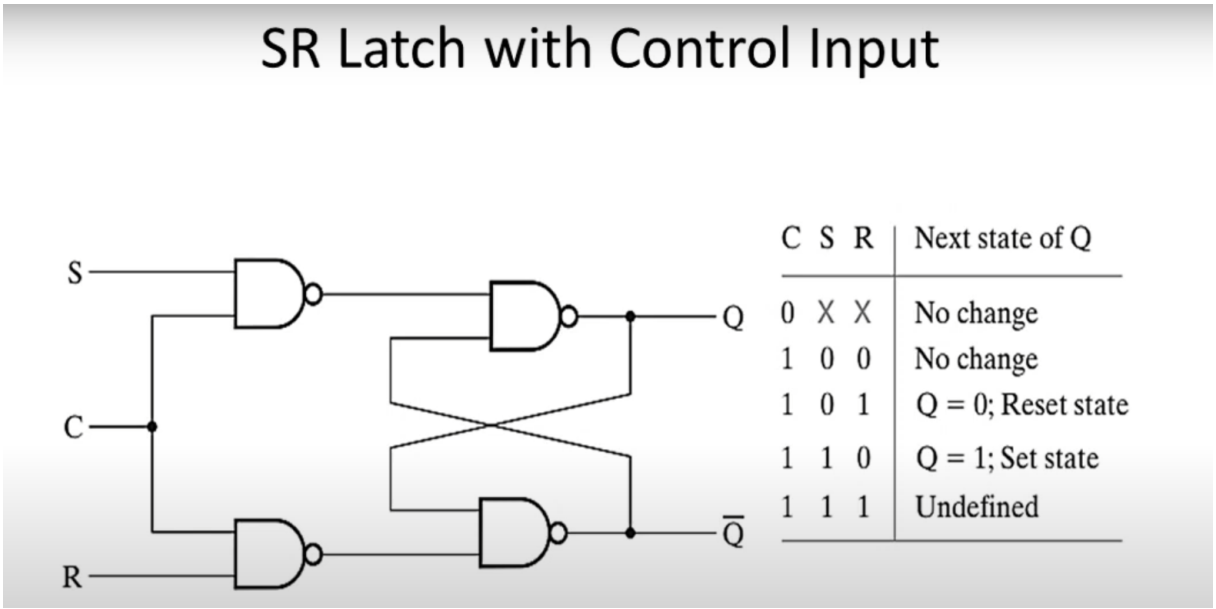

Figure 2: SR-Latch with Enable and Truth Table

1.6 PRELIMINARY 6

The JK Flip Flop Truth table is given in Table 1.

CLK	**J**	**K**	**Qn+1**
0	X	X	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	X

Table 1: JK Flip Flop Truth Table

1.7 PRELIMINARY 7

The D Flip Flop truth table is given in Table 2.

CLK	**D**	**Qn+1**
0	X	Qn
1	0	0
1	1	1

Table 2: D Flip Flop Truth Table

2 EXPERIMENT

2.1 PART 1

SR Latch's design and simulation results are given below.

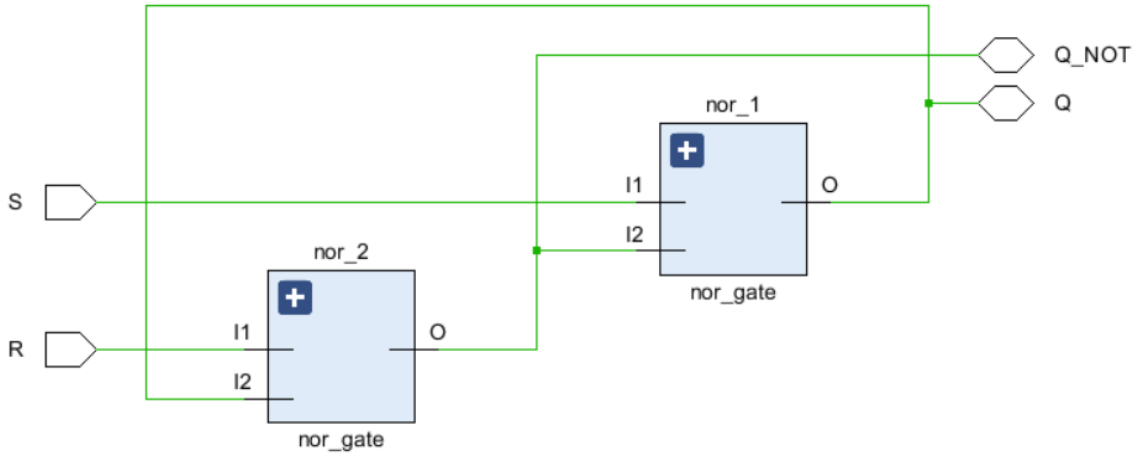

Figure 3: SR Latch Design

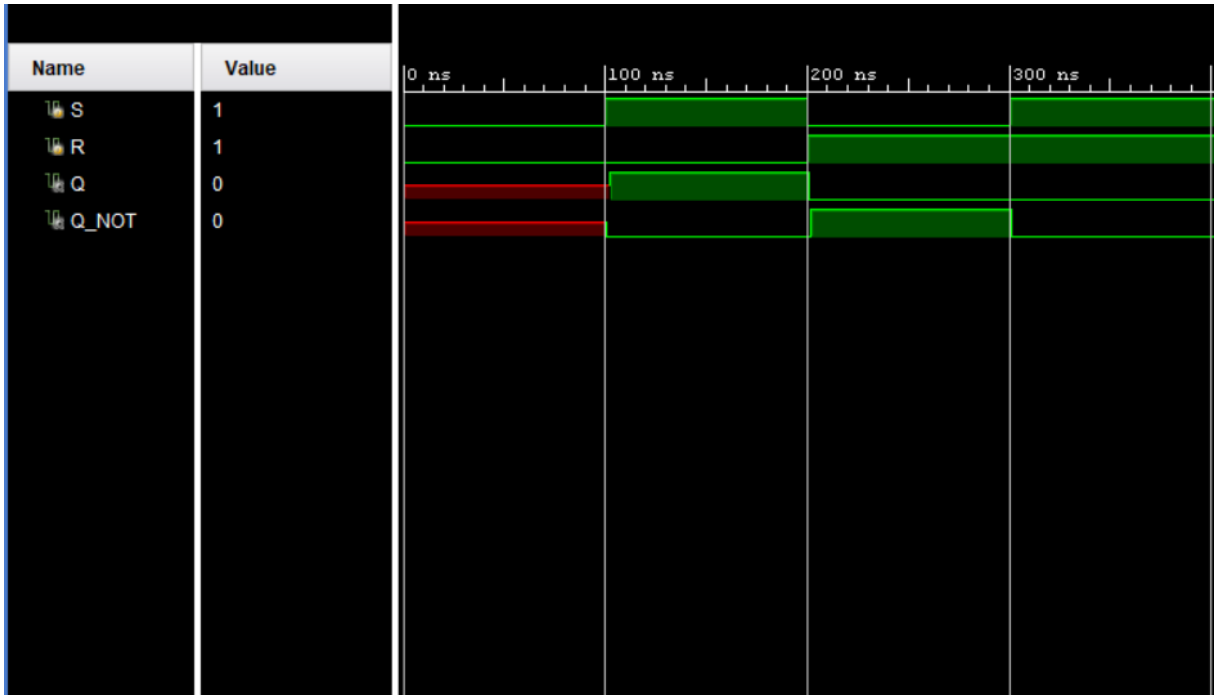

Figure 4: SR Latch Simulation

2.2 PART 2

SR Latch with Enable input's design and simulation results are given below.

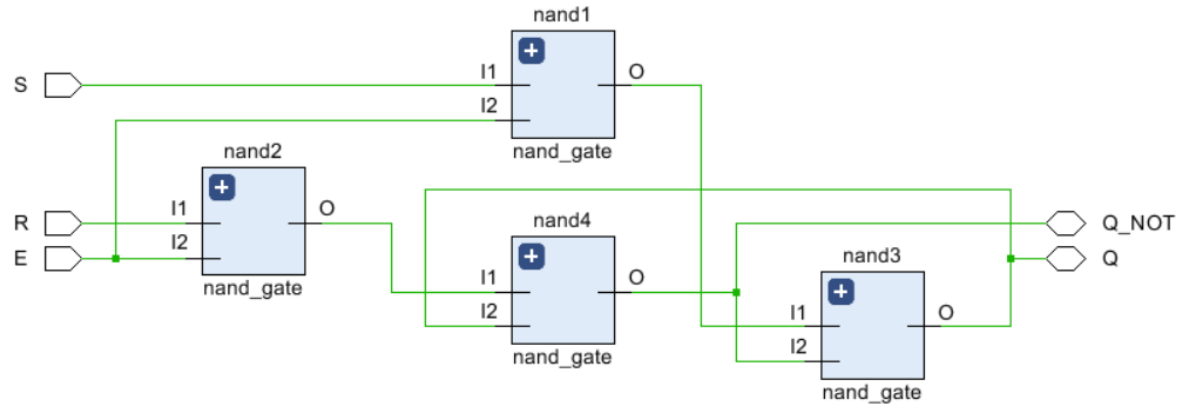

Figure 5: SR Latch with Enable Design

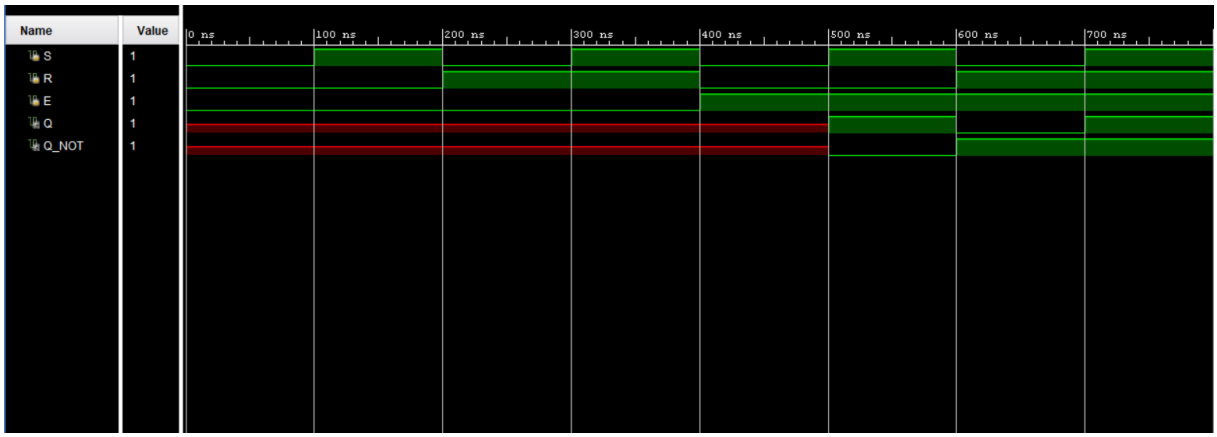

Figure 6: SR Latch with Enable Simulation

2.3 PART 3

D Latch and rising edge triggered D Flip-Flop's designs and simulation results are given below.

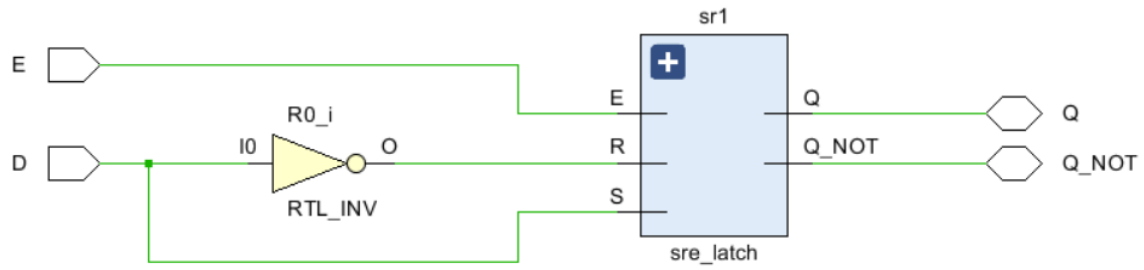

Figure 7: D Latch Design

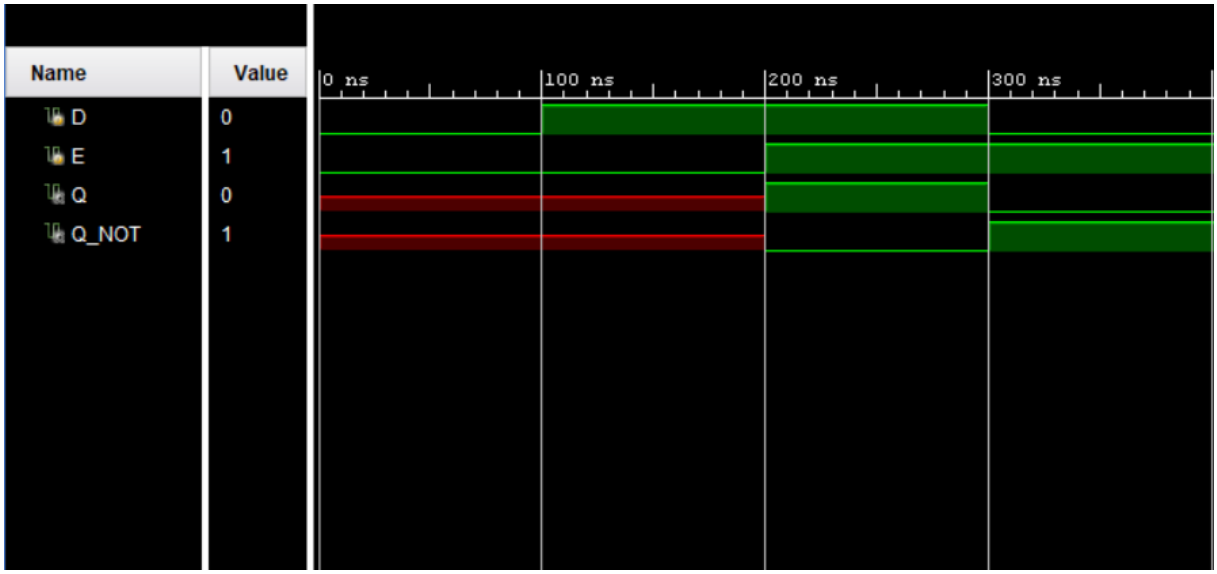

Figure 8: D Latch Simulation

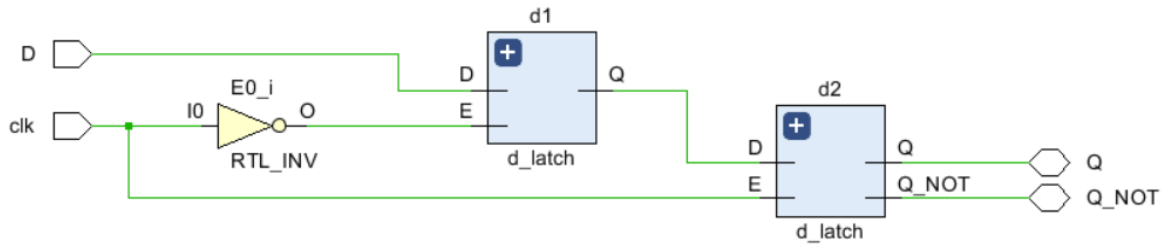

Figure 9: D Flip-Flop Design

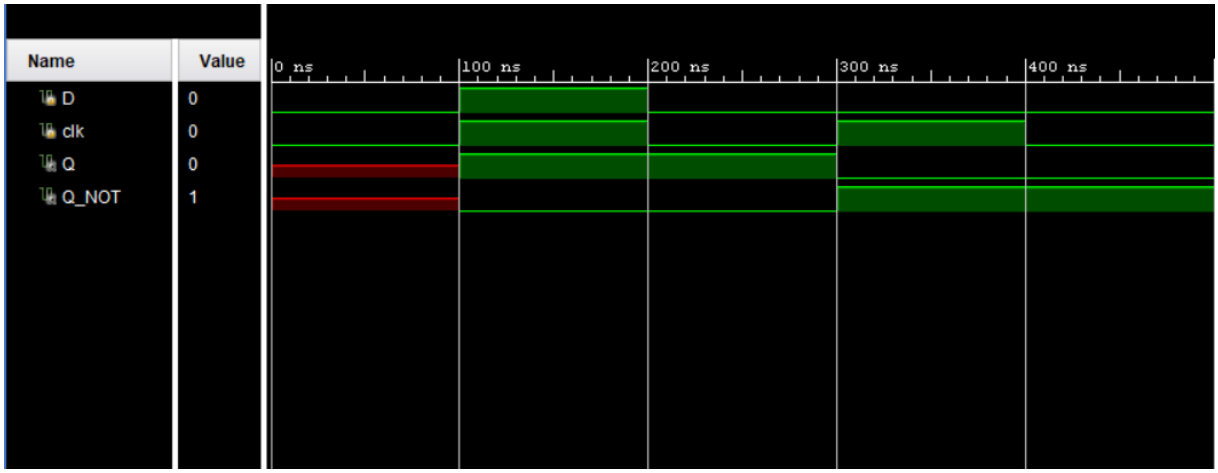

Figure 10: D Flip-Flop Simulation

2.4 PART 4

Design and simulation results of rising-edge triggered JK flip flop that uses an SR latch and NAND gates are below.

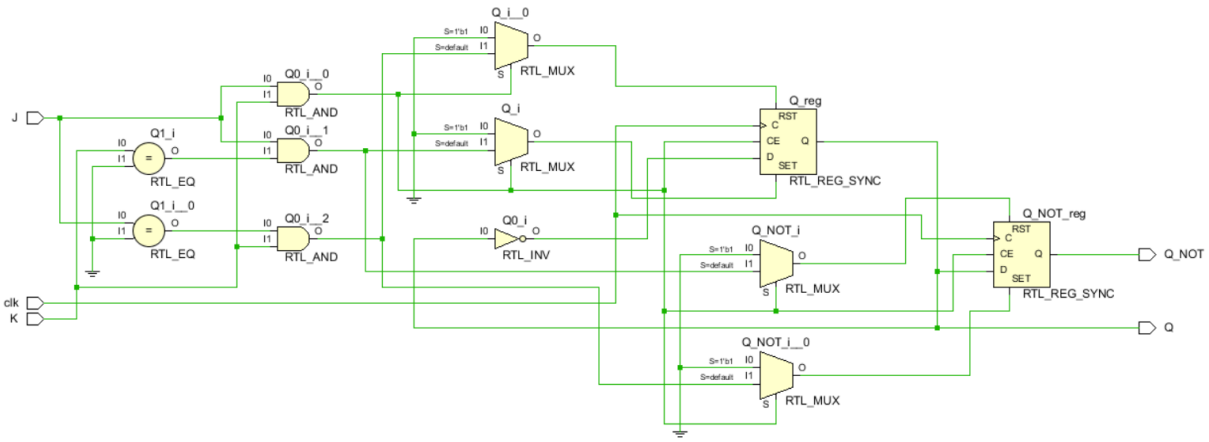

Figure 11: JK Flip-Flop Design

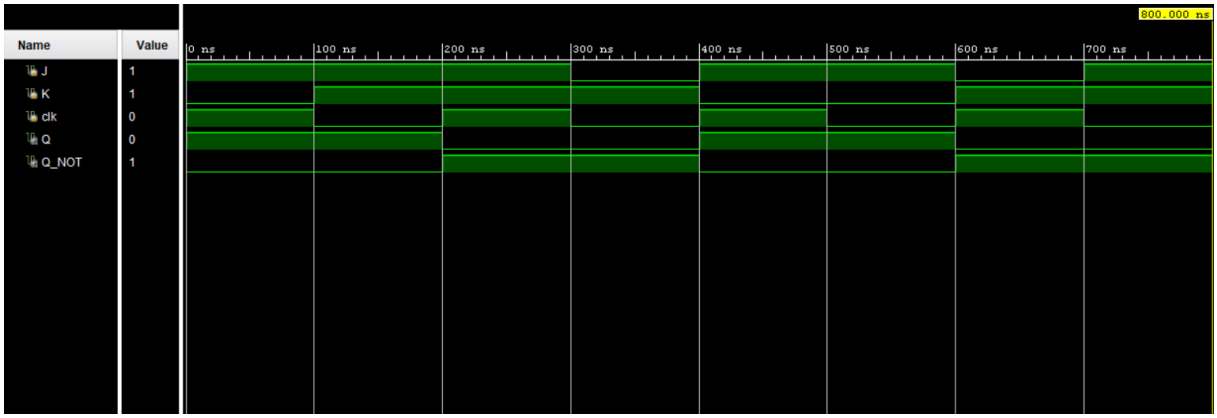

Figure 12: JK Flip-Flop Simulation

2.5 PART 5

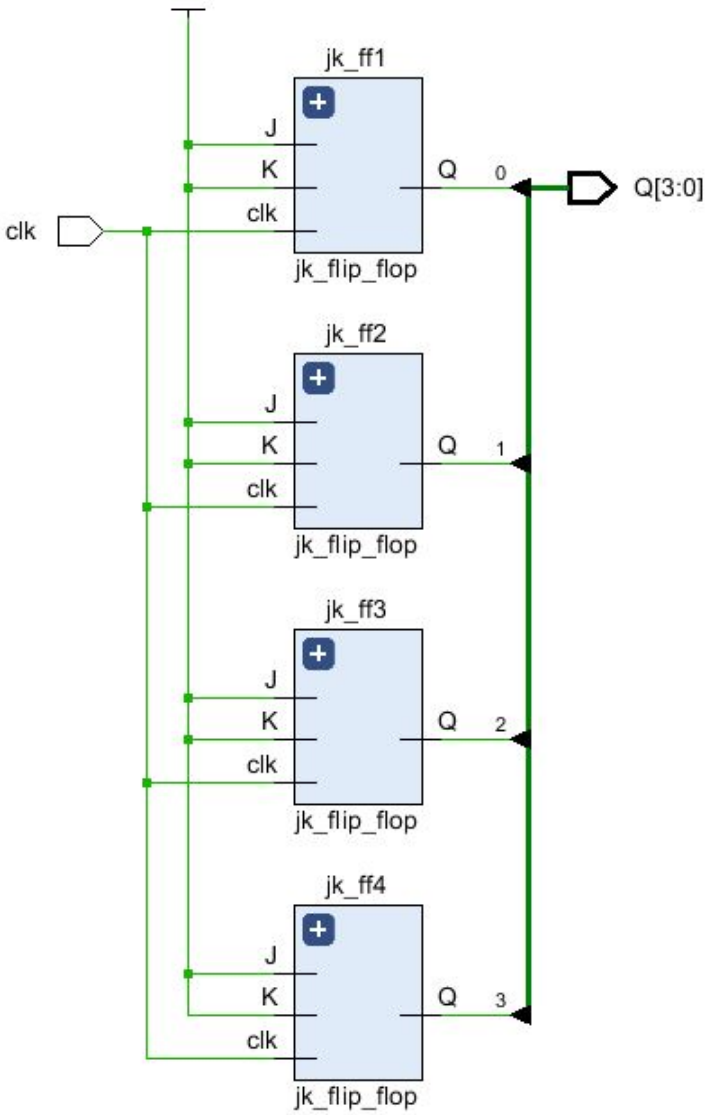

Figure 13: Part5 Design

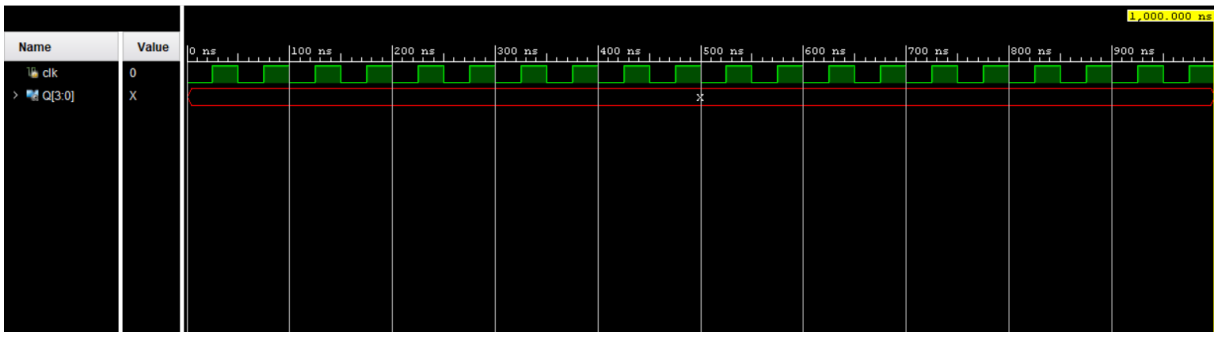

Figure 14: PART5 Simulation

2.6 PART 6

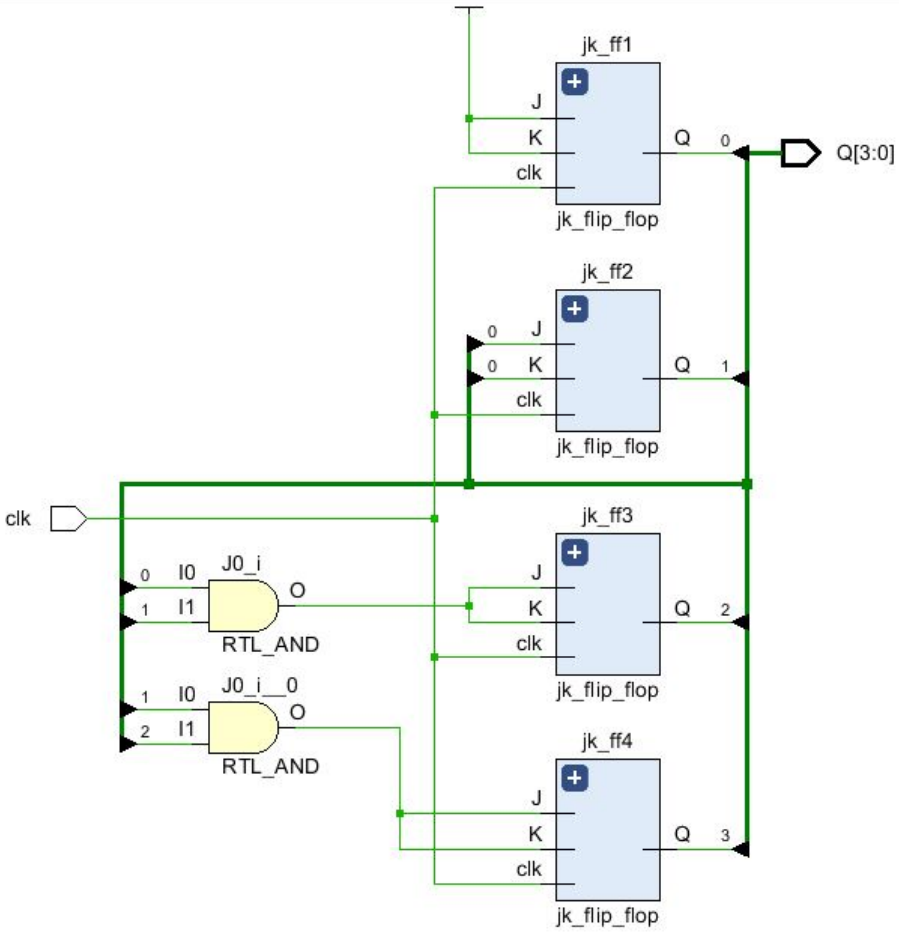

Figure 15: Part6 Design