Chen-Chia Chang

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Research Interests

Electronic Design Automation (EDA), Machine Learning for EDA

Education

Duke University *09/2020 - PRESENT*
Ph.D. Student in Electrical and Computer Engineering *Durham, NC*
Advisor: Prof. Yiran Chen

National Taiwan University (NTU) *09/2015 - 01/2020*
B.S. in Electrical Engineering *Taipei, Taiwan*

Experience

Computational Evolutionary Intelligence Lab (Prof. Yiran Chen) *09/2020 - PRESENT*
Graduate Research Assistant, Duke ECE

- **Automated ML Model Development for Digital and Analog IC Applications**
  - Proposed feature selection and the NAS method to automatically develop the ML model without human interference for routability prediction [ICCAD'21] and analog placement prediction [ASPDAC'23].
- **ML Model Security and Reliability Investigation in EDA**
  - Examined the threat of ML model extraction attack against EDA applications [ASPDAC'23].
  - Surveyed the ML Model Security and Reliability open questions for EDA [TCAD'22]
- **Decentralized training on ML for EDA application**
  - Proposed a federated learning method [DAC'22] to collaboratively train ML model with the data provided by multiple design companies
  - Investigated a privacy-preserving data-collecting framework [to be summited to DAC'23].

IBM Corporation *05/2023 - 08/2023*
Research Intern

- **Automated Analog Design via Language Model**
  - Investigated applying LLM for analog topology generation and performance prediction.

Cadence Design Systems *05/2022 - 08/2022*
Machine Learning Software Engineer Intern

- **Analog placement parasitic prediction**
  - Developed a DL-based technique to predict the capacitance of the critical net from placement.

Electronic Design Automation Lab (Prof. Yao-Wen Chang) *01/2018 - 01/2020*
Undergraduate Research Assistant, NTU EE

- **Initial Detailed Routing (2nd place in 2019 ISPD Contest)**
  - Designed a robust detailed routing engine that capable of routing circuits with 1 million nets while considering the trade-off between industrial DRC and wirelength.
- **System-level FPGA Routing with Timing Division Multiplexing [ICCAD 2021]**
  - Proposed a two-stage algorithm to realize FPGA-routing and TDM assignment.

Applied Logic and Computation Lab (Prof. Jie-Hong R. Jiang) *01/2018 - 01/2020*

Undergraduate Research Assistant, NTU EE

- **QBF Certification: From Countermodel to Resolution**
  - Proposed a proof transformation method to convert the Herbrand function to LQU refutation proof; Provided more compact resolution proofs than the ones derived from the state-of-art QBF solver.

Publications

1. **C.-C. Chang**, J. Pan, Z. Xie, J. Hu, and Y. Chen. "Rethink before Releasing your Model: ML Model Extraction Attack in EDA," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023 ***[Best paper award]***.
2. **C.-C. Chang**, J. Pan, Z. Xie, Y. Li, Y. Lin, J. Hu, and Y. Chen. "Fully Automated Machine Learning Model Development for Analog Placement Quality Prediction," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023 ***[Best paper nomination]***.
3. Z. Xie, S. Li, M. Ma, **C.-C. Chang**, J. Pan, Y. Chen, and J. Hu. "DEEP: Developing Extremely Efficient Runtime On-Chip Power Meters." in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2022.
4. J. Pan, **C.-C. Chang**, Z. Xie, J. Hu, , and Y. Chen. "Robustify ML-Based Lithography Hotspot Detectors," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2022.
5. Z. Xie, J. Pan, **C.-C. Chang**, J. Hu, and Y. Chen. "The Dark Side: Security and Reliability Concerns in Machine Learning for EDA," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022
6. Z. Xie, R. Liang, X. Xu, J. Hu, **C.-C. Chang**, J. Pan, and Y. Chen. "Pre-Placement Net Length and Timing Estimation by Customized Graph Neural Network," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.
7. J. Pan, **C.-C. Chang**, Z. Xie, A. Li, M. Tang, T. Zhang, J. Hu, and Y. Chen."Towards Collaborative Intelligence: Routability Estimation based on Decentralized Private Data," in *Proc. IEEE/ACM Design Automation Conference (DAC)*, 2022.
8. **C.-C. Chang**, J. Pan, T. Zhang, Z. Xie, J. Hu, W. Qi, C.-W. Lin, R. Liang, J. Mitra, E. Fallon, and Y. Chen, "Automatic Routability Predictor Development Using Neural Architecture Search," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2021.
9. W.-K. Liu, M.-H. Chen, C.-M. Chang, **C.-C. Chang**, and Y.-W. Chang, "Performance-Driven System-Level FPGA Routing with TDM Optimization," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2021.

Honors & Awards

2023 **Best Paper Award**, IEEE/ACM ASP-DAC
2019 **Outstanding Performance Scholarship**, National Taiwan University
2019 **Top 5, Honorable Mentions**, IEEE/ACM ICCAD CAD Contest - Problem C
2019 **2nd Place**, ACM ISPD Initial Detailed Routing Contest

Skills

Programming C/C++, Python, Verilog
VLSI tools Cadence Innovus, Quartus II, FPGA Prototyping
Deep Learning Toolkits Pytorch, Tensorflow, Keras