Chen-Chia Chang

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Research Interests

Electronic Design Automation (EDA), Machine Learning & LLM for EDA

Education

Duke University *09/2020 - 02/2025*

Ph.D. in Electrical and Computer Engineering

- Advisor: Prof. Yiran Chen

National Taiwan University (NTU) *09/2015 - 01/2020*

B.S. in Electrical Engineering

Experience

NVIDIA Corporation *02/2025 - PRESENT*

Senior Machine Learning Engineer

- **ML for Analog Automation from Design to Layout**

NVIDIA Corporation (Manager: Mark Ren) *05/2024 - 12/2024*

Design Automation Research Intern

- **Automated DRC Code Generation Using LLM-Agent [ISPD'25]**
  - Proposed a multi-agent framework with multi-modal vision capability to automate DRC checker code generation.
  - Generated correct DRC codes for sub-3nm technology (F1=1.0) for all design rules considered in NVCell.

IBM Corporation (Manager: Xin Zhang) *05/2023 - 08/2023*

MIT-IBM Watson AI Research Intern

- **Language Model-based Topology Generation for Analog Integrated Circuit [ICML'24]**
  - Proposed a text-based hypergraph circuit representation to capture graph similarity via original LM loss function.
  - Achieved efficient generation of an optimized circuit design from the custom specification with a success rate of 96% under a strict tolerance of 0.01.

Computational Evolutionary Intelligence Lab (Prof. Yiran Chen) *09/2020 - 02/2025*

Graduate Research Assistant

- **AutoML for Digital and Analog IC [ICCAD'21] [ASPDAC'23] [TCAD'23]**
  - Proposed a feature selection and a neural architecture search (NAS) method to automatically develop ML models without human interference for routability prediction and analog placement prediction.
  - Achieved up to 10% performance improvement over the state-of-the-art manually-designed models and shortened the model development time into 0.3 days.
- **ML Model Security for EDA [ASPDAC'23]**
  - Proposed two model extraction attack methods: confidence-based and information-based iterative data selection.
  - Examined the threat of EDA model privacy and raise concerns about ML security issues in EDA.
- **Privacy-Preserving Circuit Data Sharing for ML Applications [ASPDAC'25]**
  - Proposed a mask-based pruning network to effectively obfuscate feature patterns and incorporated with adversarial training to retain abundant prediction information in protected features.
  - Achieved 55% feature protection improvement over state-of-the-art obfuscating methods in computer vision.

Cadence Design Systems *05/2022 - 08/2022*

Machine Learning Software Engineer Intern

- **Analog placement parasitic prediction**
  - Developed an ML model to predict the capacitance of the critical net in analog placement.

Electronic Design Automation Lab (Prof. Yao-Wen Chang) *01/2018 - 01/2020*

Undergraduate Research Assistant

- **Initial Detailed Routing [2nd place in 2019 ISPD Contest]**
  - Developed a robust detailed routing engine that completes routing circuits with 1 million nets while considering the trade-off between industrial DRC and wirelength.
- **System-level FPGA Routing with Timing Division Multiplexing [ICCAD 2021]**
  - Proposed a simultaneous FPGA routing and TDM assignment algorithm considering net timing criticality.
  - Outperformed all existing works with up to 9X runtime speedup.

Publications

First Author Papers:

1. **C.-C. Chang**, W.-H. Lin, Y. Shen, Y. Chen, and X. Zhang. "LaMAGIC2: Advanced Circuit Formulations for Language Model-Based Analog Topology Generation," submitted to *International Conference on Machine Learning (ICML)*, 2025
2. **C.-C. Chang**, C.-T. Ho, Y. Li, Y. Chen, and H. Ren. "DRC-Coder: Automated DRC Checker Code Generation Using LLM Autonomous Agent," in *Proc. ACM International Symposium on Physical Design (ISPD)*, 2025
3. **C.-C. Chang**, W.-H. Lin, J. Pan, G. Zhou, Z. Xie, J. Hu, and Y. Chen. "PRICING: Privacy-Preserving Circuit Data Sharing for Lithographic Hotspot Detection," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2025
4. **C.-C. Chang**, Y. Shen, S. Fan, J. Li, S. Zhang, N. Cao, Y. Chen, and X. Zhang. "LaMAGIC: Language-Model-based Topology Generation for Analog Integrated Circuits," in *Proc. International Conference on Machine Learning (ICML). PMLR*, 2024
5. **C.-C. Chang**, J. Pan, T. Zhang, Z. Xie, J. Hu, and Y. Chen, "Towards Fully Automated Machine Learning for Routability Estimator Development ," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 2023
6. **C.-C. Chang**, J. Pan, Z. Xie, J. Hu, and Y. Chen. "Rethink before Releasing your Model: ML Model Extraction Attack in EDA," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023 ***[Best paper award]***
7. **C.-C. Chang**, J. Pan, Z. Xie, Y. Li, Y. Lin, J. Hu, and Y. Chen. "Fully Automated Machine Learning Model Development for Analog Placement Quality Prediction," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2023 ***[Best paper nomination]***
8. **C.-C. Chang**, J. Pan, T. Zhang, Z. Xie, J. Hu, W. Qi, C.-W. Lin, R. Liang, J. Mitra, E. Fallon, and Y. Chen, "Automatic Routability Predictor Development Using Neural Architecture Search," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2021

Collaborated Papers:

1. Q. Zhang, S. Li, G. Zhou, J. Pan, **C.-C. Chang**, Y, Chen, and Z. Xie. "PANDA: Architecture-level power evaluation by unifying analytical and machine learning solutions," in *Proc. IEEE/ACM IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2023
2. Z. Xie, S. Li, M. Ma, **C.-C. Chang**, J. Pan, Y. Chen, and J. Hu. "DEEP: Developing Extremely Efficient Runtime On-Chip Power Meters." in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2022
3. J. Pan, **C.-C. Chang**, Z. Xie, J. Hu, , and Y. Chen. "Robustify ML-Based Lithography Hotspot Detectors," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2022
4. Z. Xie, J. Pan, **C.-C. Chang**, J. Hu, and Y. Chen. "The Dark Side: Security and Reliability Concerns in Machine Learning for EDA," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022
5. Z. Xie, R. Liang, X. Xu, J. Hu, **C.-C. Chang**, J. Pan, and Y. Chen. "Pre-Placement Net Length and Timing Estimation by Customized Graph Neural Network," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022
6. J. Pan, **C.-C. Chang**, Z. Xie, A. Li, M. Tang, T. Zhang, J. Hu, and Y. Chen."Towards Collaborative Intelligence: Routability Estimation based on Decentralized Private Data," in *Proc. IEEE/ACM Design Automation Conference (DAC)*, 2022
7. W.-K. Liu, M.-H. Chen, C.-M. Chang, **C.-C. Chang**, and Y.-W. Chang, "Performance-Driven System-Level FPGA Routing with TDM Optimization," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2021

Honors & Awards

2023 **Best Paper Award**, IEEE/ACM ASP-DAC
2023 **Best Paper Nomination**, IEEE/ACM ASP-DAC
2019 **Outstanding Performance Scholarship**, National Taiwan University
2019 **Top 5, Honorable Mentions**, IEEE/ACM ICCAD CAD Contest - Problem C
2019 **2nd Place**, ACM ISPD Initial Detailed Routing Contest

Skills

Programming	C/C++, Python, Verilog
Deep Learning Toolkits	Pytorch, Tensorflow, Huggingface
VLSI tools	Cadence Innovus, Virtuoso