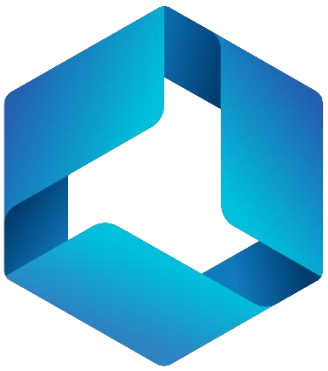

ALTIUM 365

Altium Designer

Essentials Course - Altium 365

Module 25: PCB Design Rule Checks (DRCs)

Table of Contents

Module 25: PCB Design Rule Checks (DRCs)

1.1 Purpose

Running a Design Rule Check (DRC) in Altium Designer is a crucial step in the PCB design process. The DRC is a comprehensive set of rules and checks that help ensure the integrity, manufacturability, and reliability of the printed circuit board (PCB).

In this exercise, students will learn how to properly inspect, check the health and resolve violations using the Health Check, the Design Rule Check as well as the PCB Rules and Violations panel.

1.2 Shortcuts

Shortcuts when working with Module 25: PCB Design Rule Checks (DRCs)

T » D:	Design Rule Check
T » M:	Reset Error Markers
T » P:	Preferences

1.3 Preparation

1. **Close all existing projects and documents.**
2. Next, create a Copy / Clone of the Training Project `Module 25 PCB Design Rule Checks (DRCs).`
3. Select **File » Open Project…** to open the *Open Project* dialog.
4. Navigate to the predefined Training Project: `Module 25 PCB Design Rule Checks (DRCs) (Top\Projects\Altium Designer Essentials Training Course\...).`
5. Select **Open Project as Copy…** 

.
6. At the new dialog *Create Project Copy:*
   a) Add your name to the project name: `Module 25 PCB Design Rule Checks (DRCs) – [Your Name].`
   b) Add a description: `Altium Essential Training – Module 25 – [Your Name].`
   c) Open the *Advanced* section.
   d) Select the Ellipsis Button 

from the **Folder** configuration to open the *Choose Folder* Dialog.
      i) Select the folder with your name: `Project\For Attendees\[Your Name].`
      ii) Select **OK.**
   e) Change the Local Storage path if needed.
   f) Select **OK** to create the copy.
7. Wait until Altium Designer creates the copy of the project and opens the project in the *Projects* panel; this can take up to 1 minute.

For details how to Copy / Clone the predefined training project see Module 8 Making

1.4 Health Check Information

8. Open the PCB from the Project panel.
9. A health check is performed automatically when the PCB document is opened. Anytime during the design process, you can run a specific check manually by right-clicking it in the list and selecting the **Run Check** command or run all enabled checks by clicking the **Check All** button at the bottom of the list, Figure 1.
   a) Open the *Properties* panel, button **Panel** Panels at the lower right side of the workspace and select the tab *Health Check*.
   b) Use the switch **Show issues only** to reduce the list.

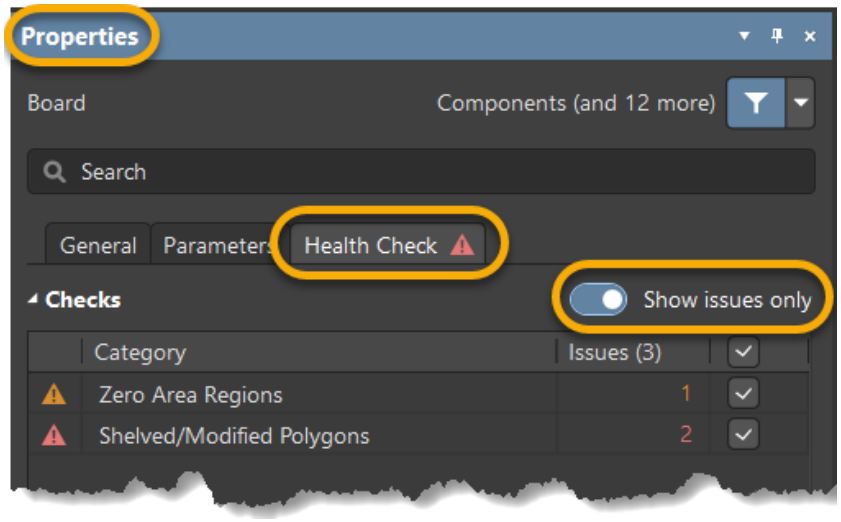

Figure 1. Health Check information for the PCB

10. The Health Check reports two issues that could be fixed automatically.
    - Zero Area Region
    - Shelved / Modified Polygons

11. Select the issue Zero Area Region
    a) Select the issue to jump to the Board Area where the Zero Area Region exist, Figure 2. You will not see the Zero Area Region.

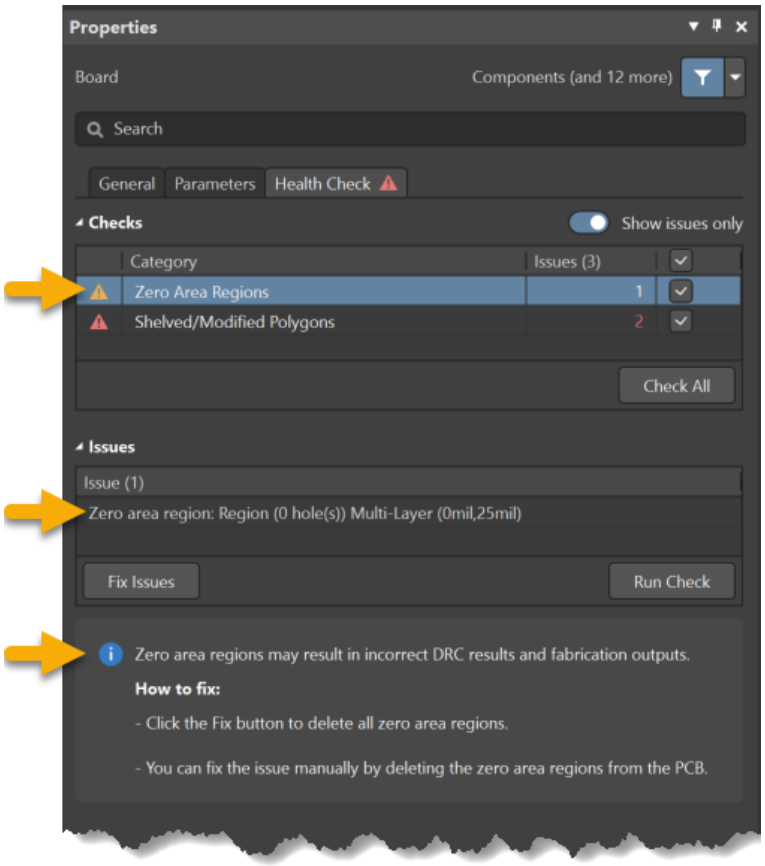

Figure 2. PCB Health Check with reported Issue

    b) Clear the masking with **Shift+C** and change back to the *Properties* panel with Health Check tab selected.
    c) Click on **Fix Issue** to automatically remove the Zero Area Region.
12. Select the remaining Issue *Shelved/ Modified Polygons* and click on **Fix Issue** to restore and repour the Polygons.

Think about other ways how you could find / list that Zero Area Region.

1.5 Design Rule Check

13. Go to **Tools » Design Rule Check…** to open the *Design Rule Checker*.
    a) Enable the **Create Report File** and **Create Violations** options.
    b) Click the **Run Design Rule Check…** button as shown in Figure 3.

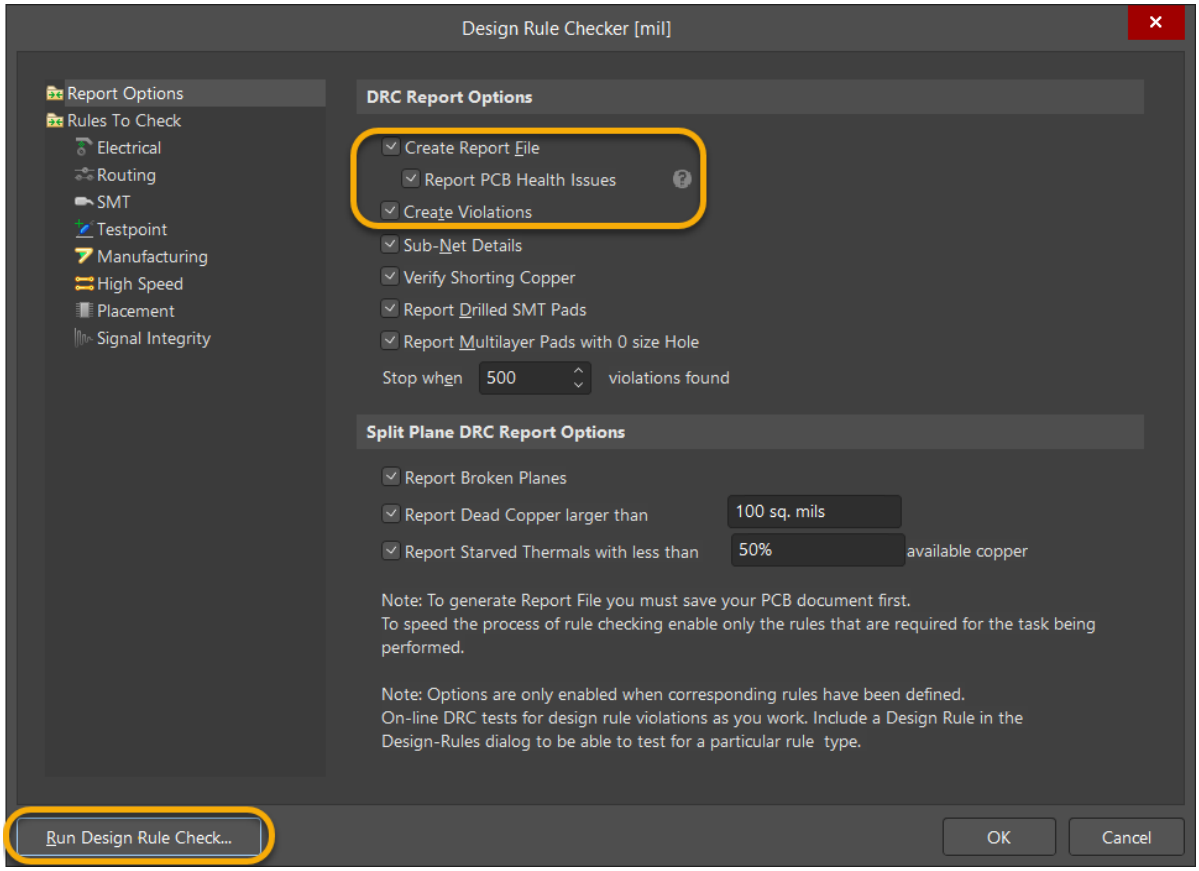

Figure 3. Design Rule Checker

14. If the *Messages* panel appears, feel free to close it for now.
15. The Design Rule Verification Report should generate showing the number and the type of violations, as shown in Figure 4. Scroll down to the Rule Violations section to see the violated rules.
    a) Un-Routed Net Constraint
    b) Minimum Solder Mask Sliver
    c) Silk to Solder Mask
    d) Component Clearance Constraint

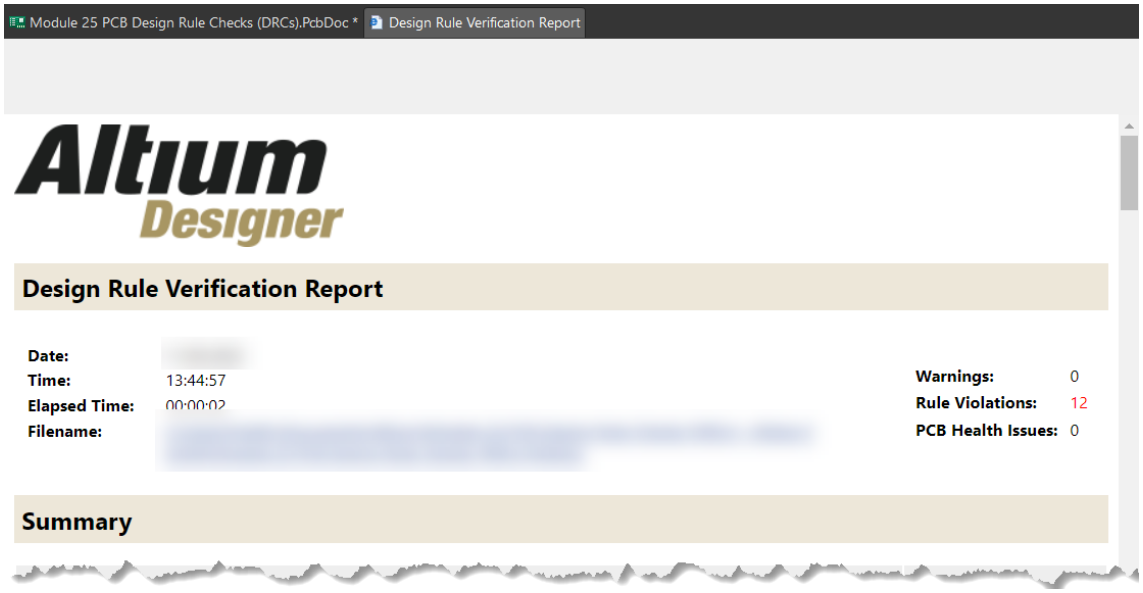

Figure 4. Rule violations in the report file

By default, the **Design Rule Verification Report** will show a maximum of 500 violations. This can be changed (increased or decreased) in the *DRC Report Options* before running the report.

16. Click on the first violation under the *Un-Routed Net Constraint* list in the report as shown in Figure 5. It should then open the PCB document and navigate to the violating area, which is near component `IOS2 / UI1`.

Figure 5. Violation List for Un-Routed Net Constraint Rule

1.6 PCB Rules and Violations Panel

17. Instead of using the report to navigate through the violations, we will use the *PCB Rules and Violations* panel while in the PCB. While in the `Module 25 PCB Design Rule Checks (DRCs).PcbDoc`, click the **Panels** button Panels and select the *PCB Rules and Violations* panel as shown in Figure 6.

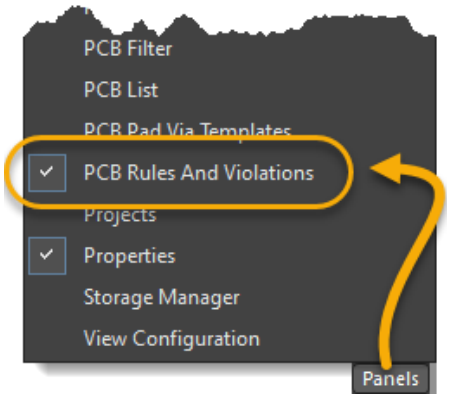

Figure 6. Opening the PCB Rules and Violations panel

18. This would open the *PCB Rules and Violations* panel. Dock this panel to the left or right of the workspace as shown in Figure 7.

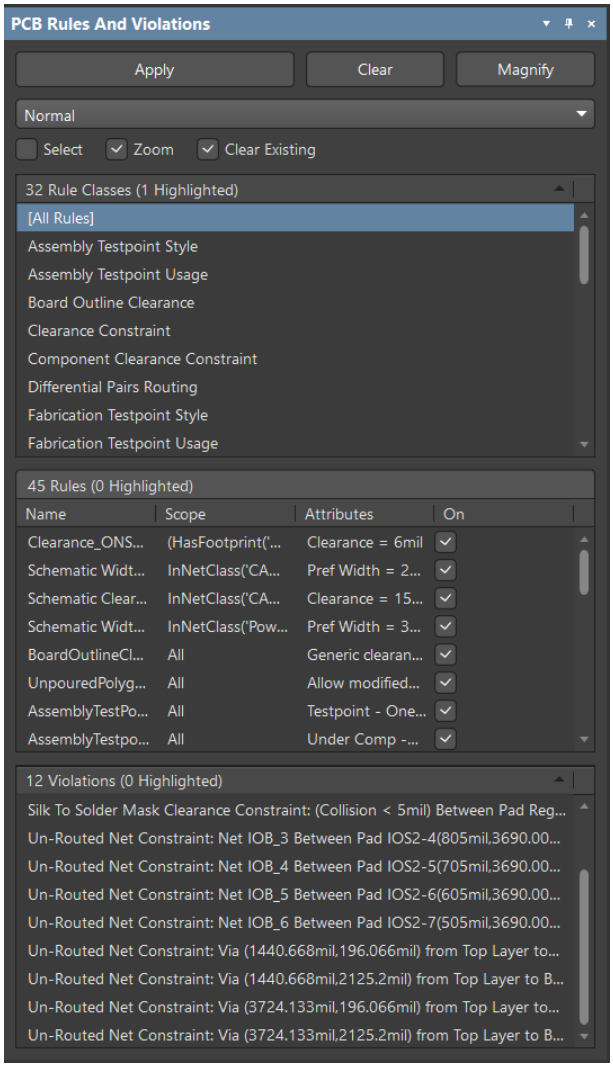

Figure 7. PCB Rules and Violations panel

19. Click on the **Component Clearance Constraint** violation in the panel, as shown in Figure 8. The order of these violations may be different for you.

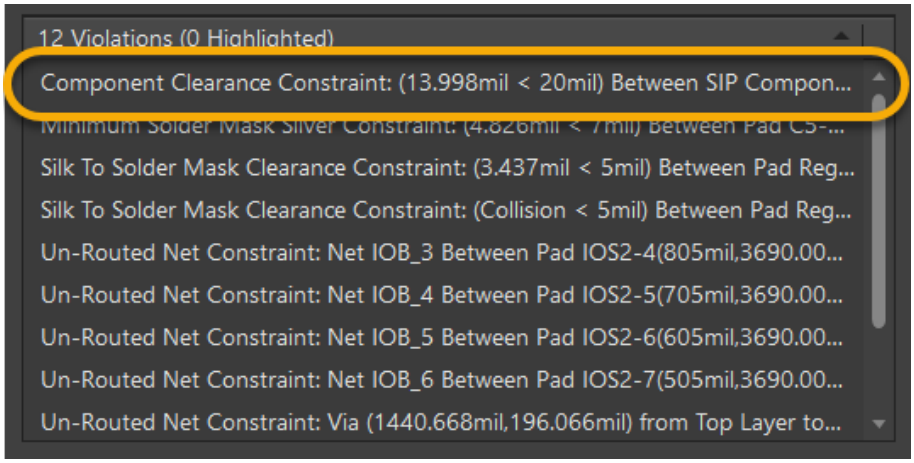

Figure 8. Component Clearance Violation

20. We would like our view to be zoomed into the violation, as well as mask the rest of the PCB to improve the visibility of the violation. In the *PCB Rules and Violations* panel, change the highlight options from **Normal** to **Mask** and enable the **Zoom** option as shown in Figure 9.

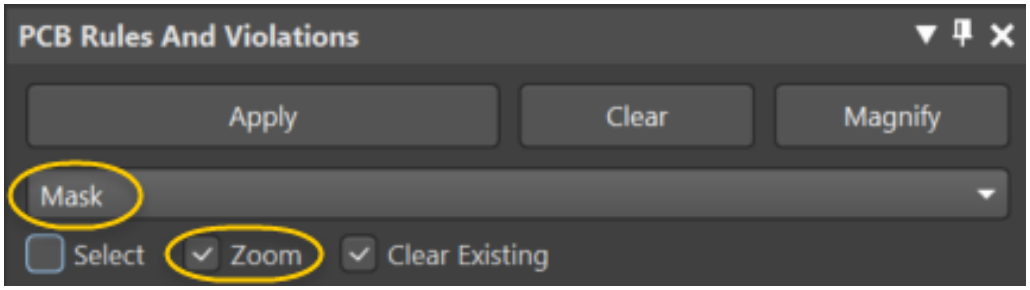

Figure 9. Mask control in the PCB Rules and Violations panel

21. Your zoom can be adjusted by clicking on the **Magnify** button and adjusting the slider to your zoom preference as shown in Figure 10.

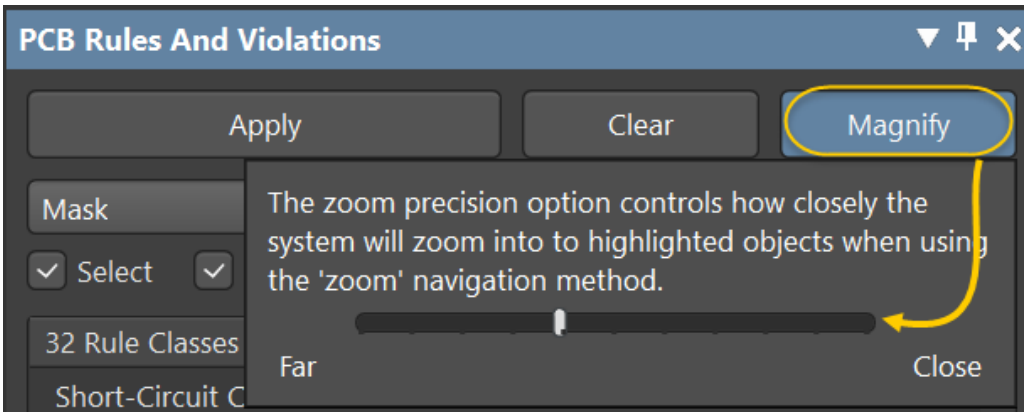

Figure 10. Adjust zoom level

22. Left-click on the **Component Clearance Constraint** violation again from *Violations* list. The workspace should zoom to the violating primitives and mask the rest of the board except for the primitives shown in Figure 11.

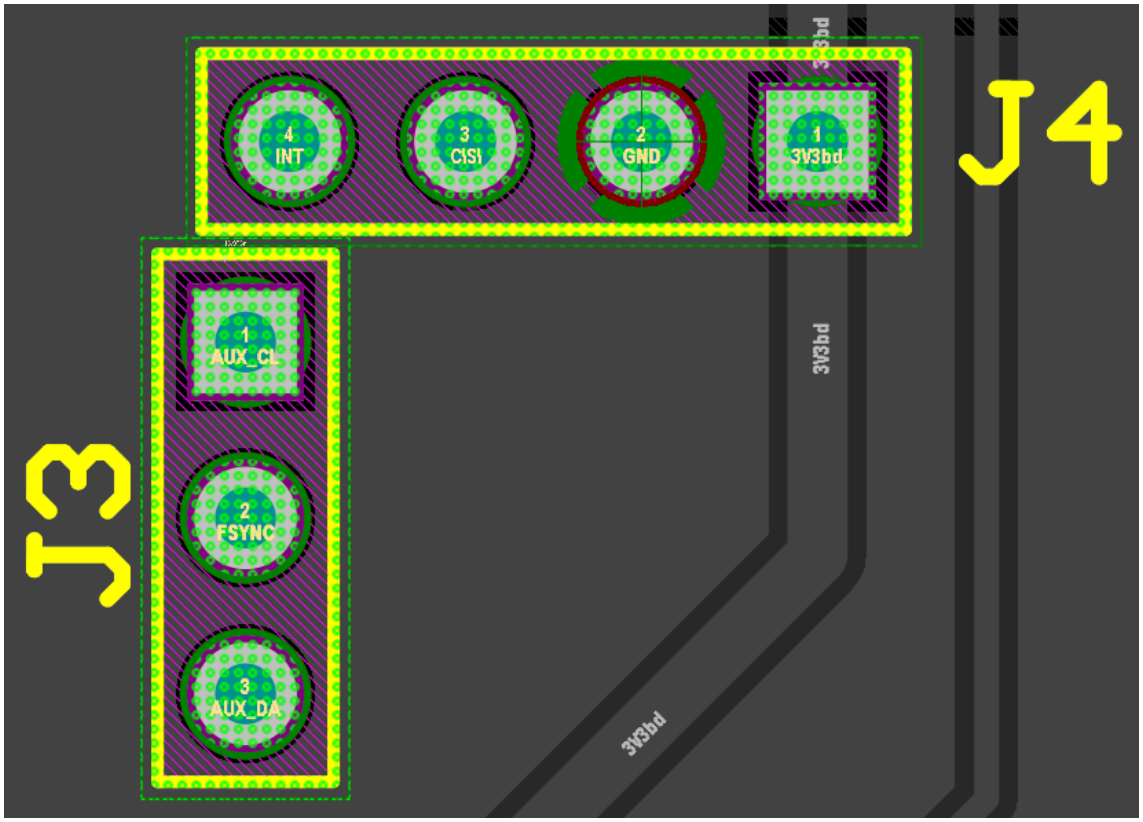

Figure 11. Violating components in the PCB

23. Enable the **Select** checkbox from the top of the *PCB Rules and Violations* panel and select the violation again. Notice that the violating primitives will now be selected.
24. To clear all the masks and selection, click the **Clear** button from the *PCB Rules and Violations* panel or hit **Shift+C** on the keyboard.

1.7 Resolving Violations

Instead of running all the rules from the Design Rule Check window as described in the previous section, we can run selected design rules from the *PCB Rules and Violations* panel.

25. Scroll down and right-click on **Un-Routed Net Constraint** in the *Rule Classes* section of the *PCB Rules and Violations* as shown in Figure 12.

1.7.1 Un-Routed Net Constraint

26. Click on the **Run DRC Rule Class (Un-Routed Net Constraint)** option from the popup menu to run the Design Rule Check.

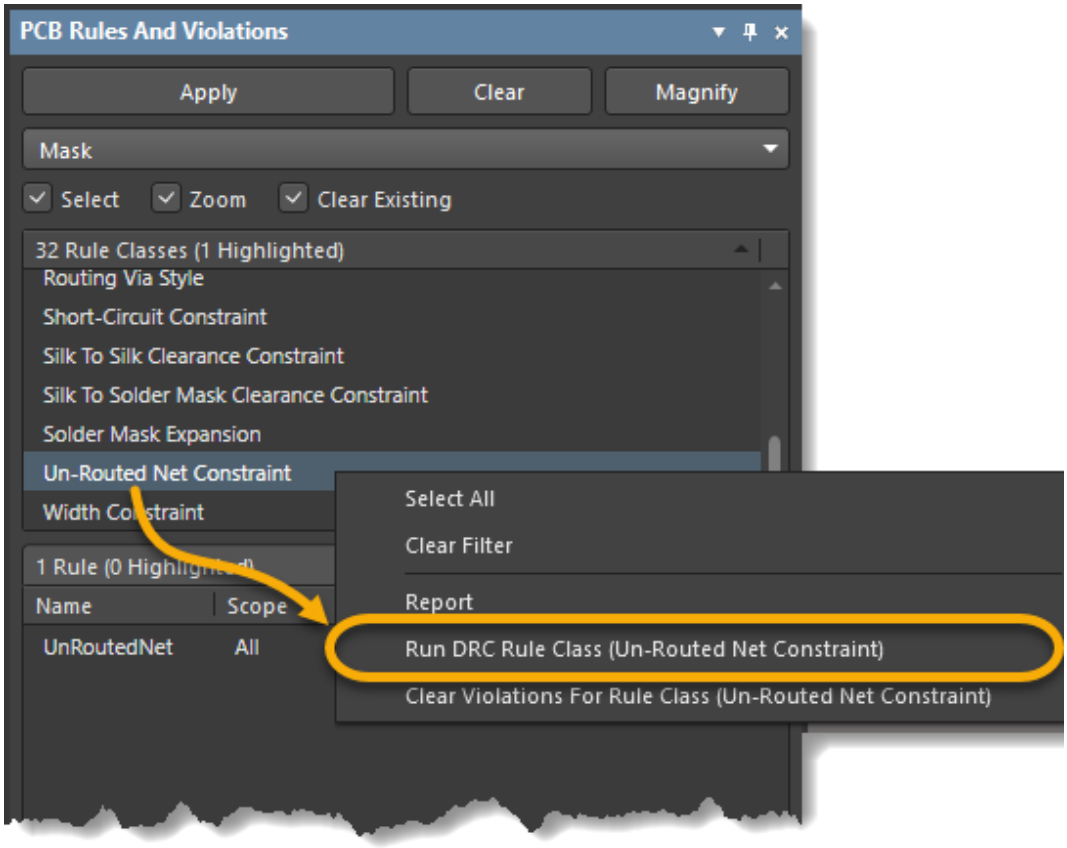

Figure 12. Rule Classes in the PCB Rules and Violations panel

27. Four (4) violations will be listed at the bottom of the *PCB Rules and Violations* panel in the *Violations* section as shown in Figure 13.

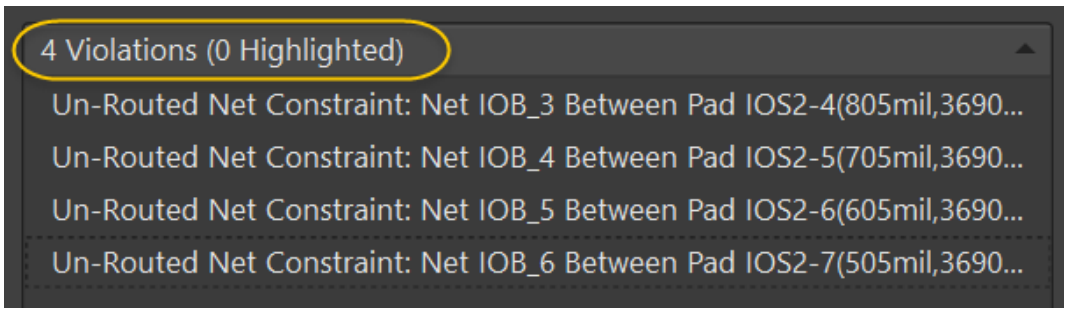

Figure 13. Un-Routed Net violations

28. In the *Violations* pane of the panel, click on any violation in the list to jump to component `IOS2`. One of the pads from `IOS2` should be highlighted along with one pad of component `UI1`, and the rest of the board is masked similar to Figure 14.

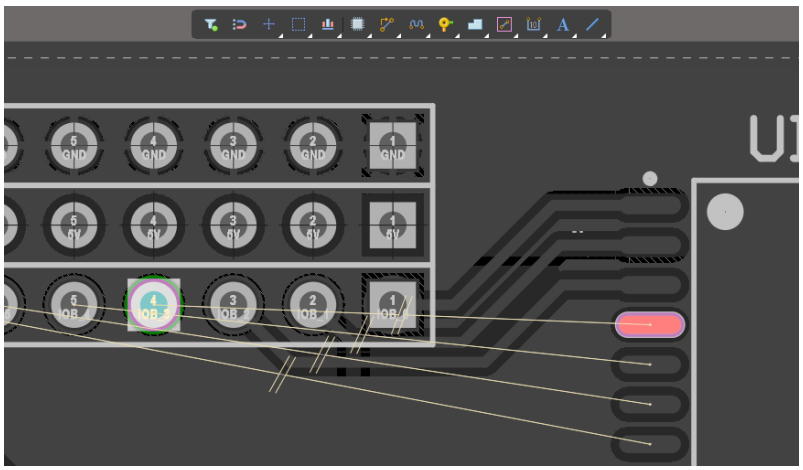

Figure 14. Highlighted violations

29. Next, we will shelf the polygon in the area of the missing connections, this will make it easier to route the missing connections.
    Feel free to skip this step to see the behavior if you route inside an existing polygon; based on the Preference settings like **Repour Polygons After Modification**.
    a) Press the Clear Button or use **Shift+C** to clear the masking.
    b) Left click on the Top Layer GND polygon to select it.
    c) **Right Click » Polygon Actions » Shelve Selected**. This will make it easier to see the routing you will do in the next step.
30. Since this is an **Un-Routed Net Constraint** violation, we will resolve it by routing a trace from the highlighted pad of `UI1` to the highlighted pad of `IOS2` with **Route » Interactive Routing**. Clearing the selection with **Shift+C** may help you see the route better.
31. Repeat the previous steps for the other three (3) Un-Routed Net Constraint violations in the *PCB Rules and Violations* panel. Ensure you have enough clearance for the rest of the connections to be routed.
32. After you're finished routing the 4 connections, restore the Polygon from the **Tools » Polygons** menu.
33. If needed, repour the polygon by going to **Tools » Polygon Pours » Repour All**. The polygon will then look similar to Figure 15 . Your polygon may repour automatically if that *Preference* option is enabled.
34. Rerun the check **- Run DRC Rule Class (Un-Routed Net Constraint).** No Violation will be reported after you routed the connection.

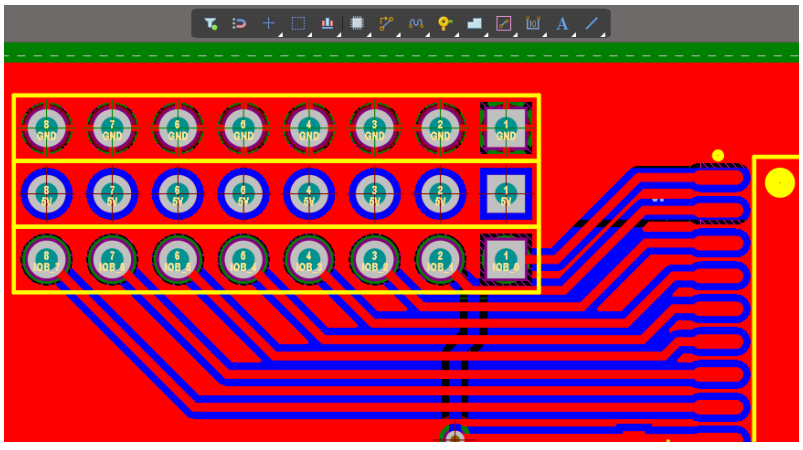

Figure 15. Routed nets with the repoured polygons

1.7.2 **Component Clearance Constraint**

35. Go to **Tools » Design Rule Check…** and click **Run Design Rule Check...** .
36. The *Design Rule Verification Report* should now show eight (8) rule violations as shown in Figure 16.

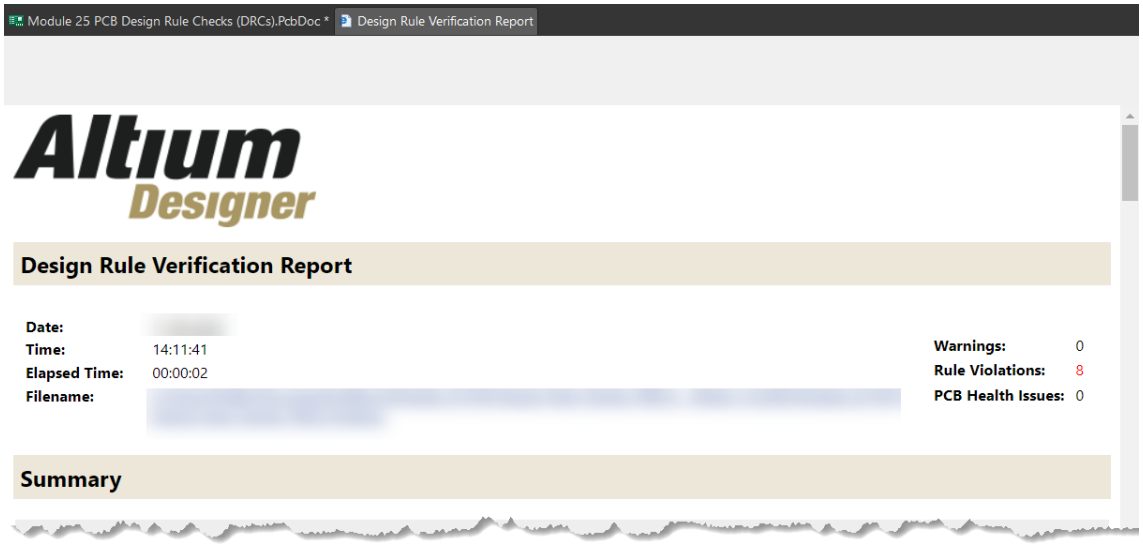

Figure 16. Design Rule report

37. Back in the PCB, select the **Component Clearance Constraint** rule class from the *Rule Class* section, to view its 3 rules and the Component Clearance Violation <20mil as shown in Figure 17.
38. Double-click on the rule named *"Component Clearance"* with the Scope **All – All**. The *Edit PCB Rule – Component Clearance* window should open. The order of these rules may vary for you.

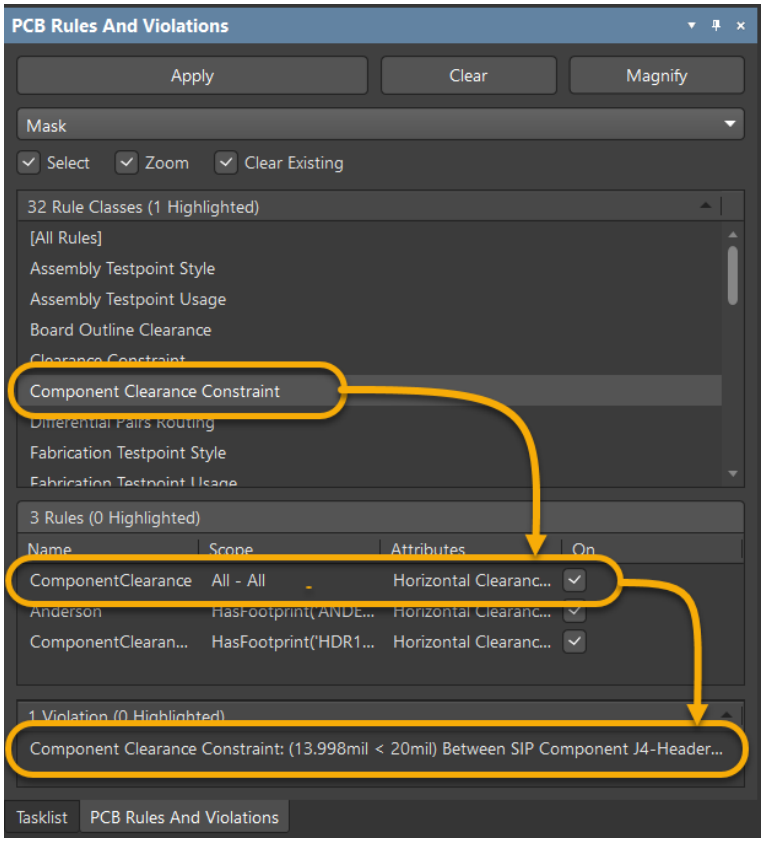

Figure 17. Component Clearance rule class

39. Notice the **Minimum Horizontal Clearance** is set at `20mil` as shown in Figure 18.
40. Click **OK** to close the window.

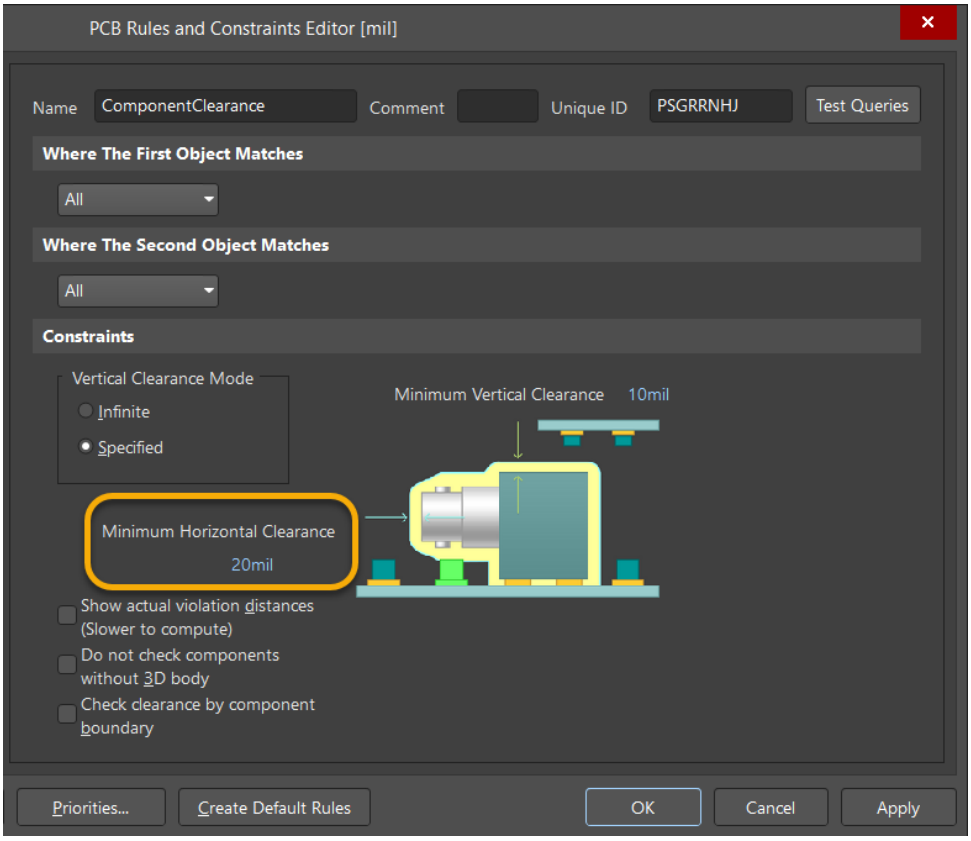

Figure 18. Editing the Component Clearance design rule

41. Let's resolve this violation by creating a new component clearance rule.
42. Open the Design Rules menu **Design » Rules,** add a new **Placement – Component Clearance** Rule, see Figure 19.

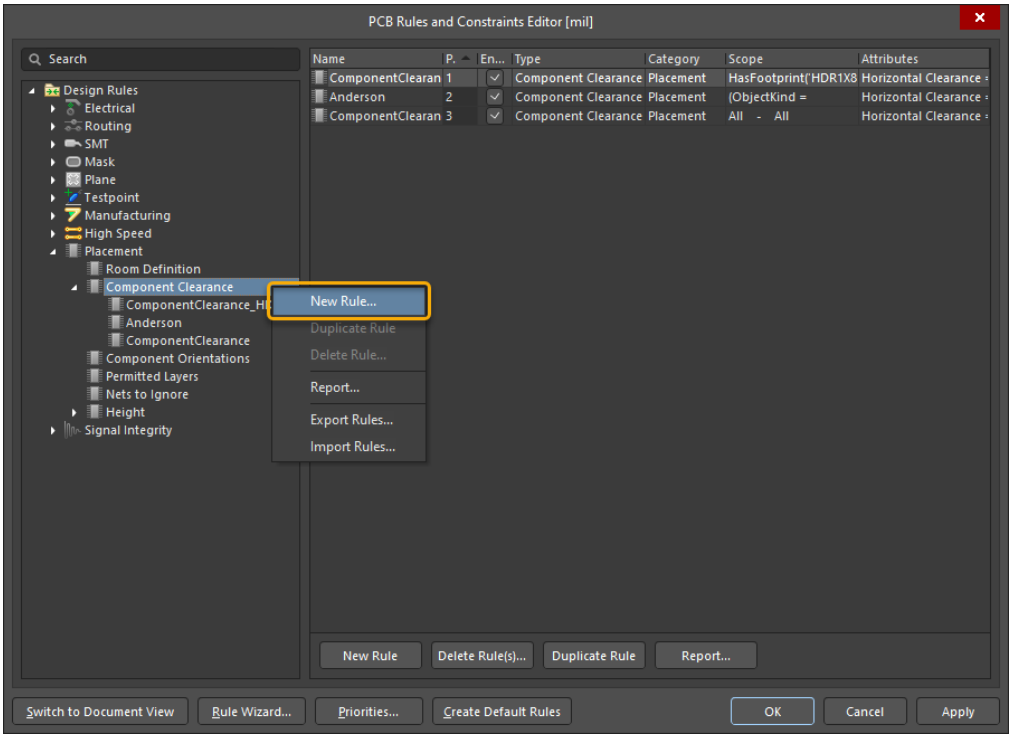

Figure 19. Placement Rule

43. Use Figure 20 as reference to add the information required.

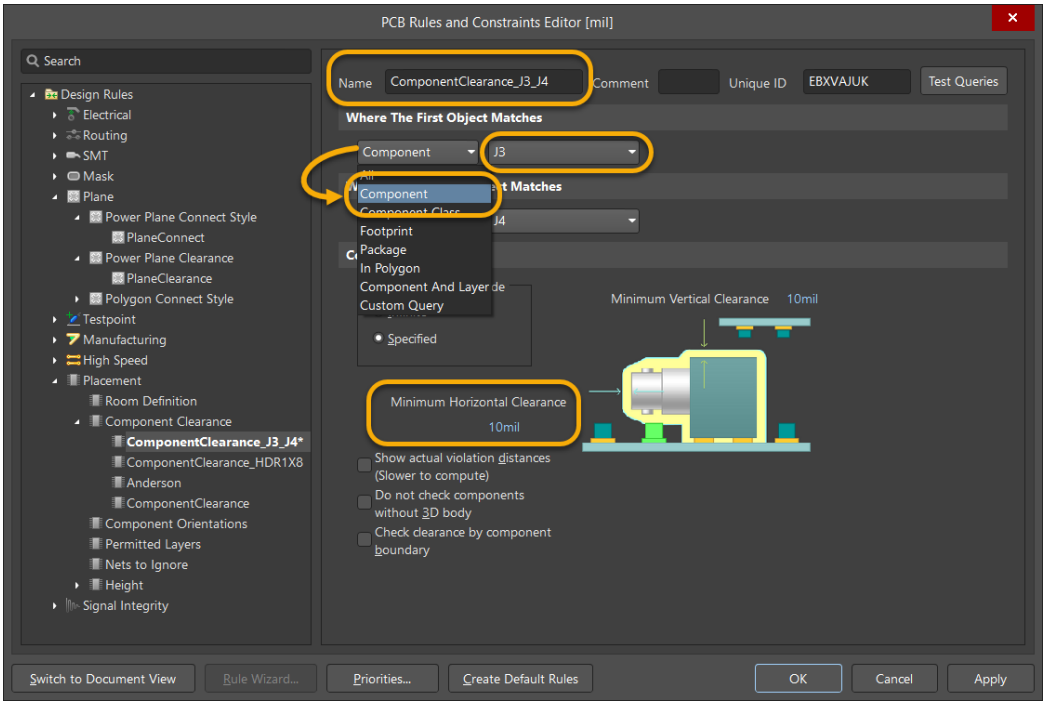

Figure 20. Where The First Object Matches

a) Change the name to: `ComponentClearance_J3_J4`

b) Change the **Minimum Horizontal Clearance** to `10mil`.

c) From the **Where The First Object Matches** section, select **Component** from the drop-down list, and then select **J3** from the second dropdown list.

d) Repeat this for the **Where The Second Object Matches** section, do the same as above and select **J4,** see Figure 21.

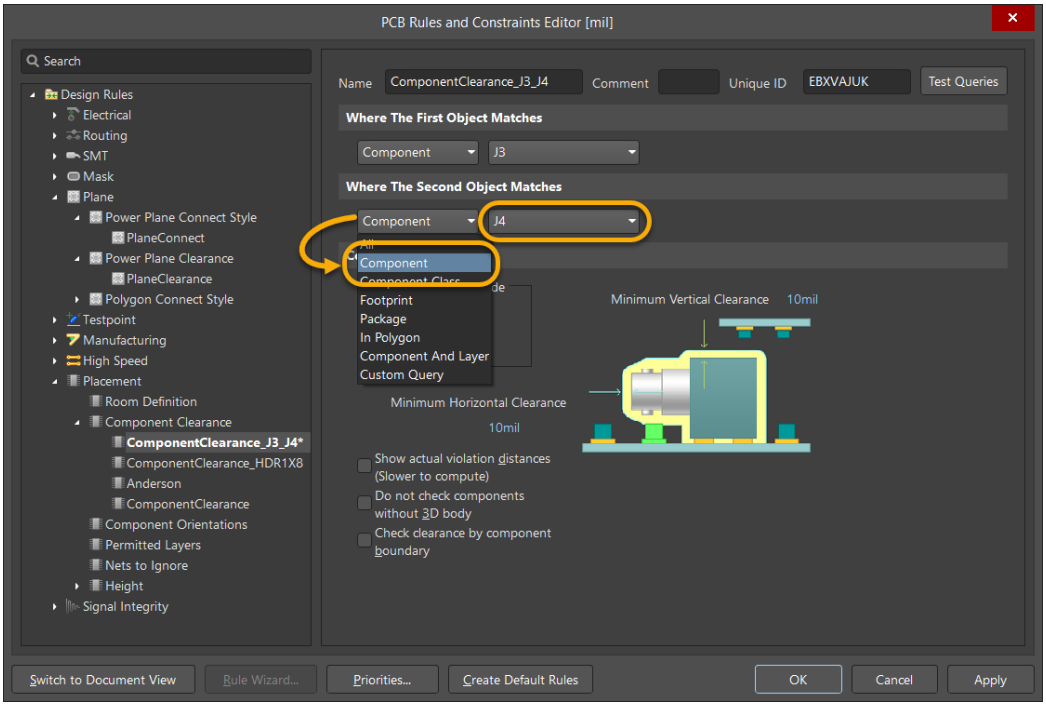

Figure 21. Where The Second Object Matches

44. The new rule just added will now take a higher priority than all other rules, as it is the latest rule added to the ***Component Clearance*** rules.

45. Select **OK** and close the *PCB Rules and Constraints Editor*.

1.7.3 **Waive Violations - Un-Routed Net Constraint: Via**

46. Run the **Design Rule Check…** again from the **Tools** menu. The Design Rule Check should now indicate seven (7) violations.
47. Return to the PCB document. Select **[All Rules]** from the *Rule Class* section to view the seven (7) remaining violations.
48. Group select the four violations, `Un-Routed Net Constraint: Via …` . The four Vias act as Mounting Holes in this PCB.
49. We will accept these Violations by right mouse click on the violations to open the *Waive Selected Violation* dialog with the *Waived Violation Info* option and enter details like shown in *Figure* 22.

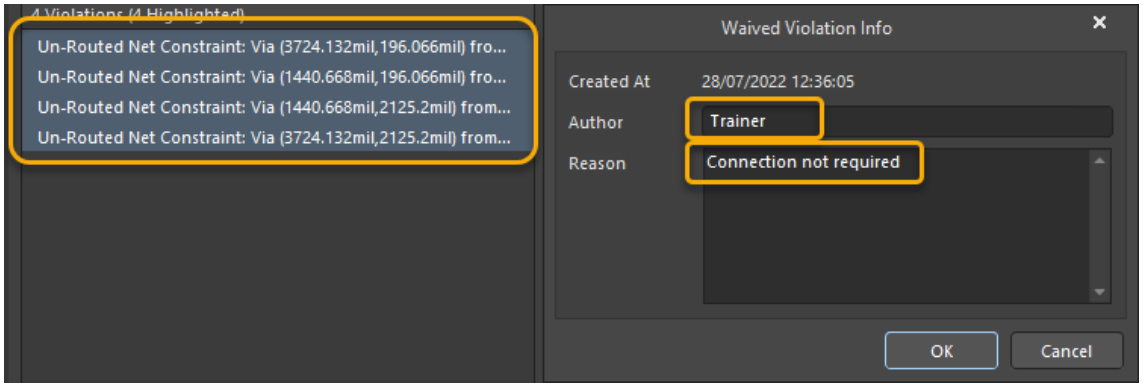

Figure 22. Waive a Violation

1.7.4 **Solder Mask Violations**

50. Return to the PCB Rules and Violations panel. Select **[All Rules]** from the *Rule Class* section to view the three (3) remaining violations.
51. Select each of the violations to see different primitives highlighted near the same pad as shown in Figure 23.

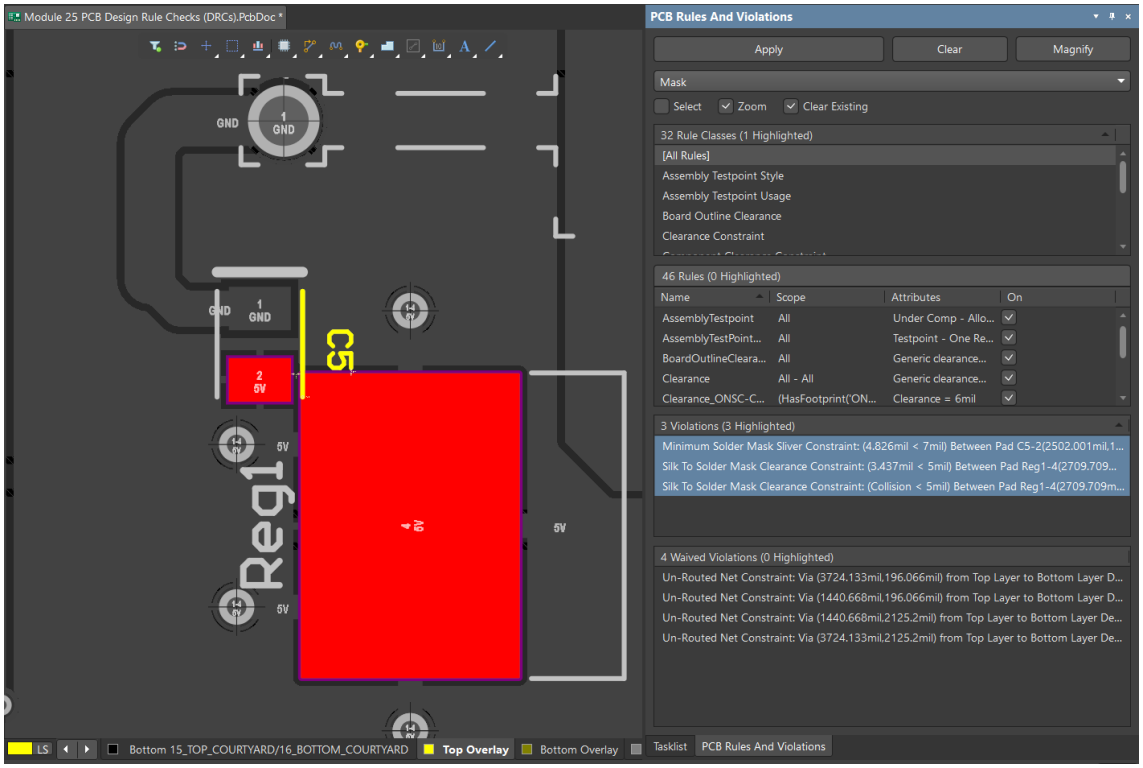

Figure 23. Remaining violations

52. Open the Preferences and navigate to *PCB Editor* branch and open the *Interactive Routing* page.
53. Activate the option **Component re-route,** as shown at Figure 24.
54. Close the *Preferences* with **OK.**

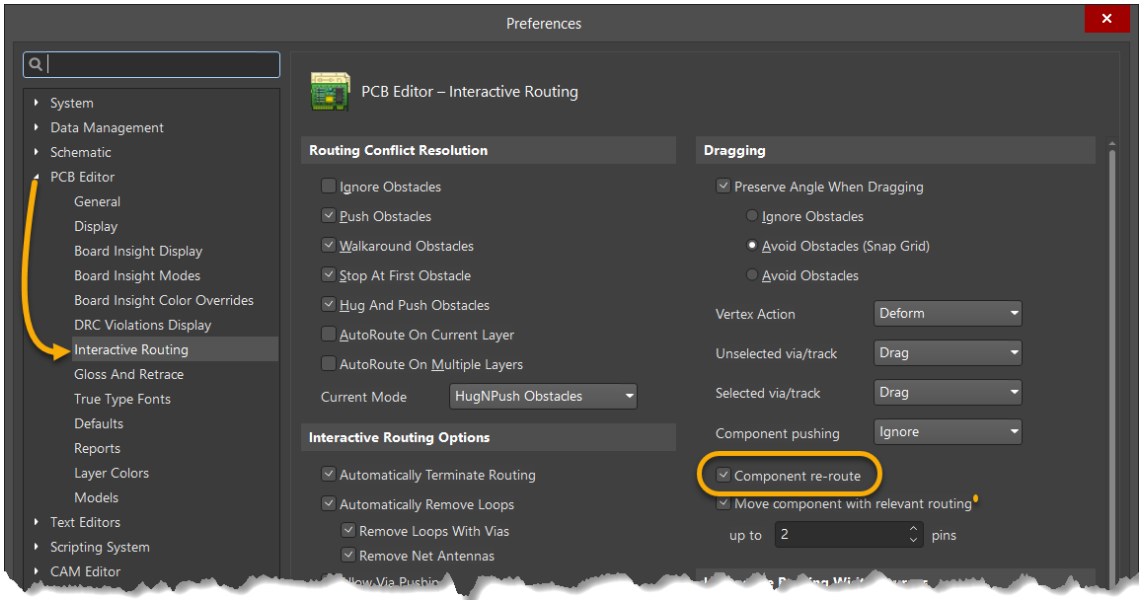

Figure 24. Preferences with active Component re-route

55. Make the Top Layer the active layer from the layer bar.
56. Click the **Clear** button from the *PCB Rules and Violations* panel.
57. Move component `C5` to the left so that it is no longer overlapping the violating pad of `Reg1` as shown in Figure 25.

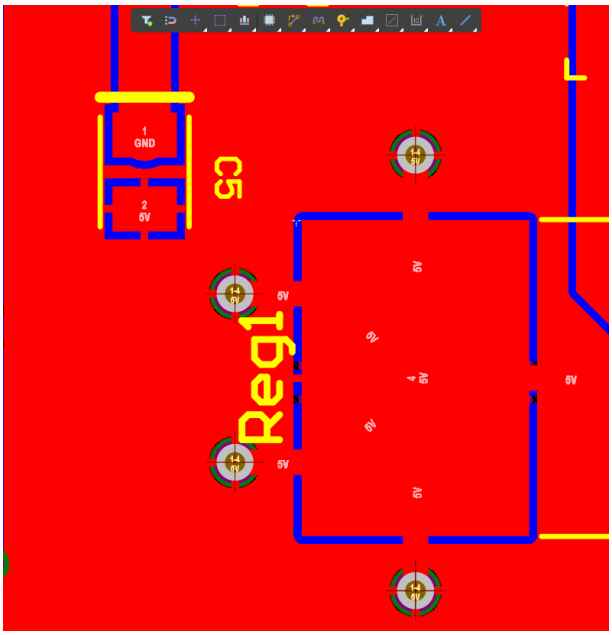

Figure 25. Move C5 to resolve violations

58. Altium start an automatic Re-route from `Pad 1` of component `C5` to the **GND** Pad that it was just connected to so that it looks similar to Figure 25. Feel free to first Shelf the Polygon.
59. If needed, repour the polygon by going to **Tools » Polygon Pours » Repour All**. Your polygon may repour automatically if that *Preference* option is enabled.

60. Run the **Design Rule Check** again and ensure there are 0 violations.
61. The Report will now include the four waived violations, see Figure 26.

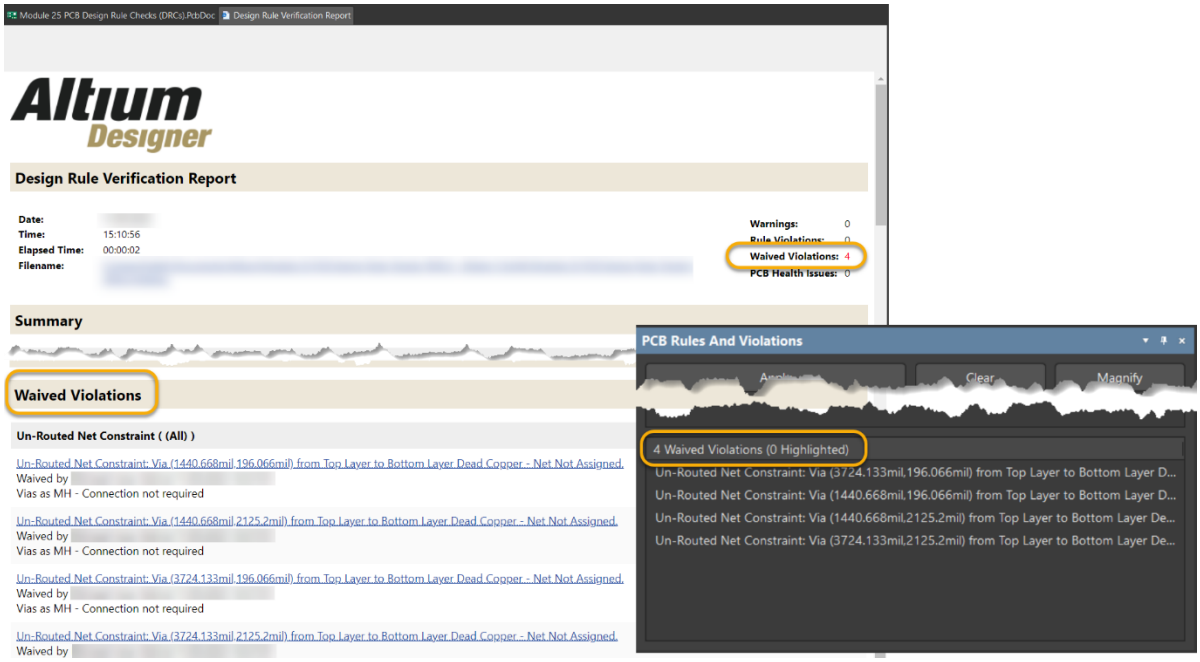

Figure 26. Report with Waived Violation

62. Save all documents using **File » Save All**.
63. Save the modifications to the server:
    a) At the *Project* panel, next to the Project name you find the command **Save to Server** 

.
    b) Select **Save to Server.**
    c) At the dialog *Save [Project Name]*.
        i) Activate the checkboxes for the files that are not under version control.
        ii) Add the comment `Module 25: PCB Design Rule Checks (DRCs) - [Add Your Name]- Finished`.
        iii) Select **OK.**
64. **When ready, close the project and any open documents. Window » Close All**.

Congratulations on completing the Module!

Module 25: PCB Design Rule Checks (DRCs)

from the

Altium Designer Essential Course
with Altium 365

Thank you for choosing Altium Designer