**CSE 3203 CT 4 Assignment**

**Roll No: 1803108**

**Assignment Problem:**

**Build CPU based on following requirements:**

1. **Word Size of CPU = 6**
2. **ALU Operations = AND, ADD, ROR**
3. **Register Number = 5**
4. **Size of RAM = 10**
5. **Word size of ISA and RAM = 16**
6. **CPU Instructions = Register Mode, Immediate Mode, JMP, JL**

**Solution:**

**Simulator Design:**

1. **ALU Circuit (Top to Bottom all circuits):**
2. **Register Set Circuit (Top to Bottom all circuits):**
3. **RAM Circuit (Top to Bottom all circuits):**
4. **ISA**
5. **CPU (Top to Bottom all circuits):**

**Verilog Code:**

1. **ALU Circuit (Top to Bottom all circuits):**

|  |
| --- |
|  |

1. **Register Set Circuit (Top to Bottom all circuits):**

|  |
| --- |
|  |

1. **RAM Circuit (Top to Bottom all circuits):**

|  |
| --- |
|  |

1. **CPU (Top to Bottom all circuits):**

|  |
| --- |
|  |