**CSE 3203 CT 4 Assignment**

**Roll No: 1803108**

**Assignment Problem:**

**Build CPU based on following requirements:**

1. **Word Size of CPU = 6**
2. **ALU Operations = AND, ADD, ROR**
3. **Register Number = 5**
4. **Size of RAM = 10**
5. **Word size of ISA and RAM = 16**
6. **CPU Instructions = Register Mode, Immediate Mode, JMP, JL**

**Solution:**

**Simulator Design:**

1. **ALU Circuit (Top to Bottom all circuits):**

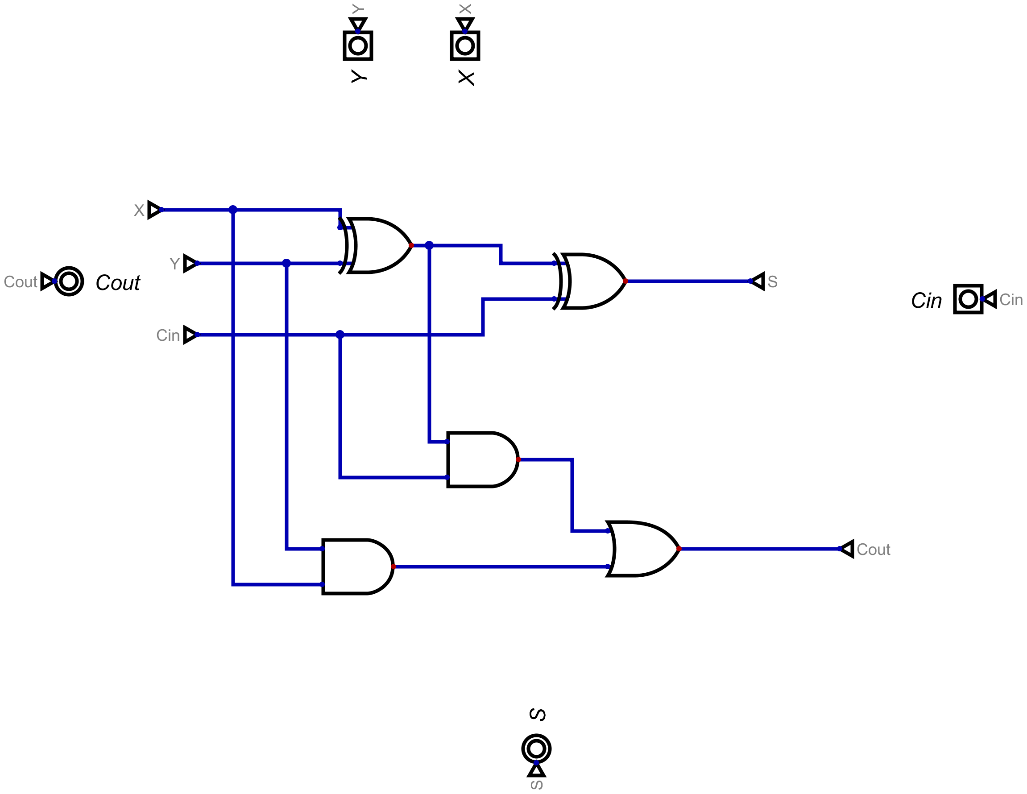
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Figure : 1 Bit Full Adder

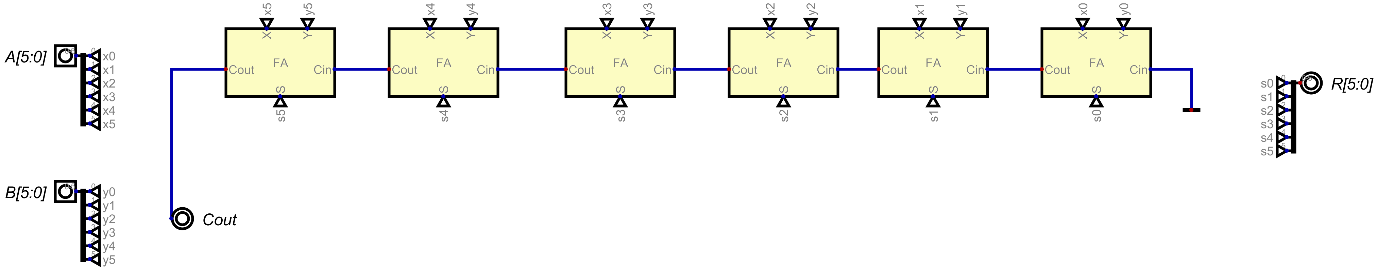
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Figure : 6 Bit Adder

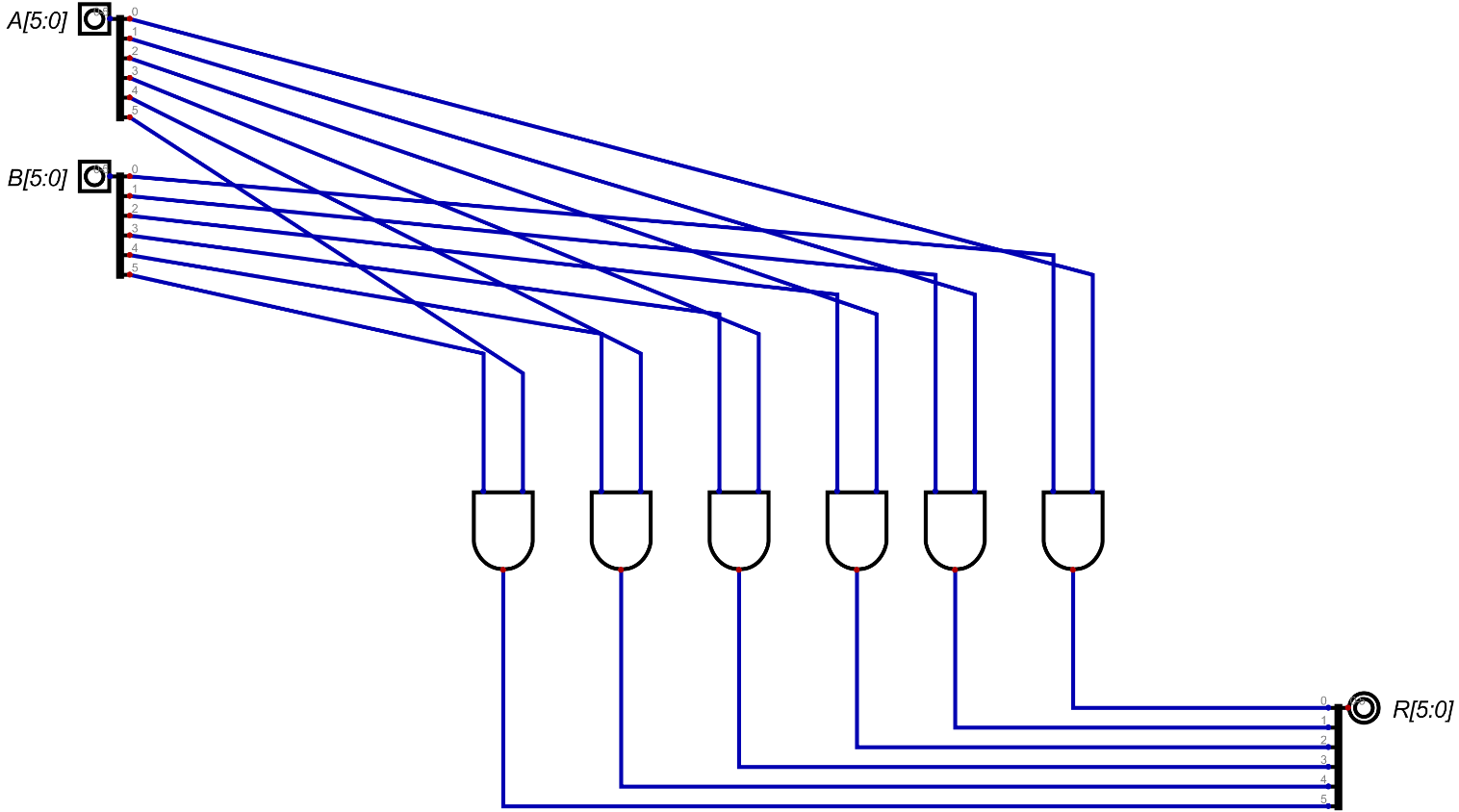
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Figure : 6 Bit And Circuit Block

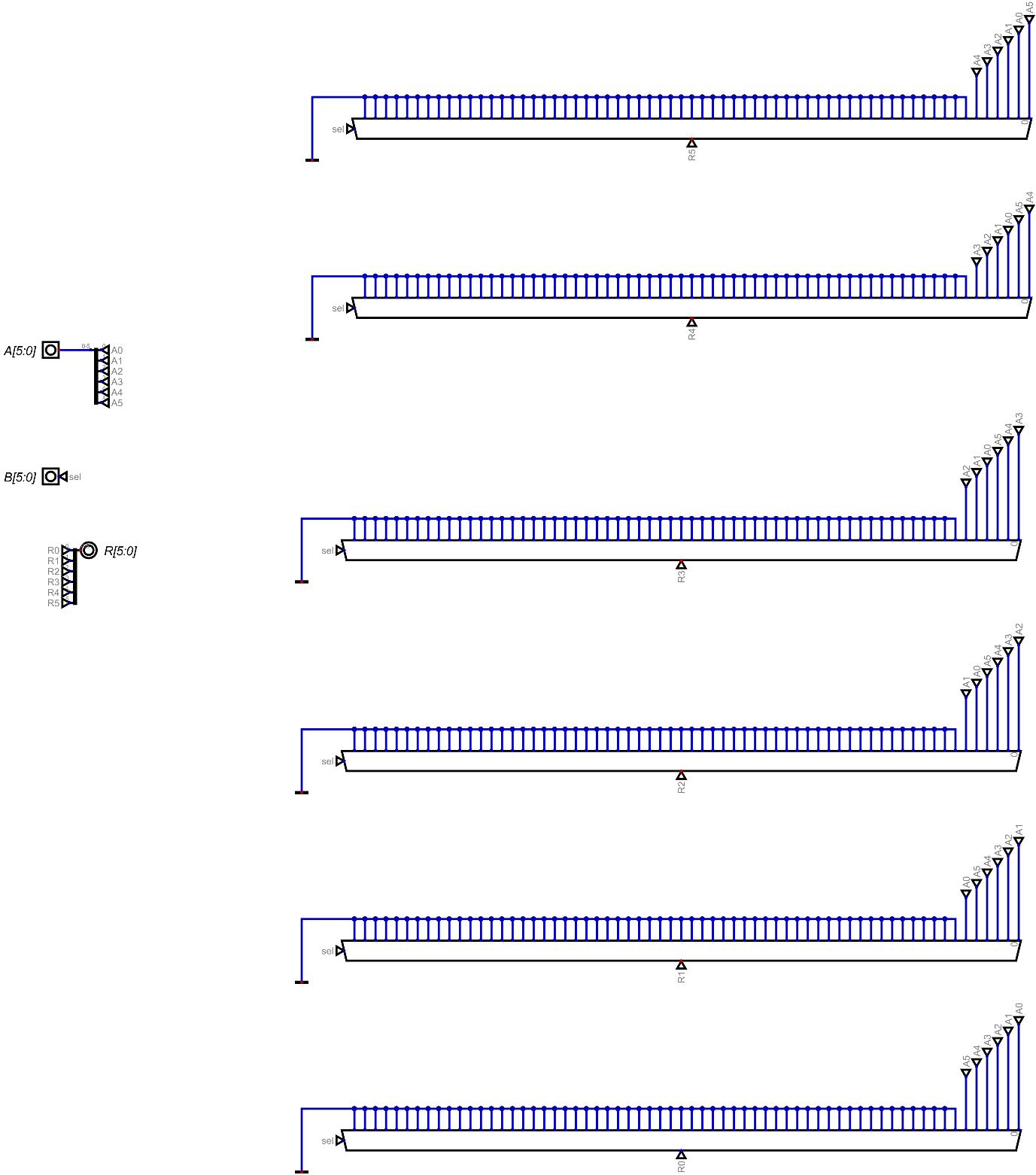
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Figure : 6 Bit Right Rotator

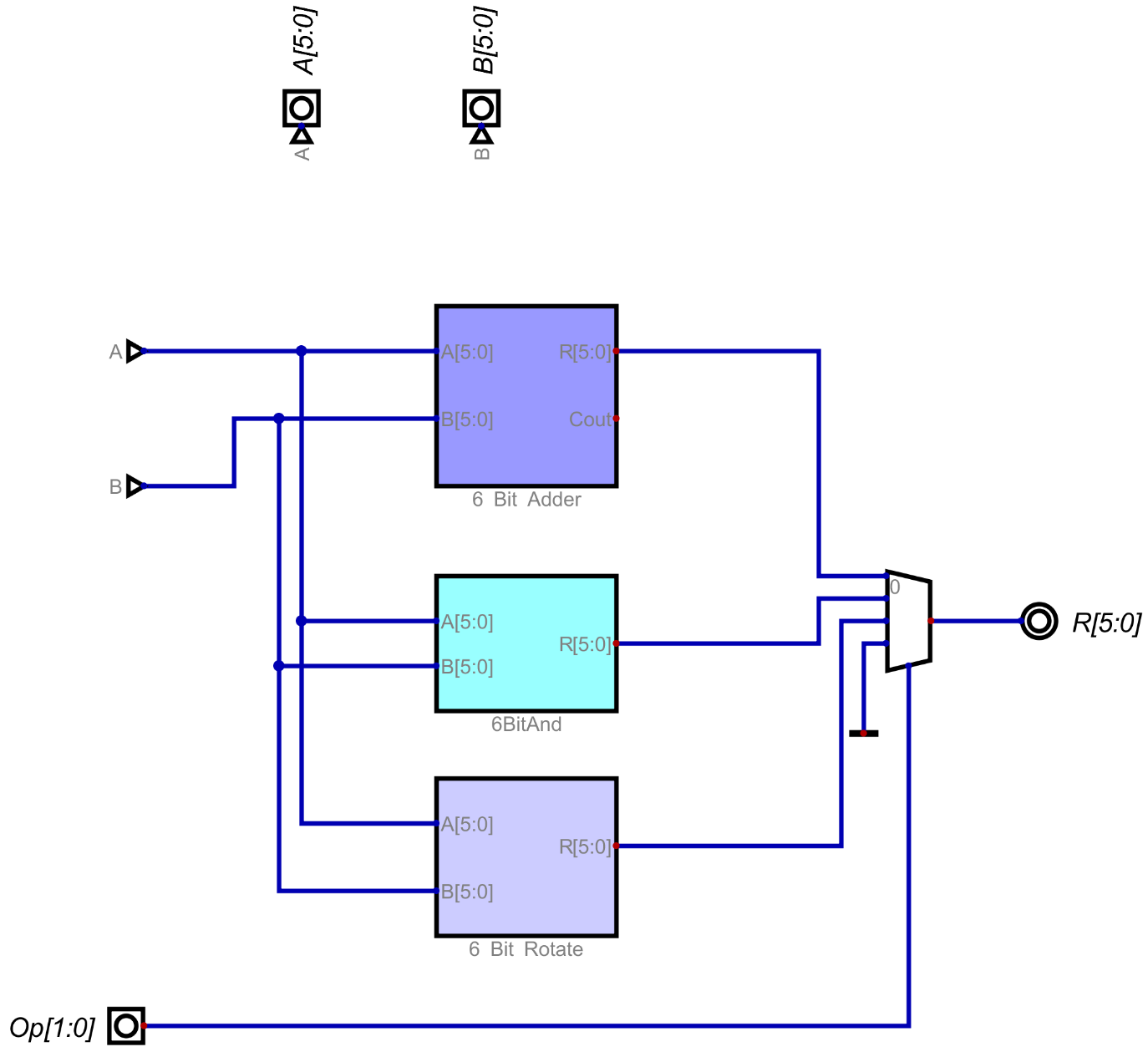
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Figure : 6 Bit ALU

1. **Register Set Circuit (Top to Bottom all circuits):**

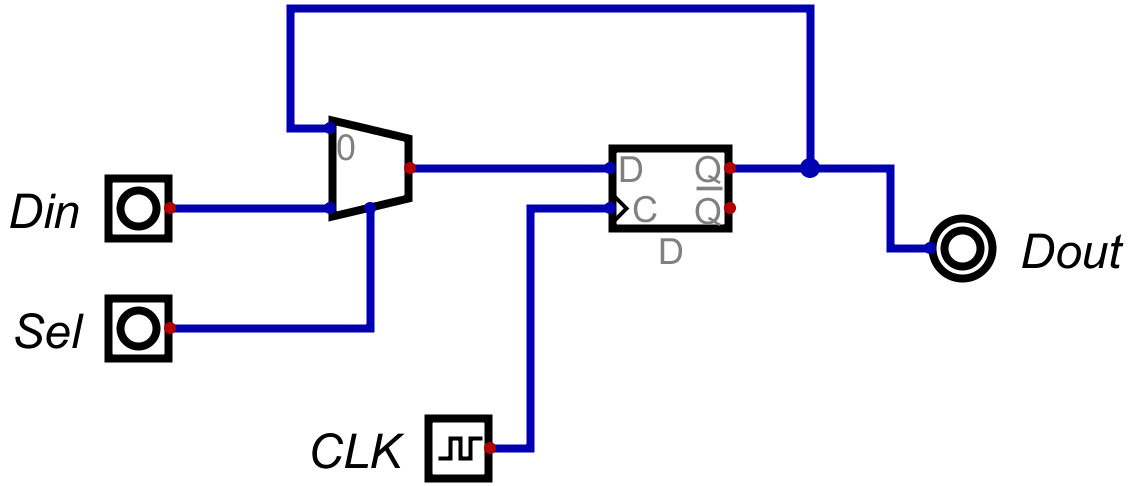
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Figure : 1 Bit Register

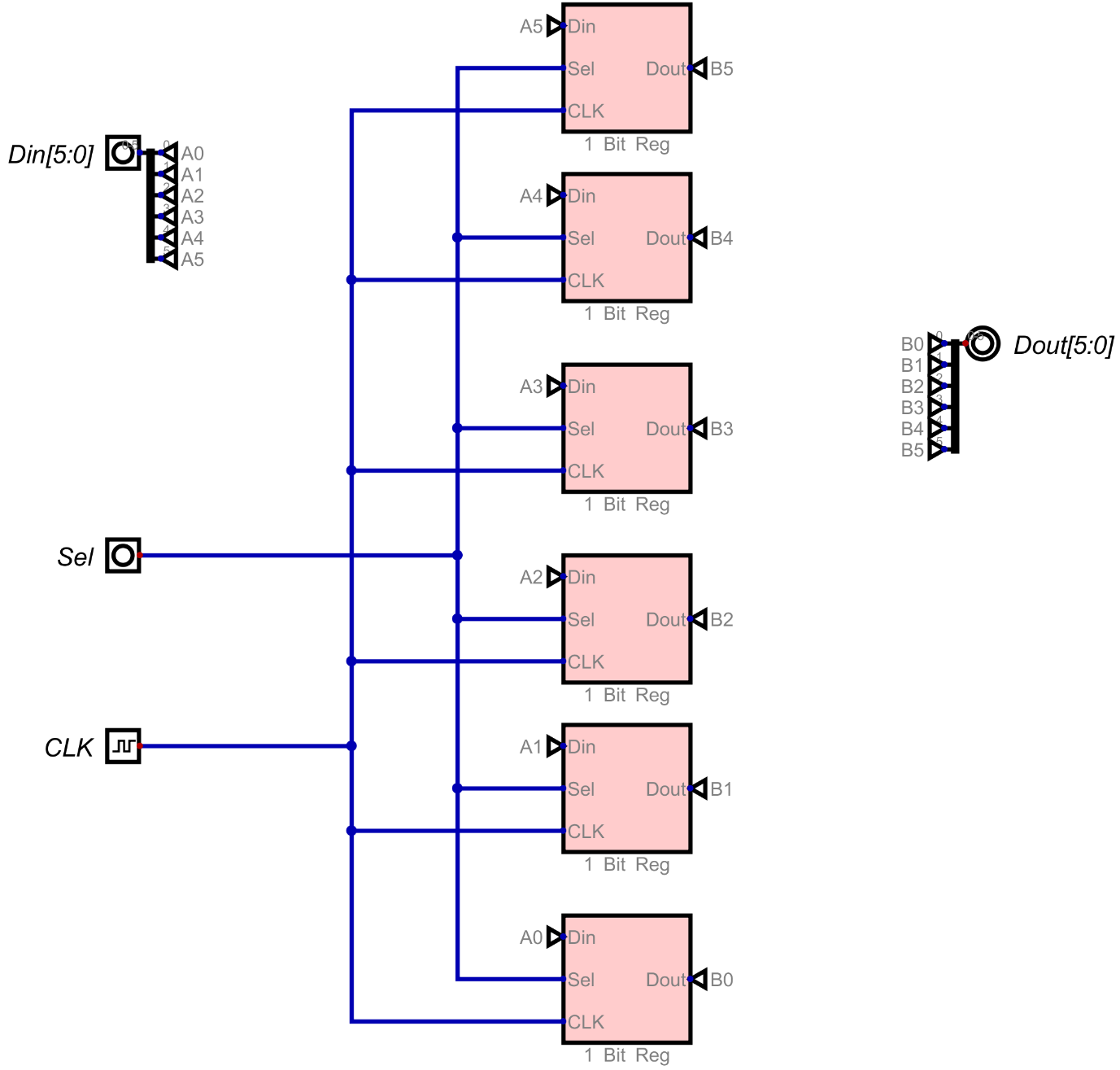
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Figure : 1x6 Bit Register

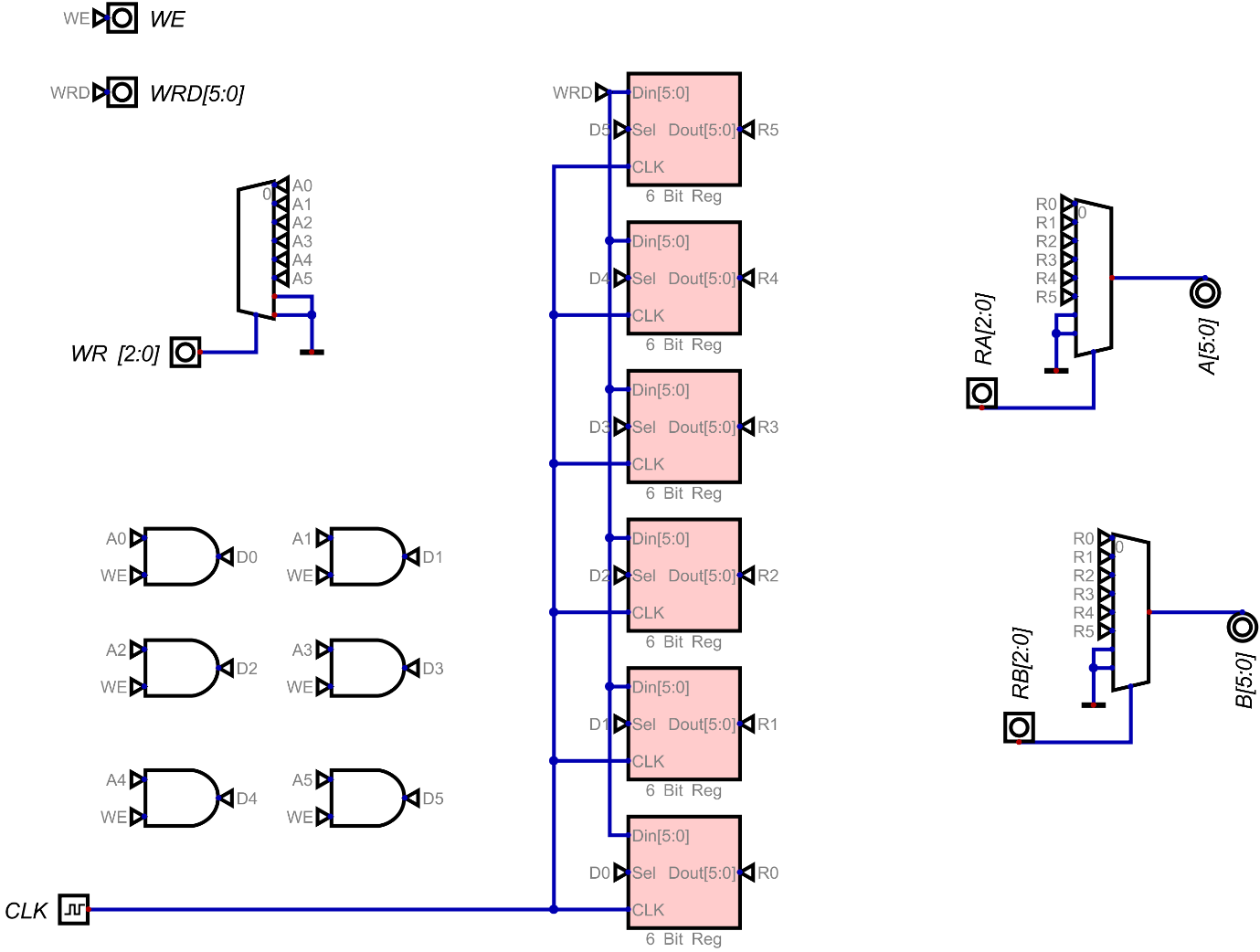
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Figure : 5x6 Bit Register Set

1. **RAM Circuit (Top to Bottom all circuits):**

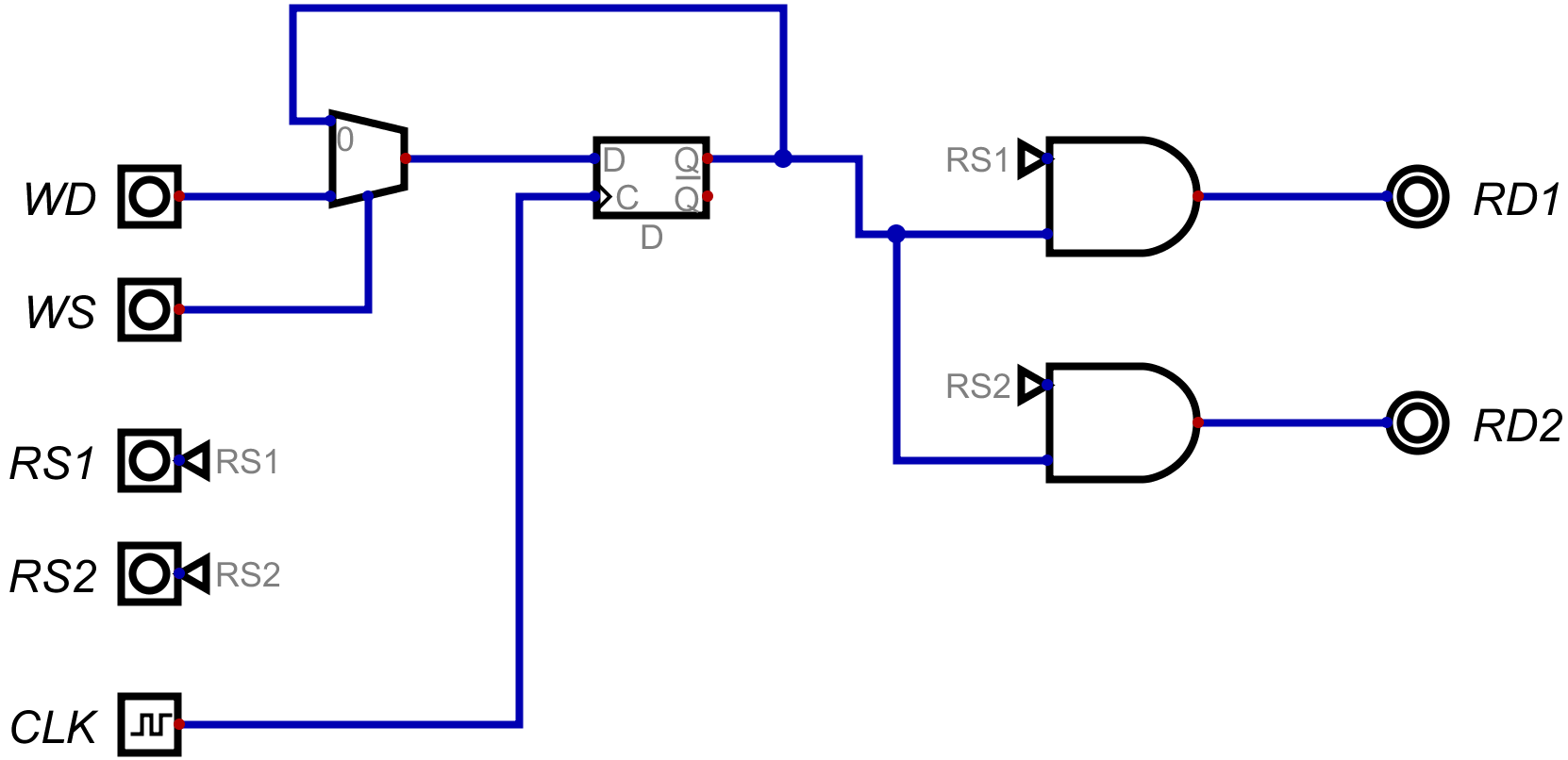
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Figure : 1 Bit RAM

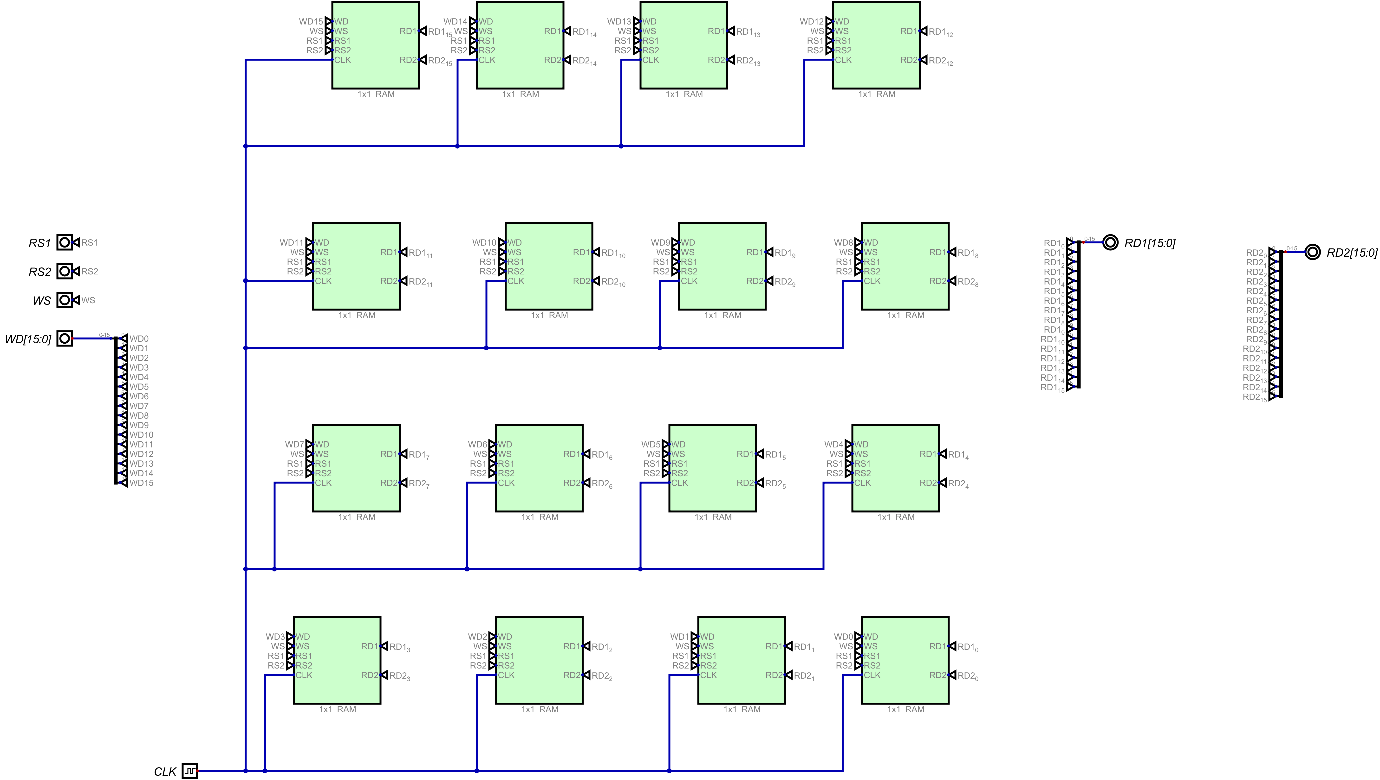


Figure : 1x16 Bit RAM

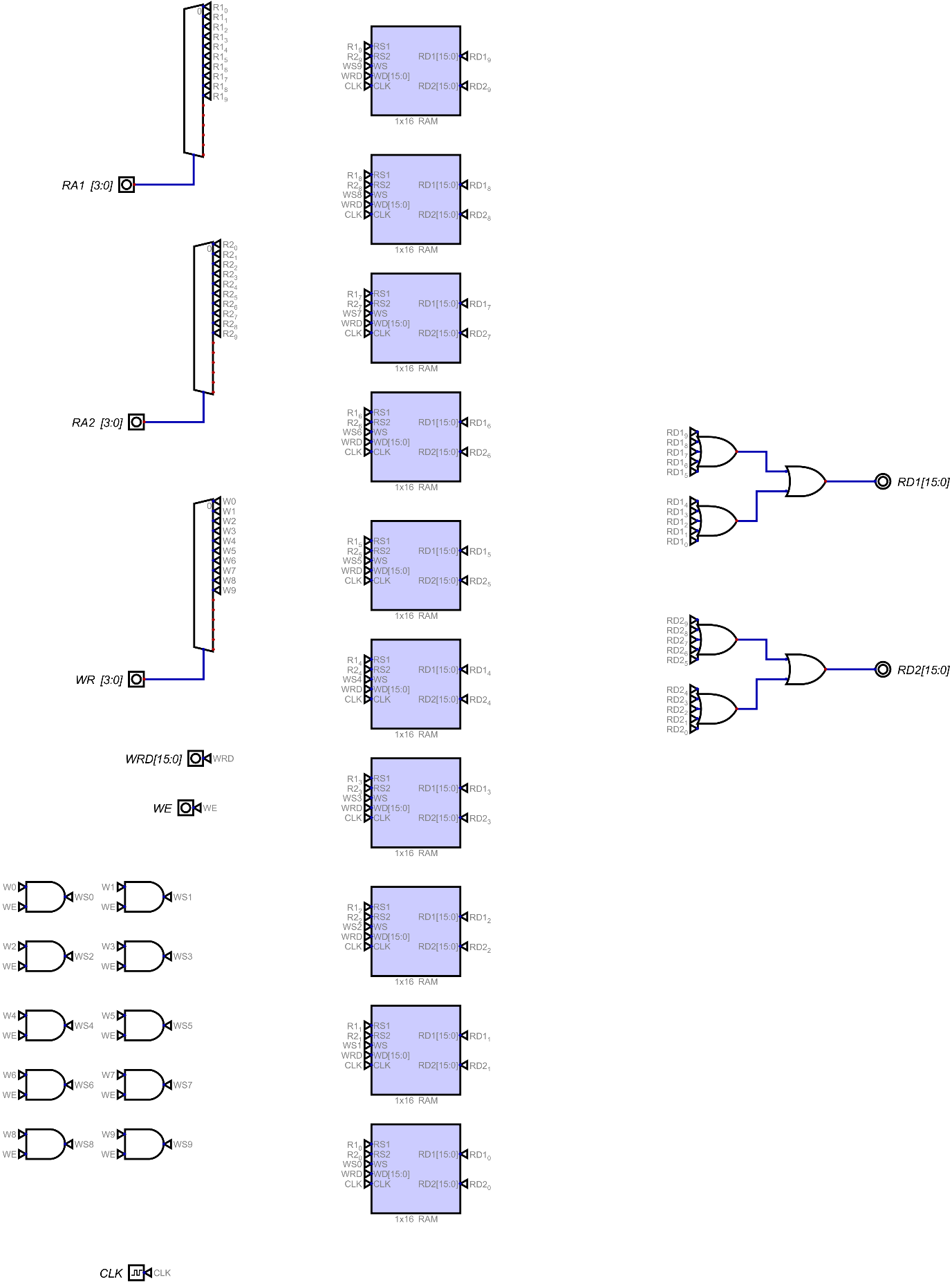
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Figure : 10x16 Bit RAM

1. **ISA**

**6 BIT CPU ISA**

**===========================================================**

**REG Mode (00) = 2 Bit (Type of OP) + 2 Bit (Operation) + 3 Bit (Reg 1) + 3 Bit (Reg 2) + 6 Bit unused**

**Immediate Mode (01) = 2 Bit (Type of OP) + 2 Bit (Operation) + 3 Bit (Reg 1) + 6 bit data + 3 Bit unused**

**Branching Mode (10) = 2 Bit (Type of OP) + 2 Bit (Operation) + 4 Bit JMP Labe + 8 Bit Unused**

**OP CODES**

**=============**

**ADD = 00**

**AND = 01**

**ROR = 10**

**JMP = 10 00**

**JL = 10 01**

1. **CPU (Top to Bottom all circuits):**

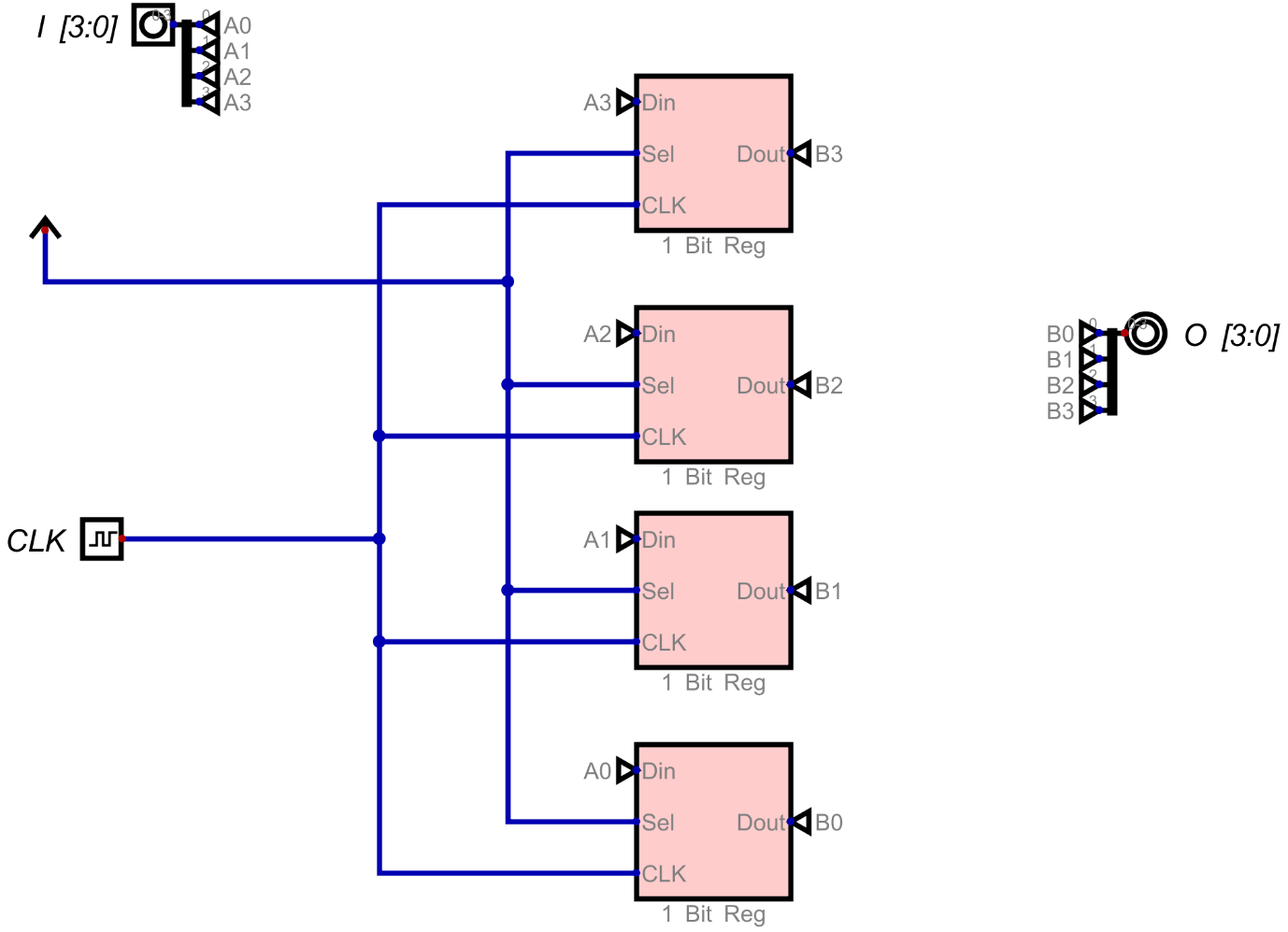
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Figure : Program Counter Register

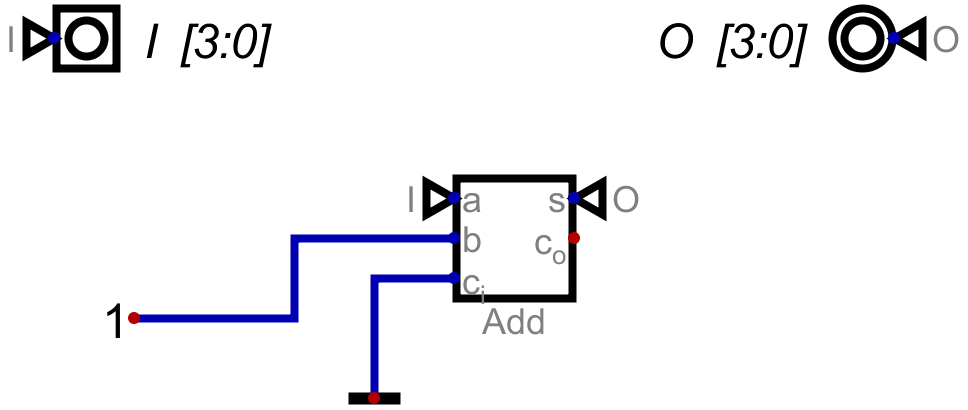


Figure : 4 Bit program counter Adder

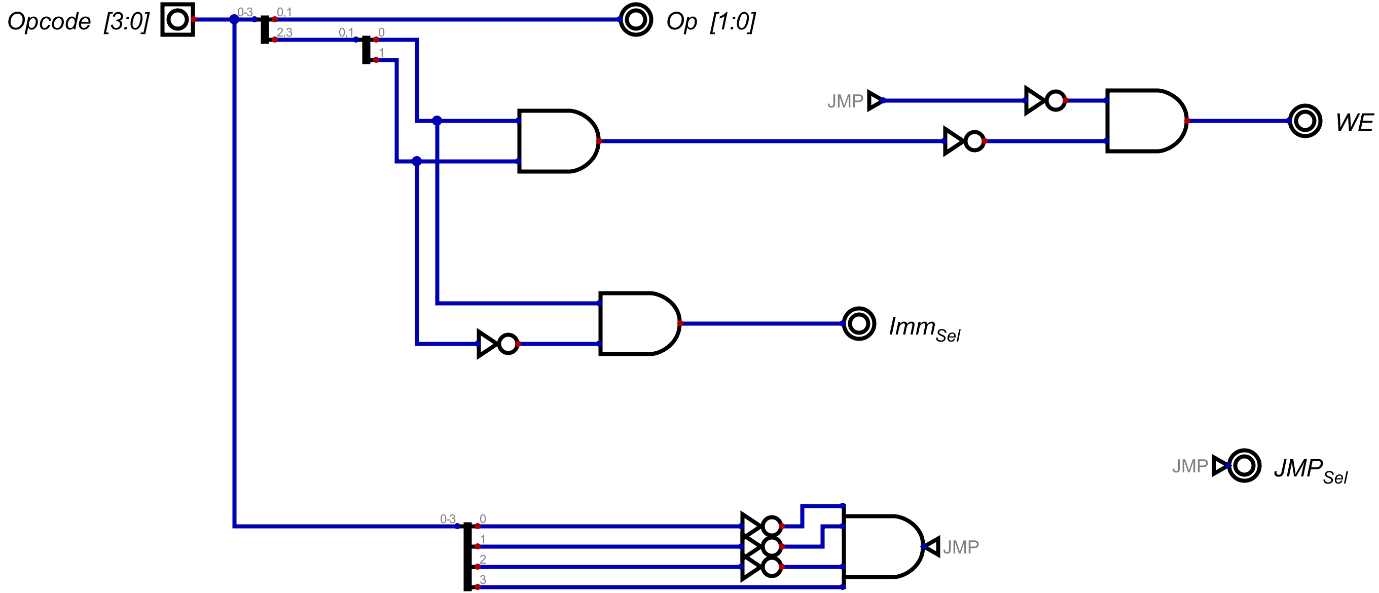


Figure : Control Logic

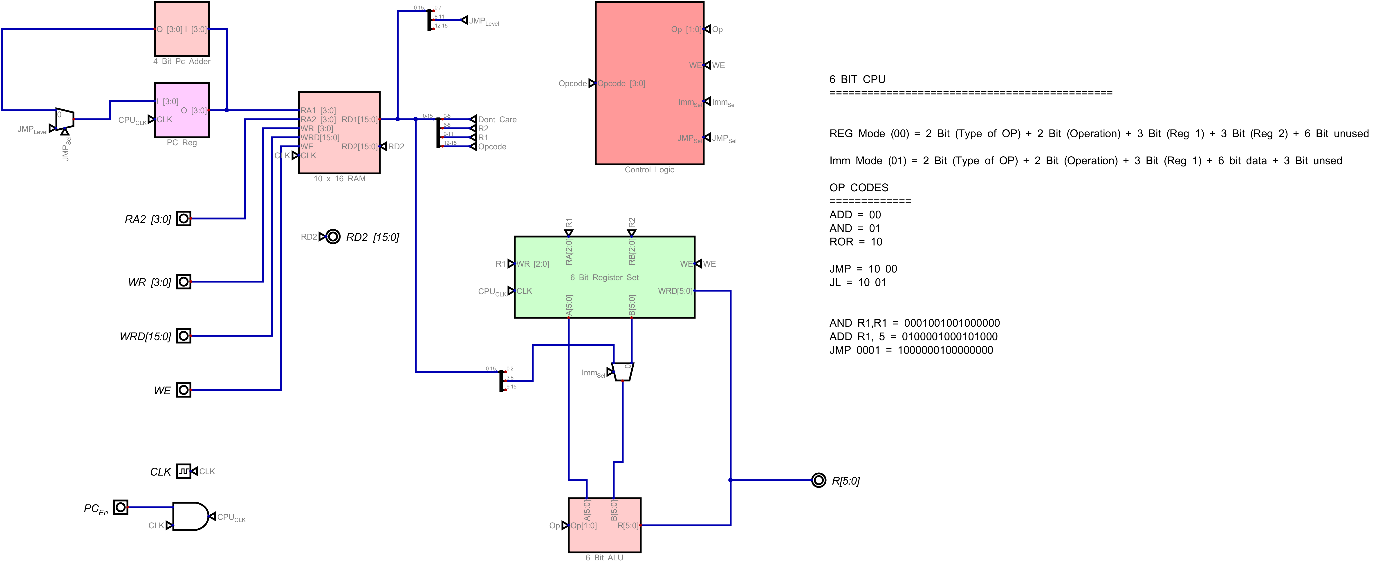


Figure : 6 Bit CPU

**Verilog Code:**

1. **ALU Circuit (Top to Bottom all circuits):**

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1. **Register Set Circuit (Top to Bottom all circuits):**

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1. **RAM Circuit (Top to Bottom all circuits):**

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1. **CPU (Top to Bottom all circuits):**

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