30 Days of RTL Coding

-By T Tushar Shenoy

Day 19

Problem Statement: Implementing Comparator in Gate level of Implementation.

Theory:

1-Bit Magnitude Comparator

Truth Table

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

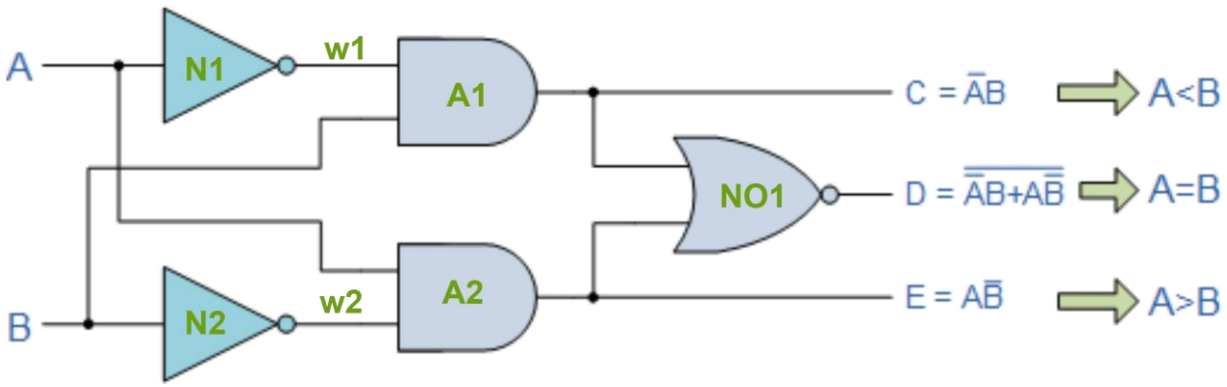


FIG: 1-Bit Magnitude Comparator

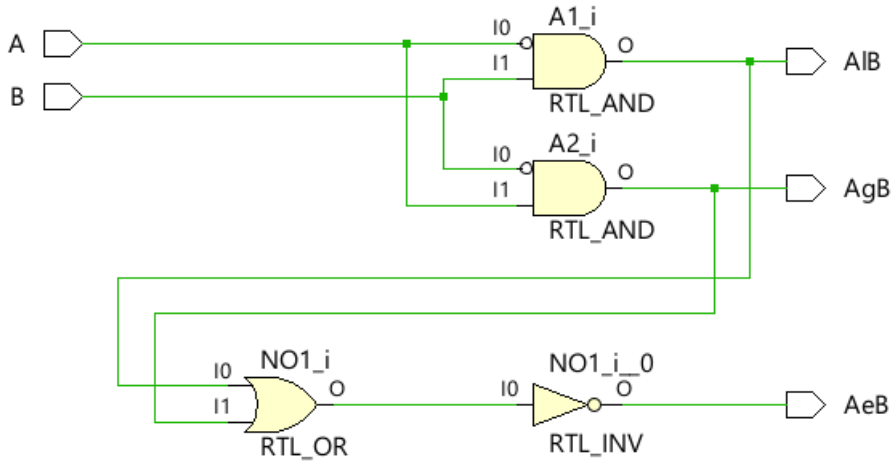
Verilog Code:

```
//Verilog Code for 1 Bit Comparator
module comparator1bit(A,B,AeB,AgB,AlB);

input A,B;
output AeB,AgB,AlB;

wire w1,w2;

not N1(w1,A);
not N2(w2,B);

and A1(AlB,w1,B);
and A2(AgB,w2,A);

nor NO1(AeB,AlB,AgB);

endmodule
```

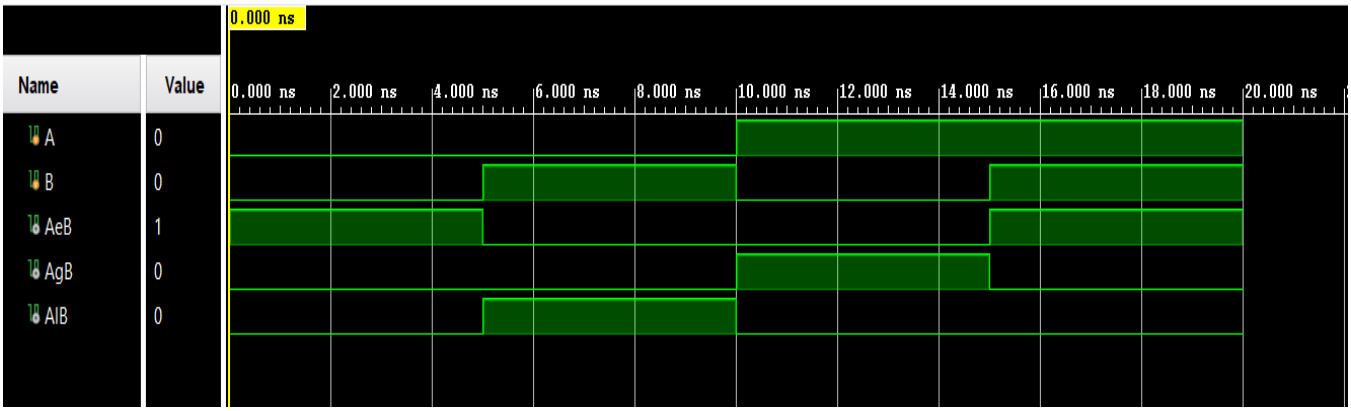
Testbench Code:

```
//Testbench code for 1 Bit Comparator
module comparator1bit_tb();

reg A,B;
wire AeB,AgB,AlB;

comparator1bit dut(.A(A),.B(B),.AeB(AeB),.AgB(AgB),.AlB(AlB));

initial begin
   A=1'b0;B=1'b0;
#5 A=1'b0;B=1'b1;
#5 A=1'b1;B=1'b0;
#5 A=1'b1;B=1'b1;
#5 $finish;
end

endmodule
```

Schematic:



Simulation Output:



2-Bit Magnitude Comparator

Truth Table

Inputs				Outputs		
A		B				
$a1$	$a0$	$b1$	$b0$	$A = B$	$A > B$	$A < B$
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

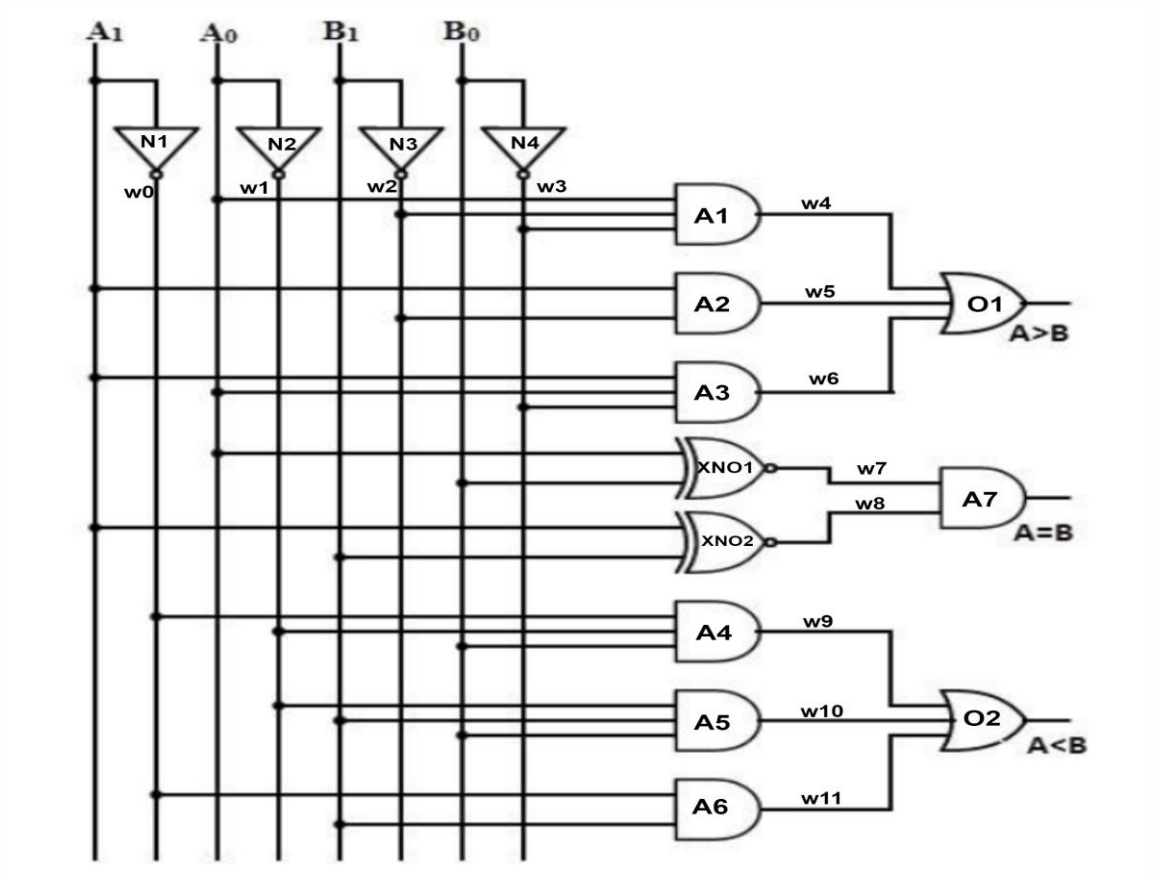


FIG: 2-Bit Magnitude Comparator

Verilog Code:

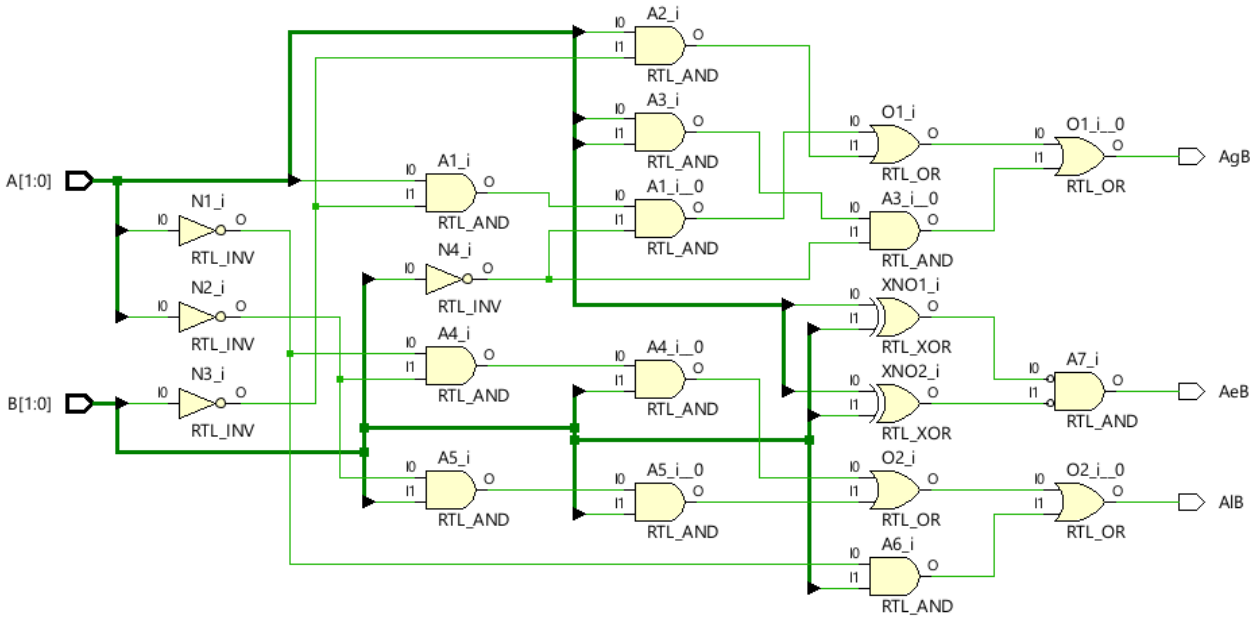
```
//Verilog Code for 2 Bit Comparator
module comparator2bit(A,B,AeB,AgB,AlB);

input [1:0]A,B;
output  AeB,AgB,AlB;

wire [11:0]w;
not N1(w[0],A[1]);
not N2(w[1],A[0]);
not N3(w[2],B[1]);
not N4(w[3],B[0]);

and A1(w[4],A[0],w[2],w[3]);
and A2(w[5],A[1],w[2]);
and A3(w[6],A[1],A[0],w[3]);

or O1(AgB,w[4],w[5],w[6]);

xnor XNO1(w[7],A[0],B[0]);
xnor XNO2(w[8],A[1],B[1]);

and A7(AeB,w[7],w[8]);

and A4(w[9],w[0],w[1],B[0]);
and A5(w[10],w[1],B[1],B[0]);
and A6(w[11],w[0],B[1]);
```

```
or O2(AlB,w[9],w[10],w[11]);

endmodule
```

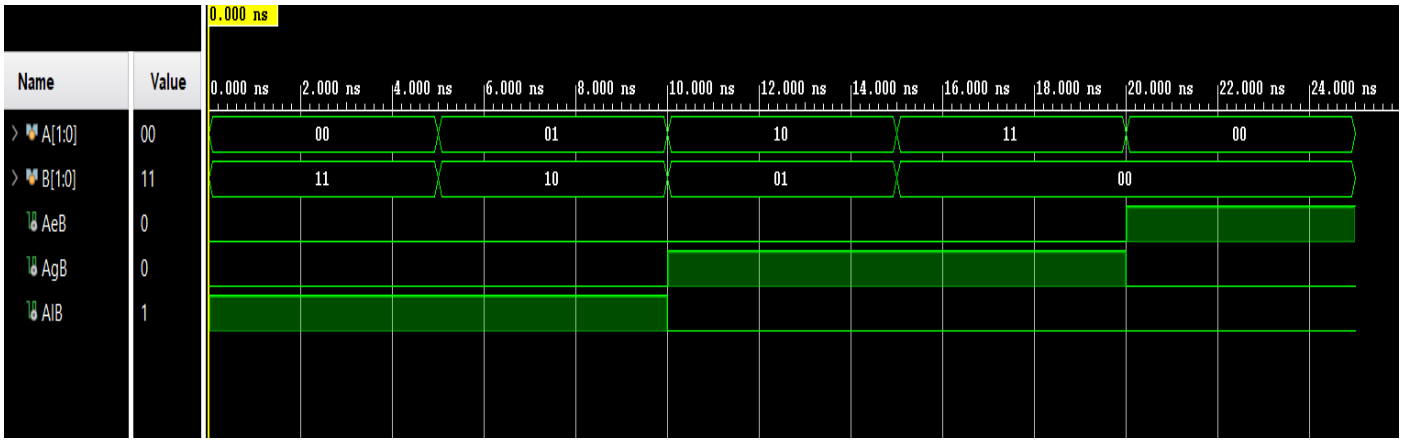
Testbench Code:

```
//Testbench code for 2 Bit Comparator
module comparator2bit_tb();

reg [1:0]A,B;
wire AeB,AgB,AlB;

comparator2bit dut(.A(A),.B(B),.AeB(AeB),.AgB(AgB),.AlB(AlB));

initial begin
   A=2'b00;B=2'b11;
#5 A=2'b01;B=2'b10;
#5 A=2'b10;B=2'b01;
#5 A=2'b11;B=2'b00;
#5 A=2'b00;B=2'b00;
//Add More Test Cases Here
#5 $finish;
end

endmodule
```

Schematic:



Simulation Output:



GitHub Repository URL: https://github.com/tusharshenoy/RTL-Day-19-Comparator-Stuctural