30 Days of RTL Coding

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Day 11

Problem Statement: Implementing 3-Bit Ring Counter and 3-Bit Gray Counter using Structural Style.

Theory:

Ring counter is a typical application of the Shift register. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift register it is taken as output. Except for this, all the other things are the same.

No. of states in Ring counter = No. of flip-flop used

Gray code is a binary numeral system where two successive values differ in only one bit position. This makes it useful in applications like digital encoders, rotary encoders, and minimizing glitches when transitioning between numbers. A ***Gray code counter*** using D flip-flops can be implemented to generate a sequence of gray code numbers. The standard Gray Code sequence for a 3-bit counter is: 000, 001, 011, 010, 110, 111,101, 100, and then repeat. Gray code, also known as reflected binary code or unit distance code, is a binary numeral system where two successive values differ in only one bit position. It is named after Frank Gray, who patented the binary code sequence in 1953, although it was independently discovered and used earlier. In traditional binary counting, when we increment from one number to the next, multiple bits can change simultaneously, leading to potential glitches or errors in some applications unlike the Gray Code.

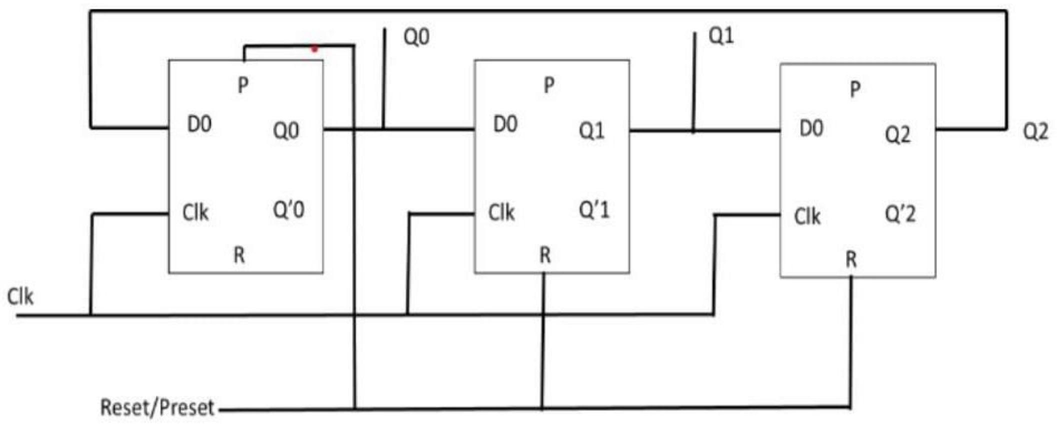


FIG: Ring Counter Block Diagram

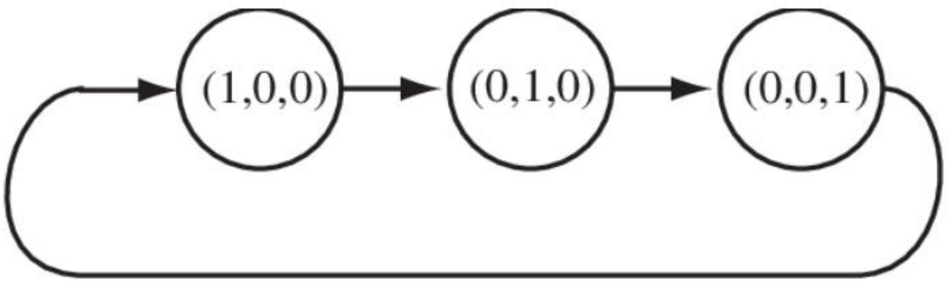


FIG: Ring Counter State Diagram

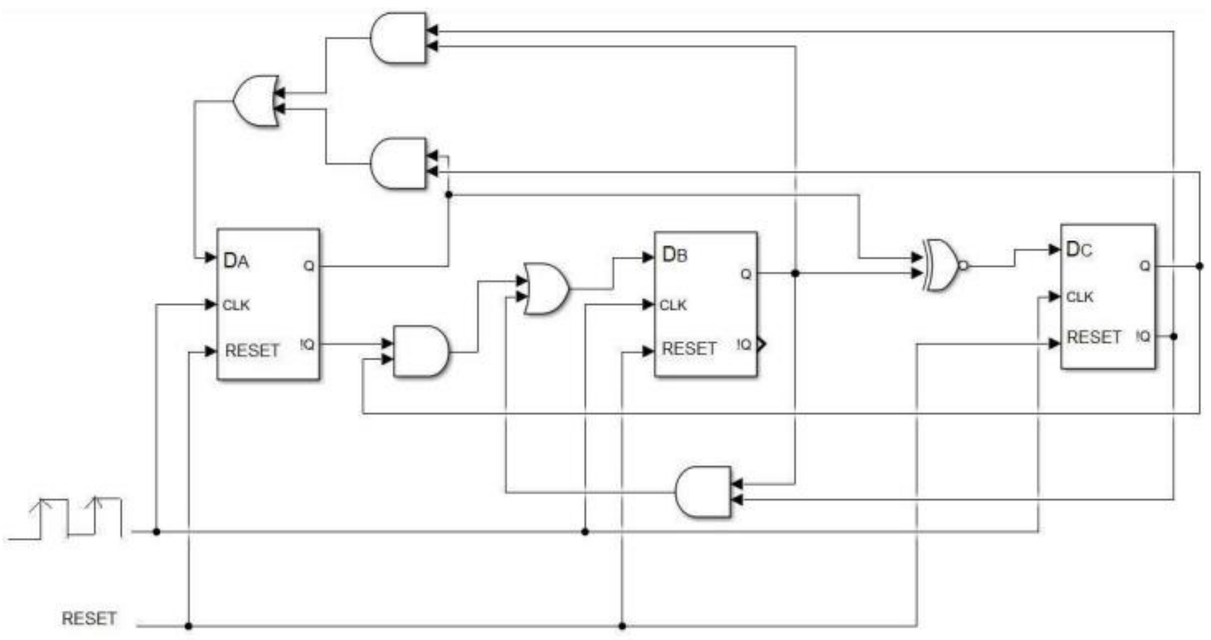


FIG: Gray Counter Block Diagram

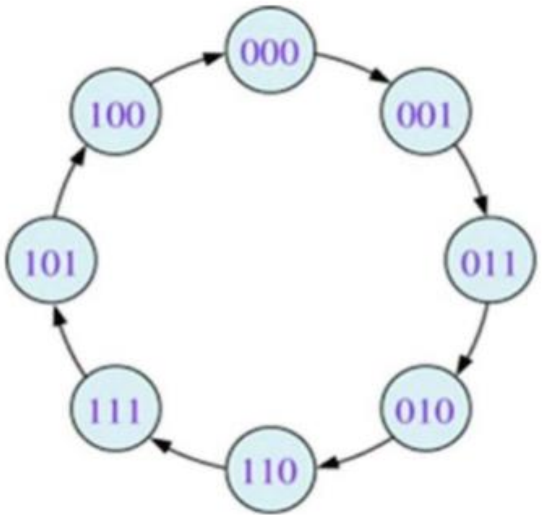


FIG: Gray Counter State Diagram

- **Truth Table of D Flip Flop**

Clock	D	Q+	$\bar{Q}$+
0	X	Q	$\bar{Q}$
⬆	0	0	1
⬆	1	1	0

Ring Counter Truth Table

Reset	Clock	Q0	Q1	Q2
1	X	0	0	0
0	↑	1	0	0
0	↑	0	1	0
0	↑	0	0	1
0	↑	1	0	0
0	↑	0	1	0
0	↑	0	0	1

Gray Counter Truth Table

Reset	Clock	Q2	Q1	Q0
1	X	0	0	0
0	↑	0	0	1
0	↑	0	1	1
0	↑	0	1	0
0	↑	1	1	0
0	↑	1	1	1
0	↑	1	0	1
0	↑	1	0	0
0	↑	0	0	0

- **RING COUNTER**

Verilog Code:

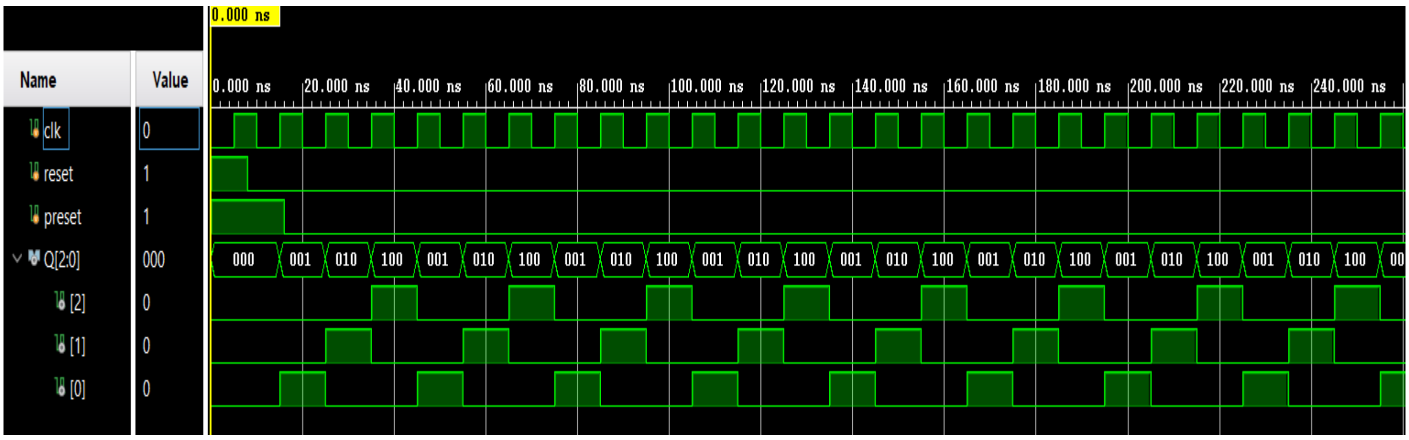
```
//Verilog Code for D Flip Flop
module D_Flip_Flop(D, reset, clk, Q, Qb);
 input D, reset, clk;
 output Q, Qb;
 reg Q, Qb;
 always @(posedge clk,posedge reset)
 begin
 if (reset)
 Q = 0;
 else
 Q <= D;
 Qb <= ~Q;
 end
endmodule
```

```
//Verilog Code for Ring Counter
module RingCounter3Bit(clk, reset,preset, Q);

input clk,reset,preset;
output [2:0]Q;

D_Flip_Flop DFF_0(.D(Q[2]+preset), .reset(reset), .clk(clk), .Q(Q[0]));
D_Flip_Flop DFF_1(.D(Q[0]), .reset(reset), .clk(clk), .Q(Q[1]));
D_Flip_Flop DFF_2(.D(Q[1]), .reset(reset), .clk(clk), .Q(Q[2]));

endmodule
```

Testbench Code:

```
module Johnson_Counter_4bit_tb;
reg clk,reset;
wire [3:0]Q;

Johnson_Counter_4bit dut(clk, reset, Q);

initial begin
 clk=1'b0;
 reset=1;
 #8 reset=0;
end
always #5 clk=~clk;
endmodule
```

Simulation Output:



- **GRAY COUNTER**

Verilog Code:

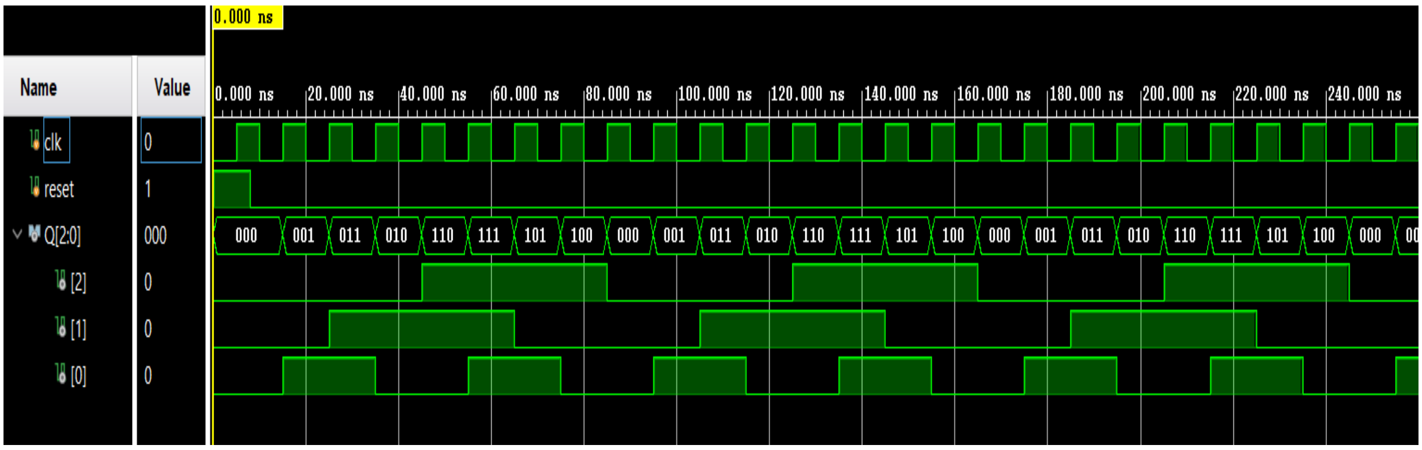
```
//Verilog Code for D Flip Flop
module D_Flip_Flop(D, reset, clk, Q, Qb);
 input D, reset, clk;
 output Q, Qb;
 reg Q, Qb;
 always @(posedge clk,posedge reset)
 begin
 if (reset)
 Q = 0;
 else
 Q <= D;
 Qb <= ~Q;
 end
endmodule
```

```
//Verilog Code for Gray Counter
module Gray_Code_Counter(clk,reset,Q);

input clk,reset;
output [2:0]Q;
wire [2:0]Qb;
wire [3:0]w;
wire d2,d1,d0;

and a0(w[0],Q[2],Q[0]);
and a1(w[1],Q[1],Qb[0]);
or o0(d2,w[0],w[1]);

and a2(w[2],Qb[2],Q[0]);
and a3(w[3],Qb[0],Q[1]);
or o1(d1,w[2],w[3]);

xnor x0(d0,Q[2],Q[1]);

D_Flip_Flop dff2(.D(d2),.clk(clk),.reset(reset),.Q(Q[2]),.Qb(Qb[2]));

D_Flip_Flop dff1(.D(d1),.clk(clk),.reset(reset),.Q(Q[1]),.Qb(Qb[1]));

D_Flip_Flop dff0(.D(d0),.clk(clk),.reset(reset),.Q(Q[0]),.Qb(Qb[0]));

endmodule
```

Testbench Code:

```
module Gray_Code_Counter_tb;

reg clk, reset;
wire [2:0] Q;

Gray_Code_Counter dut(.clk(clk), .reset(reset), .Q(Q));

initial begin
  clk = 1'b0;
  reset = 1'b1;
  #8 reset = 1'b0;
end

always #5 clk = ~clk;

endmodule
```

Simulation Output:



GitHub Repository URL: https://github.com/tusharshenoy/RTL-Day-11-Ring-and-Gray-Counter