30 Days of RTL Coding

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Day 6

Problem Statement: Implementing a 4-Bit Parallel Adder / Subtractor using Structural Style of Implementation.

Theory:

In Digital Circuits, A Binary Adder-Subtractor is capable of both the addition and subtraction of binary numbers in one circuit itself. The operation is performed depending on the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit).

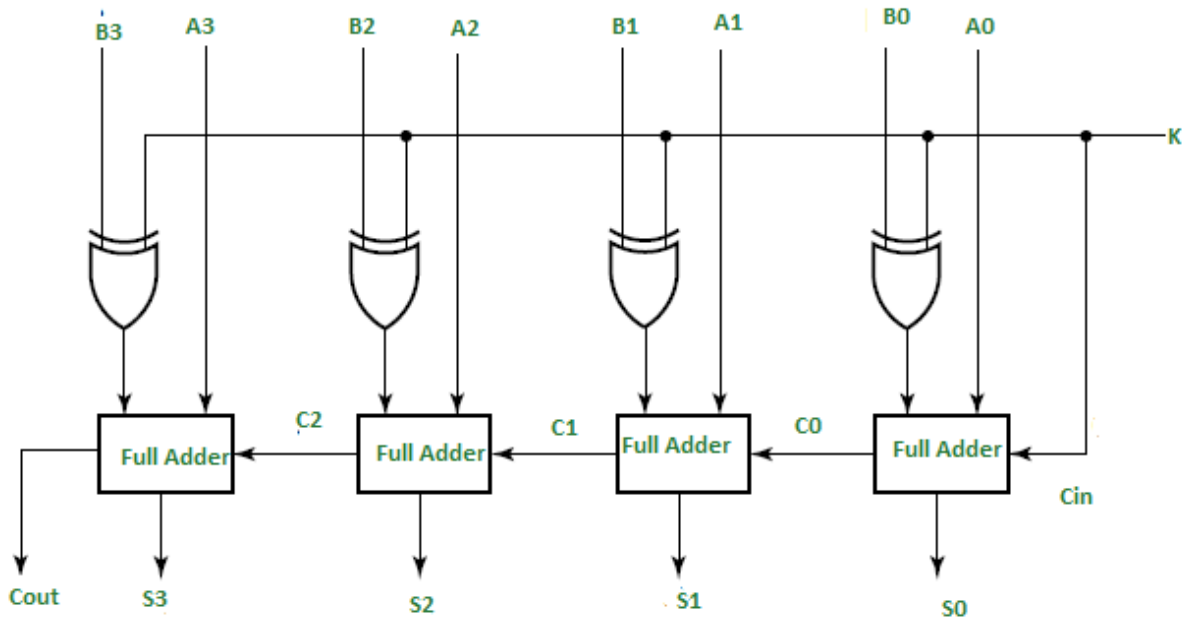


FIG: 4-Bit Parallel Adder / Subtractor

As shown in the figure, the first full adder has a control line directly as its input (input carry Cin), the input A0 (The least significant bit of A) is directly input in the full adder. The third input is the exor of B0 and K. The two outputs produced are Sum/Difference (S0) and Carry (C0).

If the value of K (Control line) is 1, the output of B0 (exor) K=B0′ (Complement B0). Thus the operation would be A+ (B0′). Now 2's complement subtraction for two numbers A and B is given by A+B'+Cin. This suggests that when K=1, the operation being performed on the four-bit numbers is subtraction.

Similarly If the Value of K=0, B0 (exor) K=B0. The operation is A+B which is simple binary addition. This suggests that When K=0, the operation is performed on the four-bit numbers in addition.

Then C0 is serially passed to the second full adder as one of its outputs. The sum/difference S0 is recorded as the least significant bit of the sum/difference. A1, A2, A3 are direct inputs to the second, third and fourth full adders. Then the third input is the B1, B2, B3 EXORed with K to the second, third and fourth full adder respectively. The carry C1, C2 are serially passed to the successive full adder as one of the inputs. C3 becomes the total carry to the sum/difference. S1, S2, S3 are recorded to form the result with S0.

Drawback of Parallel Adder or Subtractor

As the architecture of parallel adder or subtractor is very similar to that of a parallel adder (and also to that of a parallel subtractor), even this design is prone to the effect of ripple propagation delay. Nevertheless, these kind of circuits find their application in the field of computers as a part of arithmetic and logic (ALU) unit, aiding numerous computations.

Verilog Code:

```
//Verilog Code for 1 Bit Full-adder
module full_adder_1bit(a,b,cin,sum,carry);
input a,b,cin;
output sum,carry;

assign sum=a^b^cin;
assign carry=(a&b)|(b&cin)|(a&cin);

endmodule


//Verilog Code for Parallel Adder/Subtractor
module parallel_adder_subtractor(A,B,K,S,Cout,Cin);
input [3:0]A,B;
input K,Cin;
output [3:0]S;
output Cout;

wire b0,b1,b2,b3;
xor(b0,B[0],K);
xor(b1,B[1],K);
xor(b2,B[2],K);
xor(b3,B[3],K);
```

```
wire c0,c1,c2;
full_adder_1bit  F0(A[0],b0,Cin,S[0],c0);
full_adder_1bit  F1(A[1],b1,c0,S[1],c1);
full_adder_1bit  F2(A[2],b2,c1,S[2],c2);
full_adder_1bit  F3(A[3],b3,c2,S[3],Cout);

endmodule
```

Testbench Code:

```
//Verilog Testbench Code for Parallel Adder/Subtractor
module parallel_adder_subtractor_tb();

reg [3:0]A,B;
reg K,Cin;
wire [3:0]S;
wire Cout;

parallel_adder_subtractor dut(A,B,K,S,Cout,Cin);

initial begin
K=1'b0; //adder
     A=4'b0000;B=4'b0000;Cin=K;
#5 A=4'b0001;B=4'b0001;
#5 A=4'b0010;B=4'b0010;
#5 A=4'b0011;B=4'b0011;
#5 A=4'b0100;B=4'b0100;
#5 A=4'b0101;B=4'b0101;
#5 A=4'b0110;B=4'b0110;
#5 A=4'b0111;B=4'b0111;
#5 A=4'b1000;B=4'b1000;
#5 A=4'b1001;B=4'b1001;
#5 A=4'b1010;B=4'b1010;
#5 A=4'b1011;B=4'b1011;
#5 A=4'b1100;B=4'b1100;
```

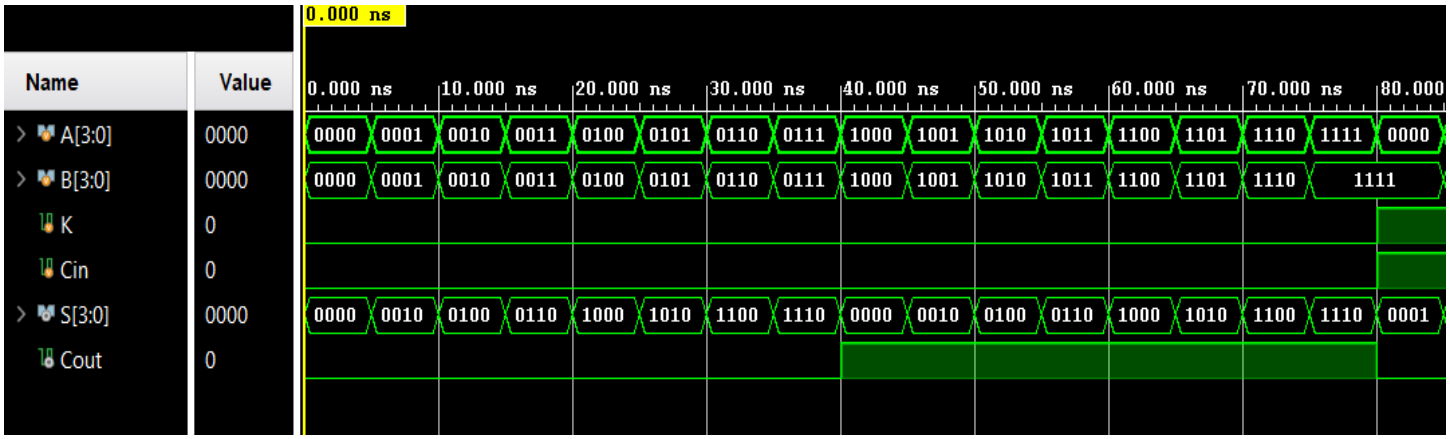
```
#5 A=4'b1101;B=4'b1101;
#5 A=4'b1110;B=4'b1110;
#5 A=4'b1111;B=4'b1111;

#5 K=1'b1; //subtractor
   A=4'b0000;B=4'b1111;Cin=K;
#5 A=4'b0001;B=4'b1110;
#5 A=4'b0010;B=4'b1101;
#5 A=4'b0011;B=4'b1100;
#5 A=4'b0100;B=4'b1011;
#5 A=4'b0101;B=4'b1010;
#5 A=4'b0110;B=4'b1001;
#5 A=4'b0111;B=4'b1000;
#5 A=4'b1000;B=4'b0111;
#5 A=4'b1001;B=4'b0110;
#5 A=4'b1010;B=4'b0101;
#5 A=4'b1011;B=4'b0100;
#5 A=4'b1100;B=4'b0011;
#5 A=4'b1101;B=4'b0010;
#5 A=4'b1110;B=4'b0001;
#5 A=4'b1111;B=4'b0000;
#5 $finish;
end

endmodule
```

Simulation Output:

- **Parallel Adder, K=0**



- **Parallel Subtractor, K=1**

Schematics:

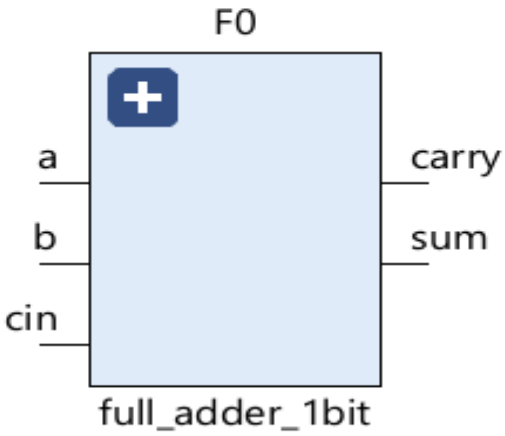


FIG: Block Diagram of full_adder_1bit

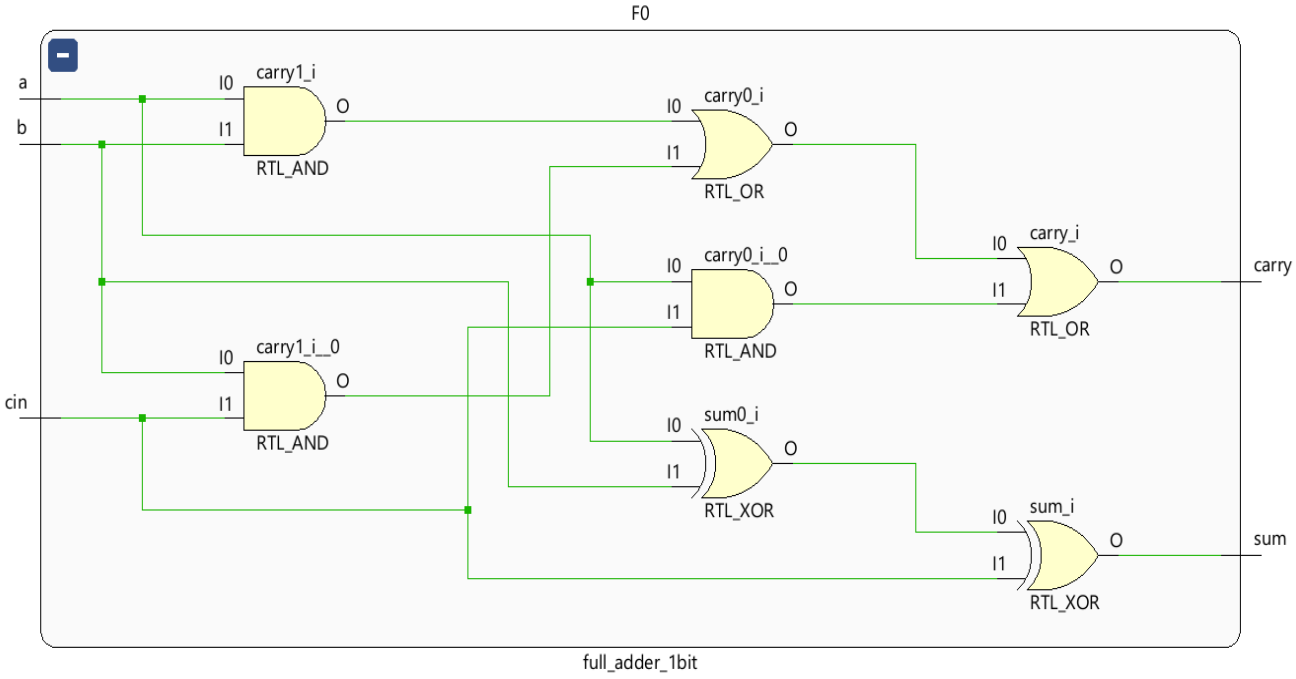


FIG: Schematic of full_adder_1bit

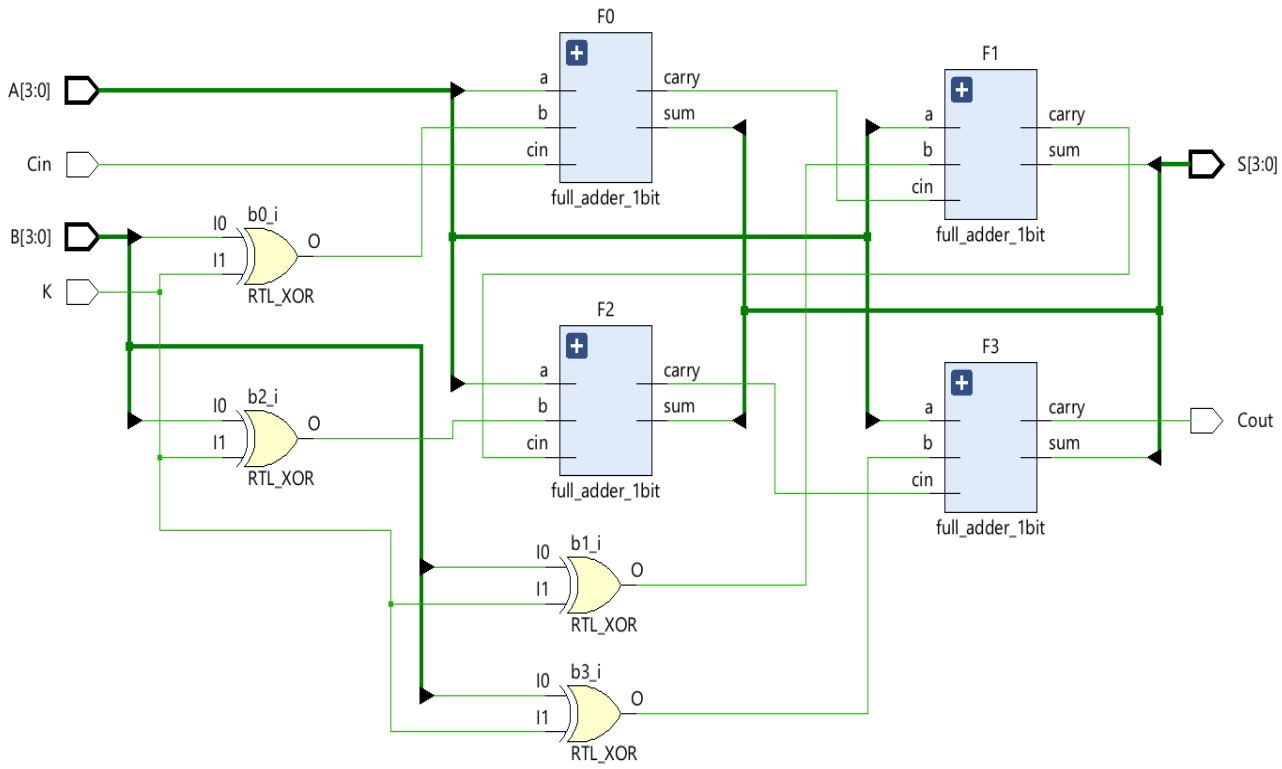


FIG: Schematic of Parallel Adder/Subtractor

GitHub Repository URL: - https://github.com/tusharshenoy/RTL-Day-6-Parallel-Adder-Subtractor