Shruti R. Kulkarni **10307022**
Electrical Engineering **M.Tech.**
Indian Institute of Technology, Bombay **Female**
Specialization: Electronic Systems **DOB: 18-10-1988**

Examination	University	Institute	Year	CPI / %
Post Graduation	IIT Bombay	IIT Bombay	2012	9.49
Undergraduate Specialization: Electronics and Communication				
Graduation	Visvesvaraya Technological University, Belgaum	RNS Institute of Technology, Bangalore	2010	78.28
Intermediate/+2	CBSE	K. V. Picket, Secunderabad	2006	92.40
Matriculation	CBSE	K. V. Picket, Secunderabad	2004	93.20

AREAS OF INTEREST:

Digital and Analog VLSI design, Embedded Systems Design.

RELEVANT COURSES:

VLSI Design, VLSI Systems Design, VLSI Design Lab (VHDL and Verilog), CMOS Analog VLSI Design, Embedded Systems Design, Electronic Systems Design, Digital Signal Processing and its Applications.

TECHNICAL SKILLS:

- **Tools:** Cadence-Virtuoso, Cadence-SoC Encounter, Synopsys Design Compiler, NG-SPICE, MATLAB, GHDL, Xilinx-ISE, Modelsim, AVR-Studios, Keil, Magic, PI Calculator, CAPEM.
- **Languages:** Hardware Descriptive Language (VHDL, Verilog, VerilogA), C, C++, Assembly Languages (8051, 8085, 8086).

PROJECTS / SEMINARS:

M.Tech Project: **[From Jan. 2011]**

Design of neuromorphic circuit on CMOS and memristor platforms **Guide: Prof. Maryam S. Baghini**

The project involves designing a circuit that mimics the processing taking place in the retina, based on spike time-dependent latency, for pattern classification applications. The circuit is designed in CMOS technology as well as in an emerging technology as a memristor-based neural architecture. The two designs will be compared in terms of power consumption, speed and area.

Completed work: Wrote and verified one spike-time latency algorithm in MATLAB on standard images. Designed the same on CMOS 180nm platform using automatic digital design flow. RTL was converted to GDSII using Synopsys Design Compiler and Cadence SoC Encounter. Functionality was verified on sample test vectors using ModelSim.

Ongoing Work: To analyze the design and results of automatically-generated design in CMOS technology, to write more algorithms like spike count, to run more examples, develop a VerilogA model of Memristor and develop model of a neural architecture using memristor and compare the two designs across several examples. To explore other possible biological processing algorithms useful in pattern classification tasks.

M.Tech Course Projects:

Design of sequence merger and queue *(Prof. M.P. Desai)* **[April 2011]**

A sequence merger and a FIFO Queue were designed in VHDL, based on Ready-Ready protocol. Each design was broken into data-path (implemented structurally) and control-path (implemented using state machine, behaviorally), and was verified in Modelsim.

Design of N-bit Barrel Shifter, Run Length Encoder, Bus Interface unit of 8085, Floating-point adder *(Prof. D. K. Sharma)* **[Jan.-April 2011]**

Designed in VHDL /Verilog as per specifications using GHDL/Modelsim; and synthesized using Xilinx-ISE.

Design of a four quad log-antilog multiplier *(Prof. P. C. Pandey)* **[Nov. 2010]**

A four quadrant multiplier was implemented by designing log and anti-log amplifiers using operational amplifier (uA741) and BJT (npn) transistor array.

Design of a microcontroller based digital voice recorder ***(Prof. P. C. Pandey)*** **[April 2011]**
Design was implemented using AVR Atmega32. The audio files were stored in the 128MB Transcend SD card. The microcontroller was interfaced to the SD card through serial peripheral interface. The SD card was formatted with FAT32 file system, which allowed the user to selectively record and playback the audio files from the SD card.

Speech vs. silence discrimination ***(Prof. V. M. Gadre)*** **[Oct. 2010]**
Implemented (in MATLAB) using average magnitude, zero crossing rate and Mahalanobis distance function as a linear pattern classifier. The algorithm was tested on standard speech samples, and was able to classify speech signal as voiced, unvoiced or as background noise.

Synthesis of vowel sound using LPC and cepstral coefficients ***(Prof. Preeti Rao)*** **[Nov. 2010]**
For a given segment of speech sound, 10^{th} order LP and cepstral coefficients were computed (in MATLAB), which were used to determine the pitch and vocal tract magnitude response for synthesizing the vowel sound in each case. The transmission bit rate achieved using the speech model was small (2.4kbps) compared to the instantaneous quantization (64kbps).

B.E. Project: **[Feb – March 2010]**
Design of an Integrated Control Unit (ICU) for DVBS receiver ***(Bharat Electronics Ltd., Bangalore)***

- The project involved designing of a user interface board for a Digital Video Broadcast Satellite (DVBS) receiver, which allows the user to configure the receiver based on input frequency, and it also displays the status of the signal and the channel. The ICU was implemented using microcontroller 8051.
- A DVB-S receiver Interface Simulation Application was developed using Visual Basics for testing purposes. This replies to the commands sent by the Integrated Control unit.

Technical Seminars:

- Review of Biomorphic circuits in CMOS and emerging Technologies (M.Tech Seminar, Nov 2010).
- Study on Code Division Duplexing (B.E. seminar, April 2010).

POSITIONS OF RESPONSIBILITY:

Teaching Associate, IIT Bombay for the following courses:

- Electronic Systems Design Lab (Aug'11 to Nov'11) under Prof. P.C. Pandey.
- Analog Electronics Lab (Jan'11 to April'11) under Prof. Anil K. G.
- Electronic Devices Lab (Aug'10 to Nov'10) under Prof. A. K. Tulapurkar.

ACHIEVEMENTS:

- GATE 2010 score in ECE - 848/1000 (All India Rank 114 out of 1,04,291 candidates)
- Awarded for securing 5^{th} rank in college during 1^{st} year, B.E. out of 360 students.
- Secured first rank in school; class XII CBSE board examination.
- Won 1^{st} place in Bhagavad-Gita chanting competition organized by Chinmaya Mission at Jamnagar district level in 2001; participated in the Gujarat state level competition.

EXTRACURRICULAR ACTIVITIES :

- Won 1^{st} place in Cricket and 2^{nd} place in Basketball, in RNSIT Hostel Fest, Utopia 2007.
- Secured 2^{nd} position in inter-house volley ball competition, in school (2005).
- Participated in Lead India 2020 Movement at Hyderabad (2004).
- Won 1^{st} place in Sanskrit recitation and group song competition in school (2003).

OTHER ACTIVITIES:

- **Hobbies:** Photography, Sketching, Singing.
- **Sports:** Table-tennis, Carrom, Badminton.