Sanket Diwale | **08D07038**
Electrical Engineering | **Dual Degree (B.Tech+M.Tech.)**
Indian Institute of Technology, Bombay | **Male**
Specialization: Microelectronics | **DOB: 29 Nov 1990**

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2012	8.48
Intermediate/+2	HSC	N Wadia College, Pune	2008	77.00
Matriculation	ICSE	CDS School, Nagpur	2006	89.50

Completed a Minor in Aerospace Engineering with corresponding CPI of 8.81/10

Scholastic Achievements and Awards

- **First Position** at **Mahindra Satyam's Mechatronics Young Engineer Awards 2011** among 100 plus nominations across UG, PG and research streams from over 70 institutes including various IITs, IISc and NITs
- **First runner up** at **UMP International Competition for Underwater Gliders**, **Spain 2011**
- **Institute Technical Color,** for excellence in overall contribution to technical activities in the year 2011-2012
- **Institute Technical Special Mention,** for excellent technical contributions in the year 2009-2010
- Secured **All India Rank-252** in IIT-JEE 2008, with over 300,000 aspirants appearing for the exam
- Secured **State rank-81** in AIEEE-2008 among 800,000 aspirants
- Secured a position in **Top 1%** in State in **National Physics Olympiad 2007**

Master's Dissertation

High Level Synthesis and Application mapping to Many-core, NoC architectures May. 2012 – Present
Guide: Prof. Sachin Patkar High Performance Computing Lab, IIT Bombay

- Working on increasing computational performance in both energy efficiency and throughput by exploiting application's thread level parallelism and optimized inter-processor communication
- Prototyped a 14 node Projective Geometry NoC on Altera DE2-70 FPGA boards to enhance communication throughput (with a 2-hop all to all connection) compared to widely used multi-hop mesh architectures
- Implemented all the sub modules for the NoC, namely the processing and routing nodes with fast arbiter and routing logic, bypass FIFOs and modified-MIPs processors as the processing elements in Verilog
- Mapped bipartite graph applications like N-point FFT, Matrix vector product, LDPC decoding to this prototype (obtaining close to 7-fold increase in throughput)
- Built a GUI (in C++) to allow easy input and visualization of Data Flow Graphs and **automated** the **scheduling** and folding/**placement** of tasks to a minimal set of cores (minimizing power without loss of throughput)
- Reviewed literature for existing many core architectures with GALS and DVFS clocking schemes and automation tools for application mapping to such platforms

Professional Experience

Shwas – **India's First Underwater Glider** Dec. 2009 – Present
Guide: Prof. K. Sudhakar, Prof. Hemandra Arya Micro Aerial Vehicles Lab, IIT Bombay

- **Initiated the project**, **formed and led a team** of 3 students **over a span of 2 years**
- Procured **funding of 1.5 Lacs** from **Boeing Student Design Projects** and **Technovation**, IRCC, IIT Bombay
- **Modeled** the **vehicle dynamics** in MATLAB, **designed a controller** and **integrated** with FlightGear (open source flight simulator) for easy visualization of simulations in 3D environments
- Designed the **embedded system** and **firmware** for attitude estimation, control & Ground station communication
- Parameterized the **performance** (published at ADE's biannual conference SAROD); **optimized** the design constrained in speed, range, endurance and payload requirements for optimal transport economy and weight
- Designed the structure in CAD, fabricated and tested **two prototype Gliders** in a first pass process
- Captured the attention of eminent technology leaders at various conferences and competitions; **Invited** by Dr. Chakraborti, Associate Director, NSTL, DRDO to NTSL, Vishakhapatnam for a talk on design & future prospects
- **First runner up** at **UMP International Competition for Underwater Gliders**, **Madrid** amongst 17 teams spanning 5 different countries

Project Starfish – National University of Singapore May - July 2010
Guide: Dr. Mandar Chitre ***Summer Internship*** Acoustics Research Lab, NUS

- Implemented data acquisition and acoustic signal processing algorithms for the development of a real time target detection system module to be placed onboard the AUV (Starfish) with a forward looking SONAR
- Tested the system successfully in sea, lake and swimming pool environments
- Targets were successfully detected and placed on a map with error positioning of less than 1 meter

***PRATHAM*- IIT Bombay's Student Satellite** Dec. 2008 – May 2010

Nano-satellite slated for launch by ISRO with the payload to find Total Electron Count Density in the ionosphere

- Member of the satellite system engineering and mechanisms subsystem teams
- Designed an antenna deployment mechanism and separation (snap) detection switch for the satellite
- Reviewed military standards(MIL-PRF 8805) to check suitability of COTS switches for snap detection
- Made CAD models for the satellite, mechanisms and ISRO's IBL-230 launch vehicle interface

Key Academic Projects

Mixed Signal Lock In Amplifier Jan - April 2010

Guide: Prof. Dipankar Saha

- Designed and fabricated a lock in amplifier with PLL driven reference input, quadrature phase clock generation, analog mixer, high-Q DSP filter and tunable operational frequency ranges
- Extracted signals of up to 1mV amplitude in -60dB and -80dB SNR with less than 8% and 20% error respectively

Decentralized Multi Agent control in non-static connectivity networks Aug 2012 – Present

Guide: Prof. Arpita Sinha SYSCON, IITB

- Implemented consensus tracking and formation control algorithms for multi-agent systems
- Finite sensor/communication ranges accounted for with state dependent connectivity graphs
- Working on dynamic formation selection from a finite set, based on consensus optimality

VLSI Design and Testing Oct. 2011 – Apr. 2012

Process and Device char.	Simulated the complete process flow for fabrication of a 90nm gate length MOSFET & measured device characteristics with simulations in Sentaurus TCAD
Circuit level characteristics	Implemented a FSM for IEEE448, 3-way handshaking at MOSFET level design in Ngspice and characterized the timing requirements and delays
VLSI layout design	Designed the layout for a 3-8 decoder in 180nm tech. with specified electrical effort and verified its functioning and characterized worst case delay by extracting the netlist to spice simulations
VLSI testing	Implemented Automatic Test Generation using the D algorithm for single stuck at fault model
System design	Implemented the instruction processor of a 8085 processor in VHDL Implemented the ALU for the 8085 microprocessor in Verilog Implemented a RS232 receiver in VHDL and tested on DE0-Nano FPGA board

Technical Skills

- Tools: SPICE, MAGIC, XilinxISE, Quartus, Sentaurus TCAD, SolidWorks, OpenGl, OGRE3D, EAGLE
- Languages: C, C++, MATLAB, python, HDL languages like VHDL, Verilog, Bluespec
- Expertize with DSP, non-linear control, embedded electronics, sensors, actuators, system modeling, simulation

Extracurricular Activities and Positions Held

Robotics:	Designed and built an image processing–character recognition robot that solves anagrams and rearranges cards using a magnetic arm mechanism. Finished the project in the 1st Summer as a part of a 5 member team which received acclaim in institute quarterly magazine "Raintree"
Aeromodelling:	Prominent member of the institute Aeromodelling club Designed and built an RC aircraft, securing 4th place at Zephyr'09, annual fest of Aerospace dept. Designed and built an ornithopter (flapping wing aircraft) in Techfest 09
Sports:	NSO swimming, part of the hostel Swimming and water polo team. Completed 7.5 km in 5.5 hrs in Swimmathon 09

Events coordinator (Techfest, 2010): Coordinator for National Open Hardware challenge and Golden Challenges

Electronics club coordinator: Conducted Electronics club sessions for freshmen and newbies in electronics

Teaching Assistant: Network Theory course (EE dept. Autumn Sem. 2012)

Conducted hostel level workshops for MATLAB for students (in the year 2011)

Technical Publications

1. **Sanket Diwale** and Intesaaf Ashraf; *Performance Analysis of Small Scale Autonomous Underwater Gliders*, **5th Symposium on Applied Aerodynamics and Design of Aerospace Vehicle (SAROD)**, Bangalore, Nov 2011
2. Saptarshi Bandyopadhyay, Haripriya Mukundarajan, Sanyam Mulay, Mayank Chaturvedi, Mihir Patel, **Sanket Diwale**, et.al., *System Engineering and Integration of Pratham*, *Indian Institute of Technology Bombay's first Student Satellite*, **International Astronautical Congress**, Prague, Oct 2010 (IAC-10-B4.1.8)
3. **Sanket Diwale**, Intesaaf Ashraf and Prasanna Shevare, *SHWAS Phase II Design Report*, UPM International Competition for Underwater Glider, **Institute of Naval Architecture (ETSI), Polytechnic University of Madrid**