Megha Bose
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EDUCATIONAL DETAILS

Examination	University	Institute	Year	CPI/%
Post Graduation	IIT Bombay (MTech in Microelectronics, EE Dept.)	IIT Bombay	2012	9.76
Graduation	Visveswaraya Technological University (ECE)	M S Ramaiah Institute of Technology, Bangalore	2010	85.00
Intermediate/+2	C.B.S.E	Delhi Public School, Bokaro	2005	82.00
Matriculation	C.B.S.E	M.G.M.Senior Secondary School, Bokaro	2003	93.40

AREAS OF INTEREST

- Analog & Mixed-Signal VLSI Design, Digital VLSI design.

SCHOLASTIC ACHIEVEMENTS

- Awarded Merit Certificate for securing **3rd Position** among 150 students in Bachelor's degree.
- Secured **All India Rank 33**(99.96 percentile) in GATE 2010 among 1,04,300 students.
- Presented a Project on **'Infra Red Tracking Robot'** in Aavishkaar 2007, MSRIT Bangalore.

TECHNICAL SKILLS

- **Tools/Softwares:** Cadence-Virtuoso, Xilinx-ISE, ModelSim, MATLAB, NGSPICE, Magic, Keil, AVR Studio, Sentaurus TCAD, GHDL, Capem, PI Calculator, Mercurial.
- **Programming Languages:** VHDL, Verilog, Assembly Language(8085, 8051), C/C++, Fundamentals of Data Structures, VerilogA, HTML.

PROJECTS/SEMINARS

- **M.Tech. Project: Design of Crosstalk-Aware Current-Mode Transceiver for High-Speed Low-Power On-chip Global Interconnects.** **Software Used**:Cadence-Virtuoso.
  Guide - Prof. Dinesh K. Sharma & Prof.Maryam S. Baghini, IIT Bombay (From Aug. 2010).
  Crosstalk being a major source of noise for high-speed on-chip buses, objective of this project is to design a current-mode signaling (CMS) scheme that enables more than 3Gbps of data-rate over 10mm long wires even in the presence of crosstalk in 90nm CMOS process. Project is split in three parts.
  ◦ ***Effect of Crosstalk on Throughput/BER of Existing CMS Scheme (completed):*** Various layouts of signal line and neighbouring lines causing crosstalk (wires adjacent to the signal-line on the same metal-layer and top-bottom metal layer) have been explored to find the worst case of crosstalk and data pattern for state-of-the art CMS schemes.
  ◦ ***Wire Design (on-going):*** Objective is to find geometry of the signal-line (width and spacing between two adjacent wires) such that intrinsic bandwidth per pitch is maximized for a given signaling scheme (given driver resistance and termination resistance).
  ◦ ***Design of Crosstalk-Aware CMS Scheme (future):*** Aims to design a crosstalk-aware CMS scheme that outperforms conventional solutions of crosstalks such as shielding and differential signaling.
- **M.Tech. Seminar: A Survey of Crosstalk-Aware Signaling Schemes for On-chip High-Speed Buses.**
  Guide - Prof. Dinesh K. Sharma & Prof.Maryam S. Baghini, IIT Bombay (Aug.-Nov. 2010).
  ◦ Having understood conventional techniques to combat crosstalk such as shielding, differential signaling and data-skewing, most recent crosstalk-aware signaling schemes for high-speed buses were surveyed. A summary table comparing these recent schemes for delay-variation, throughput, peak-current and energy-consumption was prepared.
  ◦ Among the recent techniques of reducing effect of crosstalk in full-swing signaling schemes, alternate repeaters and smart-repeaters were found to be most promising. However, for reduced swing signaling schemes, so far differential signaling is considered to be the most promising solution. Hence, there is a possibility to improve performance of reduced swing signaling scheme by using novel crosstalk-aware techniques.

- **B.Tech. Project (Final Yr.): Image Compression and Encryption using RSA Algorithm.** **Guide** - Mr. Shreedarshan K., MSRIT Bangalore (Jan.-Mar. 2010). **Software Used**: MATLAB
  ◦ An 8-bit image was first compressed using *Haar transform* to one fourth times the original image & encrypted using *RSA Algorithm*.
  ◦ The encrypted image was transmitted. At the receiving end, the image was decrypted & decompressed to get back the original image.This ensured secure transmission of confidential images.

RELEVANT COURSES

◦ Digital VLSI Design ◦ CMOS Analog VLSI Design ◦ Digital Signal Processing & Applications
◦ VLSI Design Lab ◦ Mixed Signal VLSI Design ◦ Microelectronics Simulation Lab
◦ VLSI Technology ◦ Solid State devices ◦ Embedded System Design
◦ System Design

RELEVANT COURSE PROJECTS

- **Design of a High Speed Differential Op-Amp.**(Oct.2010) **[Prof.Shalabh Gupta]**
  In this project, a High Speed Differential OP-AMP with closed loop Gain = 5, Gain error = 0.5%, Phase Margin $\geq 55°$, Differential Output Voltage Swing = 1.4V & Total Power $\leq$ 10mW, using 180nm CMOS was to be designed. After design, the simulation results were to be compared with the desired values. The design was implemented using Cadence.
- **Design of High Speed 8-bit Pipeline ADC.**(Apr.2011) **[Prof.Maryam S. Baghini]**
  In this project, an 8-bit Pipeline ADC with F_{in}=2MHz, $F_{sampling}$=20MS/s & Maximum Differential V_{swing} = $2V_{p-p}$ was to be designed in Cadence & VerilogA. It comprised of a sample & hold for first stage, & a decoder & switching block, & a comparator for every stage.
- **Design of Low Pass Switched Capacitor Filter.**(Mar.2011) **[Prof.Maryam S. Baghini]**
  This project aimed at designing a high-Q biquad SC filter with $F_{sampling}$=200kHz, F_{-3dB}=20kHz, Q = 8 & unity gain at DC. Magnitude & phase characteristics were plotted for both continuous time & SC filter. The design was implemented using Cadence.
- **Design & Layout of an 8-bit Magnitude Comparator using 4-input NAND, NOR & XOR gates in dynamic logic.**(Oct.2010) **[Prof. A. N. Chandorkar]**
  An 8-bit magnitude comparator was designed in NGSPICE, using 4-input NAND, NOR & XOR gates in compound domino logic, optimized for rail-to-rail voltage swing & with a driving capacity of 4 identical gates. It was laid out in Magic.
- **Design of N-bit Barrel Shifter, 8085 Bus Interface Unit, Run Length Encoder & Floating Point Adder/Subtractor.**(Jan.-Apr.2011) **[Prof. D. K. Sharma]**
  VHDL/Verilog code were written as per specifications in Modelsim & XilinxISE.
- **Design of a Sequence Merger & FIFO Queue.**(Mar.2011) **[Prof.M. P. Desai]**
  A sequence merger accepting two input sequences and merging them was designed based on specified properties. Also a Queue to exchange data between Queue and environment was designed. The work involved writing Proto-RTL descriptions based on Ready-Ready protocol, designing data and control paths & verification using test-benches in VHDL. Modelsim & Xilinx-ISE were used for modeling and verification.

AWARDS AND ACHIEVEMENTS

- **Positions of Responsibility:**
  ◦ **Teaching Assistant** for the following courses at IITB:
  -Introduction to Electrical and Electronic Circuits, by Prof. Anil KG (July-Dec, 2010).
  -Digital Electronics Lab, by Prof. U. Ganguly (Jan-May, 2011).
  -VLSI Design, by Prof. M. P. Desai (July-Dec, 2011).
  ◦ Held the post of the **Coordinator** in IEEE MSRIT, Bangalore (2008).
- **Others:**
  ◦ Represented EE Dept in **Table Tennis & Carrom** in PG Sports 2010 & 2011, IIT Bombay.
  ◦ Participated in **Robotics Workshop** in MSRIT Bangalore, 2007.
  ◦ Participated & Organised a Hands-on Workshop on **'FPGA based design for VLSI Applications'**.
  ◦ Participated as a **Delegate** in Pratyaksha-08, MSRIT Bangalore.

HOBBY

- Singing, Painting, Travelling to new places & Internet Surfing.