Soumitra Pal

Contact Information

Department of Computer Science and Engineering
Indian Institute of Technology – Bombay
Circular Hall, Kanwal Rekhi Building (KReSIT)
Hostel No. 12, Room No. C-422
Powai, Mumbai, MH 400076, India

Cell: +91 98697 73453
Fax: +91 22 2572 0022
Email: mitra@cse.iitb.ac.in
Web: www.cse.iitb.ac.in/~mitra

Research Interests

Algorithms, Combinatorial Optimization, Parallel and Distributed Systems

Education

Indian Institute of Technology – Bombay, Powai, Mumbai, India

Ph.D., Computer Science and Engineering, (expected submission: December 2011)

- Thesis Topic: *Component Coloring of Graphs and its applications to scheduling transmissions on Reconfigurable Bus Systems*
- Advisor: Professor Abhiram G. Ranade
- Area of Study: Graph Theory, Approximation Algorithms, Online Algorithms, Branch-And-Price based Exact Algorithms
- CPI: 9.0/10 (course work and seminar)

M.Tech., Computer Science and Engineering, August 2007

- Thesis Topic: *Improving Branch-And-Price algorithms for solving one dimensional cutting stock problem*
- Advisor: Professor Abhiram G. Ranade
- Area of Study: Branch-And-Price based Exact Algorithms
- CPI: 9.11/10

Bengal Engineering and Science University, Shibpur, Howrah, West Bengal, India

B.E., Computer Science and Technology, July 2000

- Thesis Topic: *Synthesis of Cellular Automata and Multiple Attractor Cellular Automata based classification*
- Advisor: Professor Parimal Pal Chaudhuri
- Area of Study: Cellular Automata
- Marks: 85.2%

Publications

Ajit Diwan, Soumitra Pal, and Abhiram Ranade. "Component Coloring of Interval Graphs." In preparation.

Soumitra Pal, and Abhiram Ranade. "Scheduling Light-trails on WDM Rings." Submitted to: *Journal of Parallel and Distributed Computing*.

Soumitra Pal, and Abhiram Ranade. "Scheduling Light-trails on WDM Rings." In: *Proceedings of the 17th International Conference on Advanced Computing and Communications (ADCOM'09)*, Bangalore, India. December 2009.

Soumitra Pal, Ish Dham, and Tor E. Jeremiassien. "Design and Validation Techniques to Implement a Robust Hindsight Feature on ISA Simulators." In: *Global Signal Processing Expo and Conference – GSPx*, Santa Clara, USA. September 2004. [Unrefereed].

Soumitra Pal, and Prem Kumar Vadapalli. "A methodology for Saving and Restoring the State of ISA simulators." In: *Global Signal Processing Expo and Conference – GSPx*, Santa Clara, USA. September 2004. [Unrefereed].

Academic Experience

Indian Institute of Technology – Bombay, Mumbai, India

Teaching Assistant **July 2005 to June 2009**

- Assisted in evaluating quiz, homework, exam, lab assignments and also scribed lecture notes for the following courses:
  - CS 101: Computer Programming Utilization — Autumn '05
  - CS 218/CS 301: Design and Analysis of Algorithms — Autumn '07, Spring '09
  - CS 435: Linear Optimization — Autumn '06
  - CS 606: Foundations of Parallel Computing — Spring '07, Spring '08

Web Administrator **January 2007 to June 2007**

- Maintained the *PhpWebSite* based departmental website by updating department related information on a regular basis.

Professional Experience

IBM India Research Lab. (IRL), Bangalore, India

Research Intern **May 2011 to July 2011**

- Topic: *Phase Identification in Smart Grids using Analytics*
- Mentors: T. S. Jayram, Vijay Arya

Texas Instruments (TI), Bangalore, India

Senior Software Design Engineer **July 2002 to June 2005**

- Worked with team to design and implement 'backward step' and 'backward run' feature in the Instruction Set Simulators (ISS) for the TI DSPs using lightweight check pointing of the ISS state
- Worked with team to design and implement enhancements to the standalone (loader) client application for ISS
- Worked with team to design and implement software interfaces for integrating ISS to different integrated development platforms – TI Code Composer Studio, Vitio Virtual Platform Simulators, Mentor Graphics Seamless CVE

Software Design Engineer **July 2000 to June 2002**

- Implemented new features and improved performance of the ISS for TMS320C54XX series of DSPs
- Implemented a multiprocessor ISS for TMS320C5421 DSP
- Designed a methodology to implement check pointing and restarting state of the ISS for the TMS320C55XX series of DSPs

Programming Languages

C, C++, Java, Visual Basic, Perl, PHP, UNIX shell scripting, Matlab

References

Dr. Abhiram G. Ranade
- Professor, Computer Science and Engineering
- Indian Institute of Technology – Bombay, Powai, Mumbai, MH 400076, India
- Email: ranade@cse.iitb.ac.in; phone: +91 22 2572 7734

Dr. Ajit A. Diwan
- Professor, Computer Science and Engineering
- Indian Institute of Technology – Bombay, Powai, Mumbai, MH 400076, India
- Email: aad@cse.iitb.ac.in; phone: +91 22 2572 7720

Dr. Sundar Vishwanathan
- Professor, Computer Science and Engineering
- Indian Institute of Technology – Bombay, Powai, Mumbai, MH 400076, India
- Email: sundar@cse.iitb.ac.in; phone: +91 22 2572 7727