P.D.ANEESH

Electrical Engineering

Indian Institute of Technology, Bombay

Specialization: Electronic Systems

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M.Tech.

Male

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Academic Achievements

- Scored 99.9 % in GATE 2011 & Scored 99.8 % in GATE 2010
- Secured 14^{th} rank in All India Jr. Maths Olympiad
- Runner up of state level Chess Championship Spardha'2010 at IT-BHU
- Winner of Best student award in school

Area of Interest

- Digital VLSI Design
- Embedded Systems Design

Technical Proficiency

Operating Systems	:	Windows, Linux (Ubuntu)
Programming Languages	:	Hardware Description Language (VHDL, Verilog), Visual Basic,C, C++, Assembly Language (8085,8086,8051)
DSP Processor	:	TMS320VC33
Softwares/Tools	:	NGSPICE, Xilinx ISE, Altera Quartus, Modelsim, GHDL, MATLAB, Magic Layout Editor, Keil, Proteus, Microsoft Visual Stdio, LaTeX

Key Academic Projects

- **M.Tech Project - Architecture Modelling of Multicore processors**
  (Guide : Prof. M.P.Desai, IIT Bombay) **[Jan '13 - present]**
  - **Description:** This project aims at finding the parameters that can be the bottleneck in the performance of a multicore processor.
  - **Ongoing:** Designing protocol for multicore shared cache system.

- **Research and Development Project - Design and validation Cache models**
  (Guide : Prof. M.P.Desai, IIT Bombay) **[Jan '13 - present]**
  - **Completed Work:** Using simulator SiTAR,designed in IIT Bombay, modelled a Cache with size and policies as its parameters which will be used to provide realistic behavior of a cache in future simulations.
  - **Ongoing:** Designing shared cache system model.

- **B.E. Major Project - Automatic Solar Radiation Tracker**
  (Guide : Prof. K. Uma, BIT Durg) **[Jun '10 - April 2011]**
  - Automatically align the solar panel along with sun to get the maximum efficiency out of solar panel.
  - Temperature sensors were used to keep track of sun. Enhances the efficiency to 6-7 %

TECHNICAL SEMINAR

- To review methods of implementing Floating Point Algorithm on Fixed Point Processors (*M.Tech Seminar, IIT Bombay*) (Dec 2011)

Relevant Courses

- Digital VLSI Design
- System Design
- CMOS Analog VLSI Design
- Embedded System Design
- Digital Signal Processing
- VLSI Design Lab
- Microprocessor Application in power
- Sensors & Instrumentation
- Electronic System Design
- BioMEMS

Course Projects

- **VLSI Design project** (Oct 2012)
  - **3:8 Decoder**
    - Designed a 3:8 Decoder with given specification of time and capacitances.
    - Layout of the designed decoder is done using MAGIC Layout Editor.
- **Analog Design project** (Oct 2012)
  - **Resistance Deviation to Frequency Deviation Converter**
    - Modelling the Resistance Deviation to Frequency Deviation Converter using Macro Models and to optimally design the OPAMP in it
    - Design of Differential OPAMP is carried out with the help of NGSPICE, while the layout work is done in MAGIC LAYOUT TOOL
- **VLSI design lab projects** (April 2012)
  - **8085 Processor**
    - Designing a mimic of famous 8085 microprocessor architecture using hierarchial structural modelling in VHDL
    - 8085 architecture consists of Interupt handling,Bus handling,ALU and Instruction Decoding structures
  - **Run Length Coder**
    - Designed Run Length Coder in VHDL to compress incoming bit string
  - **Serial Communication reciever**
    - Designed a Serial bit reciever system which can recieve train of data frames with phase shift and frequency mismatch w.r.t the clock of reciever system
- **Glitch Free Reset Stabalized Amplifier** (*Electronics System Design course project*) (October 2011)
  - Objective of project was to amplify low level signal (like biomedical signals) while restoring the baseline of signals to increase the accuracy of measurement
  - Circuit was designed which continuously tracks the input signal and restores the baseline of the signal when it excurses out of the specified range
- **BLDC motor Back EMF Filter** (*Digital Signal Processing course project*) (October 2011)
  - Objective of project was to filter out the back emf produced during the operation of BLDC motor using IIR filter
  - Back EMF filtering enhances the performance of BLDC motor by suppressing PWM noise
- **Ultrasonic Distance Measurement System** (*Embedded System Design course project*) (April 2012)
  - Objective of the project was to measure the distance of an obstacle using Ultasonic transducers and display it on a LED setup.
  - Ultrasonic sensors were used in burst mode and the recieved signal was passed through a rectifier circuit to form a big pulse. Thus avoiding error in input voltage level due to noise.
- **Implementation of Single and Multi Cycle MIPS Architecture** **[April '12]**
  - Designed in Verilog with datapath (specified structually) and control-path (specified using state machines behaviorally) for a limited instruction set.
  - Verified using MARS MIPS assembler

Positions of Responsibility

Research Assistant, IIT Bombay

- Research Assistant, Contrubuting in embellishment of lectures for online courseware of *CDEEP (an initiative of IITB)*
- Volunteer member of the commitee for technical competitions & exhibitions conducted as a part of PHEONIX-2010 - A National Level Technical Symposium, organised by BIT Durg

HOBBY

- Listening Music, Table Tennis , Computer Games & Playing Violin