

EDUCATION			
Year	Degree/Certificate	Institute/School, City	% / CGPA
2011	M.Mgt, Strategy and Finance	SJMSOM, IIT Bombay	8.52/10
2007	B.Tech, Electrical Engineering	IIT Madras, Chennai	8.17/10
2002	Class XII	Instrumentation limited School, Kota (CBSE)	80.4
2000	Class X	Mayoor School, Ajmer (CBSE)	85.4

PROFESSIONAL EXPERIENCE			49 Months
STMicroelectronics India Pvt. Ltd.	Senior Design Engineer	Sep 2010-July 2011	
STMicroelectronics is an Italian-French electronics and semiconductor manufacturer with around 53000 employees			
Responsibilities:			
<ul style="list-style-type: none"><li>• Was instrumental in <b>project scheduling</b> which required in depth understanding of the customer requirements</li><li>• <b>Initiated</b> to <b>automate</b> the complete <b>verification environment</b> to <b>reduce the cycle time</b> to hours instead of man weeks</li><li>• Responsible for continuous interaction with the <b>cross functional team</b> across different <b>geographies</b></li><li>• Took the <b>initiative</b> to conduct <b>seminar</b> on <b>verification methodology</b> at <b>IIT Delhi</b> and <b>Delhi college of Engineering</b></li><li>• Responsible to <b>guide the level 1 engineers</b> through various technical and one to one doubt clearing sessions</li><li>• <b>Re-designed</b> the structure and architecture of the chip to make the design and verification environment suitable for <b>reuse</b></li><li>• Worked with high level technical people on the 28-32nm technology which is still in the nascent stage</li></ul>			
Cypress Semiconductor India Pvt. Ltd.	Senior Design Engineer	Jun 2007-Sep 2010	
Cypress Semiconductor Corporation is a silicon valley based semiconductor design and manufacturing company			
Responsibilities:			
<ul style="list-style-type: none"><li>• <b>Led</b> the team for <b>innovation and cycle time reduction</b> to efficiently debug the chips at the silicon stage</li><li>• <b>Led</b> the team for <b>Design and process improvement</b> in order to <b>reduce the cycle time</b> and human error</li><li>• <b>Automated</b> complete verification of CACHE memory. Designed and verified almost all the components of a programmable solution on chip (PSOC), NVL, MEMORY, FLASH, GPIO ports , CPU and AHB-protocol</li></ul>			
Achievements:			
<ul style="list-style-type: none"><li>• <b>Awarded</b> a <b>certificate</b> and <b>cash prize</b> for creating an “<b>External interface model</b>” for chips thereby <b>reducing the cycle time</b> to many folds. This saved <b>10 man weeks</b> for <b>Cypress worldwide</b> and was included in the <b>best practices</b></li><li>• <b>Awarded</b> a <b>certificate</b> and <b>cash prize</b> for designing a “<b>Debug tool</b>” which saved <b>4.4 man weeks</b> for <b>Cypress worldwide</b></li><li>• <b>Awarded</b> a certificate of appreciation for successfully completed the training on PSOC-mixed signal array</li></ul>			

ACADEMIC ACHIEVEMENTS		
<ul style="list-style-type: none"> <li>CFA Level 2 cleared in June 2012</li> <li>CFA Level 1 cleared in December 2011</li> <li>Secured an <b>All India Rank 15</b> out of <b>approximately 27000</b> aspiring candidates in <b>JMET 2011</b></li> <li>Awarded a <b>PPO</b> from <b>Cosmic Circuits</b> for doing <b>Digital implementation</b> on FPGA kit and all round performance during my internship period in engineering</li> <li>Completed finance courses from other department in <b>IIT Madras</b> such as <b>Security and Portfolio management, Accounting for managerial controls, Financial services for managerial decisions, Economics for industrial organization, Financial Economics, Probability and Random process</b> with <b>8.166/10 GPA</b></li> <li>Secured an <b>All India Rank 407</b> out of <b>approximately 3 lakh</b> aspiring candidates in <b>IIT-JEE 2003</b></li> <li>Awarded a <b>certificate</b> from Rajasthan Roadways Ajmer for securing a top rank in IIT-JEE 03</li> <li>Awarded with a best <b>all-rounder</b> at the school level for active participation in academic, sports, and painting</li> <li><b>Consistent performance</b> in getting <b>1st rank</b> in class from <b>class I to class XI</b> at school level</li> </ul>	2011-12 2010-11 2010-11 2006-07 2006-07 2002-03 2003-04 2005-06 1990-01	

POSITIONS OF RESPONSIBILITY		
Position	Key Achievement	Period
Volunteer, General Arrangement, <b>Shaastra 2003, Annual Technical Festival</b> of <b>IIT Madras</b>	Successfully managed along with the other team members in all the infrastructure and general arrangements for all the participating teams.	2003-04

EXTRA-CURRICULAR ACTIVITIES		
<ul style="list-style-type: none"> <li>Volunteer, Avenues G20 manthan summit in SJMSOM 2011</li> <li>Part of the <b>National Social Service</b> (Campus patrolling team) at IIT M, aimed to improve the security of campus</li> <li>Won the <b>general knowledge</b> quiz and <b>Hindi declamation competition</b> held at school level</li> <li>Won the <b>table tennis competition</b> held at St. Paul School at district level</li> <li>Won <b>consolidation prize</b> in a <b>drawing competition</b> and <b>poster competition</b> organized by Rotary club</li> </ul>	2011-12 2003-04 1996-97 1996-97 1996-97	