Sabareesh Nikhil Chinta

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Year(s)	Assessment	Board/University	CPI/Grade/Percentage
2010-14	Cumulative Performance Index	IIT Bombay – Electrical Engineering (pursuing minor in Computer Science and honors)	9.00
2009-10	International Baccalaureate Diploma Programme	International Baccalaureate	38/42
2007-08	All India Secondary School Examination	ICSE	95.5%

Research Experience

Designing Single Photon Avalanche Photodetectors in CMOS technology with high IQE and low dark current

Guide: Prof. Rajeev J. Ram *(May 2013 – July 2013)*

Research Laboratory of Electronics, Massachusetts Institute of Technology

The project encompasses developing a single photon detector using avalanche photodiodes in Geiger multiplication mode at using standard 90 nm CMOS process with very high quantum efficiency and responsivity and low dark currents at a low operating wavelength of 422 nm and a low temperature of 4K.

Expansion of SPARKS HTML5 circuit simulator to include non-linear and active devices

Mentor: Concord Consortium - **Google Summer of Code** *(June 2013 – September 2013)*

As a part of Google Summer of Code 2013, I have extended a circuit simulator to support non-linear and active devices by extending the code to include time functionality.

Design and simulation of Si – SiGe photodetectors in 32 nm CMOS technology

Guide: Prof. Rajeev J. Ram *(May 2012 – July 2012)*

Research Laboratory of Electronics, Massachusetts Institute of Technology

Reverse-engineered IBM's EOS 12 chip and simulated the Si-SiGe photodetectors. I analyzed the effect of several properties of the photodetector on a specific industrial performance metric. I acquired a deep understanding of the device physics factors in play and their incorporation in Sentaurus parameters.

Simulation of 3D trapezoidal bulk FinFET devices in 22 nm CMOS technology

Guide: Prof. Jakub Kedzierski *(July 2012 –) (ongoing)*

Lincoln Laboratories, Massachusetts Institute of Technology (visiting faculty, IIT Bombay)

Simulating FinFETs in Intel's Xeon E3-1230v2 chip using 22nm Ivy Bridge microarchitecture. I am working to develop the structure and optimize simulation parameters to enable more effective meshing.

Other projects - Surface Plasmon Resonance at cylindrical interfaces, Pulsed Power Supply, Statistics of ball tampering, Optical mouse hack implementation

ACADEMIC ACHIEVEMENTS

- Secured *All India Rank 8* in IITJEE 2010, *All India Rank 1* in AIEEE 2010- B.Arch, *All India Rank 99* in AIEEE 2010- B.Tech, *All India Rank 11* in VITEEE 2010 and *All India Rank 31* in ISAT 2010
- Secured *Silver Medal* in the *International Junior Science Olympiad (IJSO) 2008*, held in South Korea
- Recipient of the prestigious *Aditya Birla Group Scholarship* and *OPJEMS* (OP Jindal Engineering and Management Scholarship): the only Aditya Birla scholar from IIT Bombay for the years 2010 - 14, and the only freshman OPJEM scholar from IIT Bombay for the year 2010-11
- Recipient of the esteemed *A*STAR scholarship* offered by the Ministry of Education, Singapore in 2007
- *KVPY and NTSE Scholar*: Awarded the prestigious KVPY scholarship in 2009 and the NTSE scholarship in 2008
- Selected for the *National Chemistry Camp* in the year 2010 and the *National Junior Science* Camp in the year 2008, and was awarded a *gold medal* and a *Special Merit Certificate* respectively
- Secured *All India third rank* twice in National Science Talent Search Examination conducted by Unified Council, and *first rank in Andhra Pradesh* in State Level Talent Search Examination
- Secured *All India first position* in *Aptitude* test, and *All India first* position in *Achievement* test in the year 2005, and *All India first* position in *Aptitude*, *All India first* position in *Mathematics* and *All India second* position in the year 2008, in the *Academic Aptitude and Achievement test*
- *School topper* in both class 10 ICSE and class 12 IBDP

EXTRACURRICULAR ACTIVITIES AND POSITIONS OF RESPONSIBILITY

- *Institute Student Mentor* to mentor a batch of 25 freshmen – responsible for their holistic development
- *Department Academic Mentor* to mentor students with a poor academic performance
- *Teaching Associate for Calculus* (MA 105): one among 10 students selected out of a batch of 800
- *Debating Secretary of Hostel 6*: the only one from the hostel for the year 2011-12
- *Editor* of the official institute magazine – InsIghT, and the department magazine – Background Hum
- *Coordinator, Electronics Club* of IIT Bombay
- Blue-1 belt in Taek won do: *Gold medalist at district level* (heavyweight category)
- *Language enthusiast*: acquainted with French, Japanese, Sanskrit, Telugu, Hindi and English
- Secured *8th in India, and 1st in Hyderabad zone* in the debates on environmental issues conducted by the Association of British Scholars and Tata Steel in the year 2009

COMPUTER SKILLS

Applications Software: Sentaurus, Cadence, Verilog, MATLAB, EAGLE, LTSpice, MatLab, NI LabView, Sage

Programming and Web development Languages: C/C++, Java, Python, Javascript, PHP, MySQL, Facebook API

COURSE PROJECTS – Bloxorz in C++, Greed for Speed in Verilog (http://youtu.be/KUl72Uz-bbE)