Resume.

Arun. Chandrasekharan

arunc@ee.iitb.ac.in

Dept of Electrical Engg – IIT Bombay

Objective:

To seek career challenges in the semiconductor industry in view my past achievements and future goals.

Professional Experience:

Physical Design Engineer, 2006 to 2010.
Wipro Technologies, VLSI Wing.

- Involved in 6 IC tape-outs so far, from 180nm to 55nm technologies.
- Involved in the full chip physical design from 1 million to 10 million gate designs.

Skills:

- Good experience in ASIC/SoC design flow and methodologies.
- Excellent knowledge in Cadence and Synopsys tools used for back end design from synthesis to GDS2.
- Good experience in STA, Synthesis/LEC, PnR, CTS, LVS/DRC, Power/ IRDrop and other signoff aspects of digital design.
- Thorough knowledge of UNIX and networking with scripting skills in tcl, shell, awk, perl etc.
- Skilled at C/C++ and object oriented programming.

Educational Qualifications.:

- MTech – Microelectronics (2^{nd} Year RA)
- Mtech Project – Behavioral synthesis.
    - High level synthesis of digital systems from an algorithm specification in C/C++.
- Courses taken so far:
    - VLSI Design, System Design, Analog Design.

    - Solid State Device Physics, Physics of Transistors, VLSI Technology (Fabrication).
    - VLSI Design Lab(HDL), Microelectronic Simulation Lab(Fabrication and Device Simulation
    - Advanced Computing.
- CPI – 8.55
- Working as system and network admin of the VLSI-Lab, EE Dept, IIT-Bombay.

- BTech
    - Electronics and Communication
    - Model Engg College, Cochin (2006 batch).
    - CPI – 9.0

Address:

Arun. C

Room #523,

H12 – D Wing,

IIT- Bombay.

Place: Powai

Date: 22nd Aug, 2011.