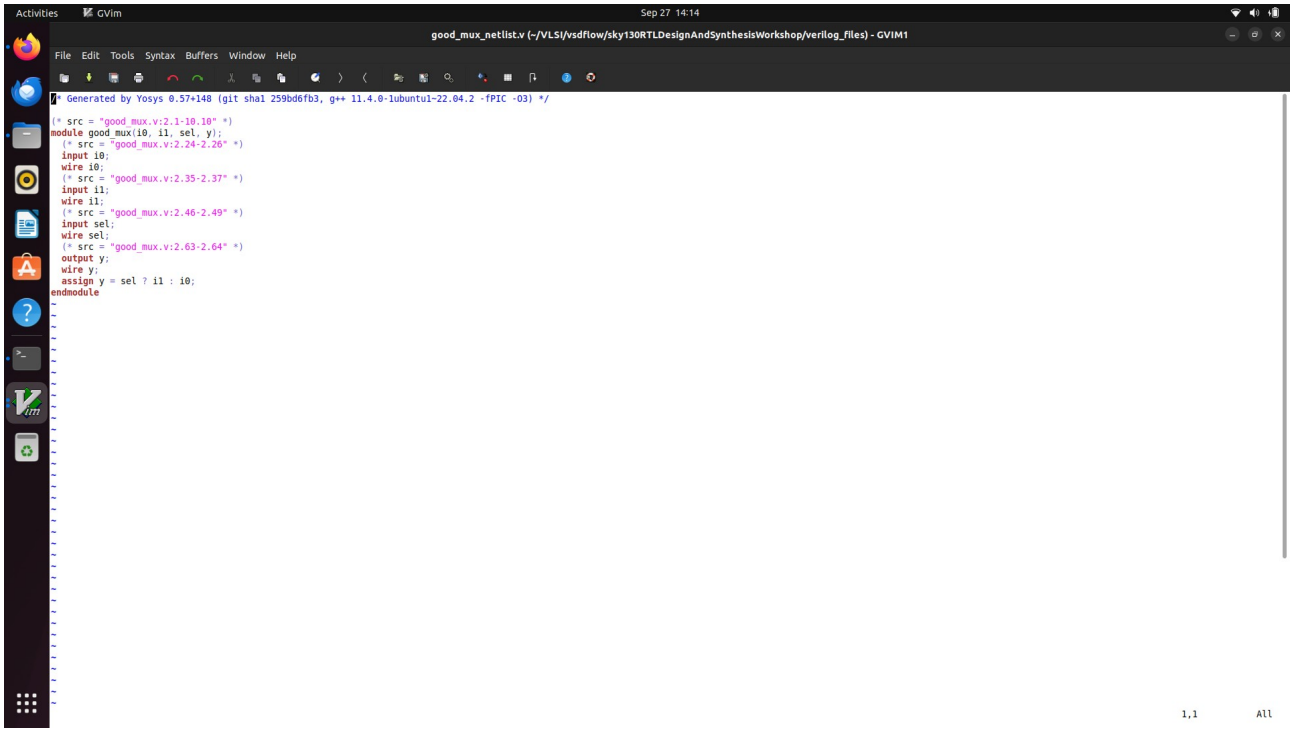
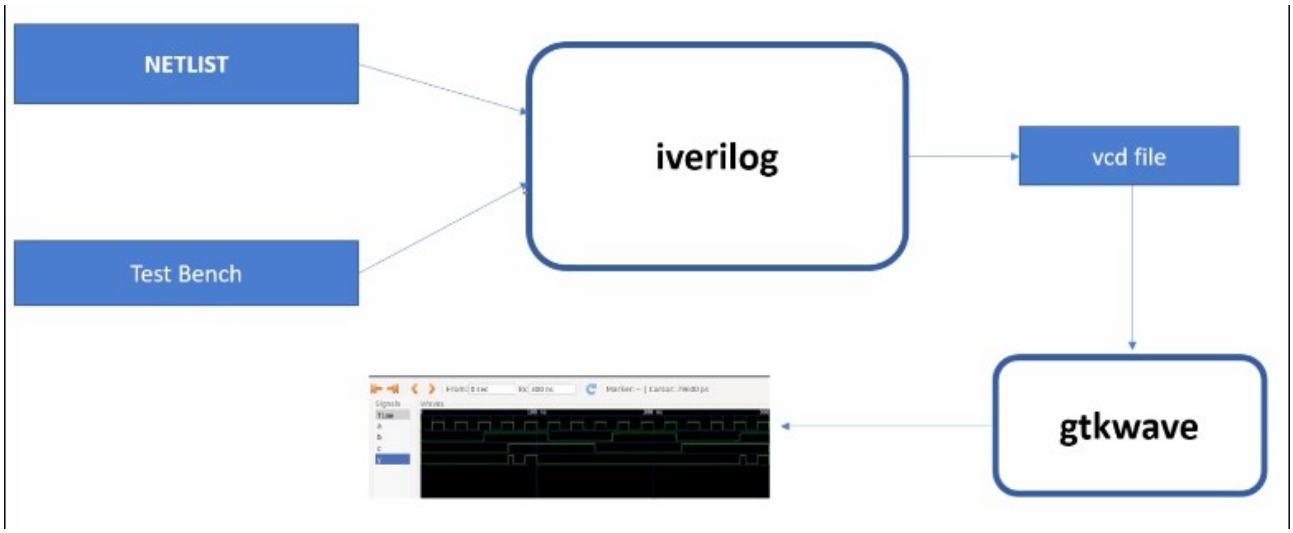
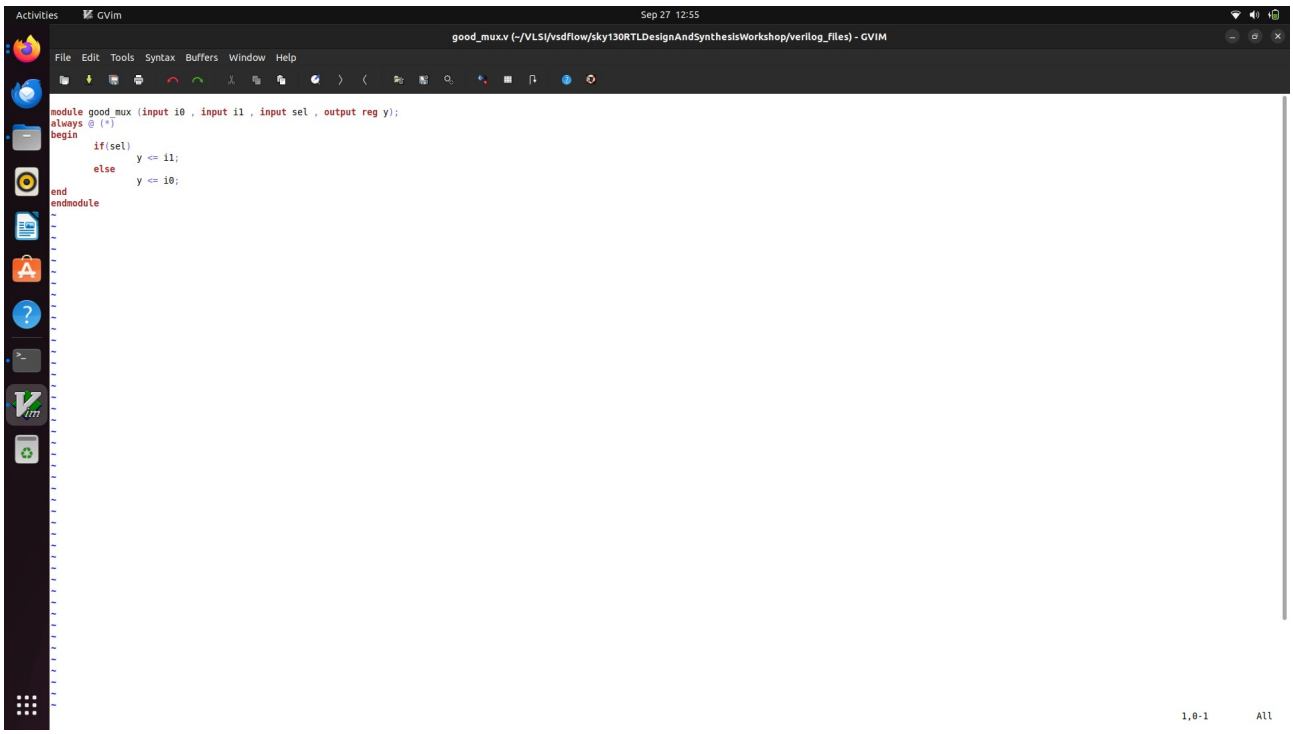

Activities
GVim
Sep 27 14:14
good_mux_netlist.v (~/VLSI/vsdflow/sky130RTLDesignAndSynthesisWorkshop/verilog_files) - GVIM1
File Edit Tools Syntax Buffers Window Help
/* Generated by Yosys 0.57+148 (git sha1 259bd6fb3, g++ 11.4.0-1ubuntu1~22.04.2 -fPIC -O3) */
(* src = "good_mux.v:2.1-10.10" *)
module good_mux(i0, i1, sel, y);
(* src = "good_mux.v:2.24-2.26" *)
input i0;
wire i0;
(* src = "good_mux.v:2.35-2.37" *)
input i1;
wire i1;
(* src = "good_mux.v:2.46-2.49" *)
input sel;
wire sel;
(* src = "good_mux.v:2.63-2.64" *)
output y;
wire y;
assign y = sel ? i1 : i0;
endmodule
1,1 All


NETLIST
Test Bench
iverilog
vcd file
gtkwave




```
=== good_mux ===

        +----------Local Count, excluding submodules.
        |
        4 wires
        4 wire bits
        4 public wires
        4 public wire bits
        4 ports
        4 port bits
        1 cells
        1   $_MUX_
```