TUSHAR GANESH PATIL

Physical Design Engineer | Physical Verification Engineer

+91-9763507705
tushgpats@gmail.com
https://github.com/tushgpats/sfal-vsd
https://www.linkedin.com/in/tushar-ganesh-patil/
Bengaluru, KA

SUMMARY

Master's Graduate in Computer Engineering specializing in physical design, timing analysis, and physical verification. Experienced in standard cell design, circuit optimization, and custom cell integration in Openlane flow. Looking for roles focused on Physical Design, STA, and Physical Verification with a focus on high-performance digital and mixed-signal SoC designs.

EXPERIENCE

Engineer (Volunteer)

Get2spec INC

08/2023 - 07/2024 Tempe, AZ

EDA Company based in Tempe, AZ

- Designed and optimized standard cells (ANDs, NANDs, NORs, XORs, XNORs, AOIs, OAIs) and combinational circuits using Domino Logic and transmission gate logic resulting in 30% more compact circuit.
- Created intricate circuits, such as 32-bit Carry Select adders and Manchester Carry Adders, using domino logic resulting in 20% faster operation.
- Conducted functionality tests on above adders with i-verilog, smash, and gtkwave, ensuring robust performance and adherence to specifications.
- Actively exchanged insights and brainstormed potential business ideas, regularly sharing these with leadership, which helped refine various design approaches.

EDUCATION

M.S, Computer Engineering (Electrical Engineering)

Arizona State University

08/2021 - 05/2023 Tempe-AZ

M.Sc., Physics

University of Mumbai

08/2015 - 05/2018 Mumbai

SKILLS

Synthesis | **Floor planning** | **Power Planning** | **Place and Route** | **Parasitic Extraction** | **CTS** | **DRC** | **LVS** | **STA** | **ECO** | **Conformal LEC** | **Design Compiler** | **ICC2 Compiler** | **Prime Time** | **ICV** | **Star-RC** | **Library Compiler** | **Openlane** | **Verilog** | **System Verilog** | **TCL Scripting**

CERTIFICATION

SoC Design and Implementation

Certification in SoC Design and Implementation from SFAL & VSD (April - Nov 2024)

SystemVerilog for Verification - I

SystemVerilog for Verification by Kumar Khandagale (Udemy)

PROJECTS

Optimizing Clock Tree Synthesis for Enhanced ASIC Performance on a RISC-V SoC using Skywater 130nm PDK.

10/2024 - 11/2024

https://github.com/tushgpats/sfal-vsd

Optimized Clock Tree Synthesis for a RISC-V SoC, focusing on minimizing clock skew and improving timing synchronization across the design.

- *Technology: Skywater 130 nm.*
- Optimized Clock Tree Synthesis (CTS) to enhance RISC-V SoC performance, focusing on precise clock region definition and skew minimization.
- Employed advanced CTS algorithms to improve timing synchronization and power efficiency across the chip.
- Used EDA tools for simulation and validation, enabling detailed clock distribution analysis and boosting chip performance.
- Achieved Positive slack of 0.52 NS even after accounting for a 0.50 NS clock uncertainty which indicates that this robust design can handle variations in operating conditions while maintaining reliable performance.

Congestion-Aware DRC-Compliant Mixed-Signal SoC Design Incorporating RISC-V Processor and Dual Analog IPs

09/2024 - 10/2024

https://github.com/tushgpats/sfal-vsd

Achieved a highly optimized, congestion-aware mixed-signal SoC design with a peak congestion of just 0.05% and zero DRC violations, integrating a RISC-V processor and dual analog IPs.

- *Technology: Skywater 130 nm.*
- Analyzed and resolved potential Design Rule Check (DRC) violations in placement and routing phases.
- Optimized core utilization, addressing layout congestion and DRC violations in mixed-signal SoC with RISC-V processor and dual analog IPs.
- Maintained noise isolation and compliance with PDK constraints, ensuring reliable performance across digital and analog sections.

Transient analysis of an Inverter Cell and integration into Openlane flow.

07/2024 - 08/2024

https://github.com/tushgpats/sfal-vsd

Performed transient analysis of a custom inverter cell and integrated it within the Openlane flow for complete PnR implementation

- Performed transient analysis of a custom inverter cell.
- Integrated custom inverter cell in Openlane flow and implemented PnR of a RISC-V core.