2024 / 25

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Ollscoil Teicneolaíochta an Oirdheiscirt

South East Technological University

Module Descriptor

Embedded Systems Architecture & Hardware (Computing and Mathematics)

Embedded Systems Architecture & Hardware (A11982)

Short Title: Embedded Sys Arch & Hardware
Department: Engineering Technology
Credits: 5 **Level:** Advanced

Description of Module / Aims

This module is concerned with the embedded architecture of high performance processor systems and modern memories. The module aims to teach the skills and techniques used in designing embedded systems hardware. The importance of timing parameters and worst-case design will be emphasised and students will be exposed to Hardware Descriptive Language (HDL) and associated development tools for hardware design.

Programmes

		stage/semester/status
EMBS-0003	BEng (Hons) in Information Engineering (International) (WD_EEELC_BI)	4 / 7 / M
EMBS-0003	BSc (Hons) in Applied Computing (WD_KACCM_B)	4 / 7 / E
EMBS-0003	BSc (Hons) in Computer Science (WD_KCMSC_B)	4 / 7 / E
EMBS-0003	BSc (Hons) in the Internet of Things (International) (WD_KINTT_BI)	4 / 7 / M
ENGR-0019	BEng (Hons) in Electronic Engineering (WD_EONIC_B)	4 / 7 / M

Indicative Content

- Overview of Computer Architecture
- Memory Management Unit (MMU), Cache Memories, External Memory controllers (EMC)
- DC and AC analysis (Timing analysis), data sheet parameters interpretation
- Input/Output design, multiprocessor design and arbitration issues
- Flash, SRAM, SSRAM, DDR SDRAM memories: characteristics, timing diagrams and interfaces
- Development tools and hardware design using Hardware Descriptive Language (HDL), basic processor architecture design

Learning Outcomes

On successful completion of this module, a student will be able to:

1. Describe computer architecture elements
2. Design and draw I/O subsystems, and arbitration circuits for multiprocessors
3. Interpret data sheet parameters and perform timing analysis for design evaluation
4. Perform basic calculations pertaining to design parameters
5. Use development tools and design flow methodology relating to HDL hardware design
6. Design, debug, test and verify computer architecture systems described by HDL languages

Learning and Teaching Methods

- Lectures and tutorials
- Practicals
- Mini-Project

Learning Modes

Learning Type	F/T Hours	P/T Hours
Lecture	36	
Practical	12	
Independent Learning	87	

Assessment Methods

	Weighting	Outcomes Assessed
Final Written Examination	60%	1,2,3,4
Final Practical	40%	5,6

Assessment Criteria

70% – 100%: The learner has: attained the module learning outcomes at an excellent level; demonstrated a comprehensive knowledge of the associated subject matter; achieved an excellent level of the skills required for the subject matter; demonstrated the ability to carry out further investigation and problem solving associated with the subject matter.

60% – 69%: The learner has: attained the module learning outcomes at a very good level; demonstrated a detailed knowledge of the associated subject matter; achieved a very good level of the skills required for the subject matter.

50% – 59%: The learner has: attained the module learning outcomes at a good level; demonstrated a good knowledge of the associated subject matter; achieved a good level of the skills required for the subject matter.

40% – 49%: The learner has: attained the module learning outcomes at a basic level; demonstrated a basic knowledge of the associated subject matter; achieved a basic level of the skills required for the subject matter.

<40%: The learner has not: attained the module learning outcomes; demonstrated sufficient knowledge of the associated subject matter; demonstrated a sufficient level of the skills required for the subject matter.

Essential Material(s)

- Furber, S. *Arm System-on-Chip Architecture.* .: Addison Wesley, 2000.
- Ganssle, J., T. Noergaard and F. Eady. *Embedded Hardware: Know It All.* UK: Newnes-Elsevier, 2008.

Supplementary Material(s)

- Andrews, J.R. *Co-verification of Hardware & Software for ARM SoC Design.* UK: Newnes, 2005.