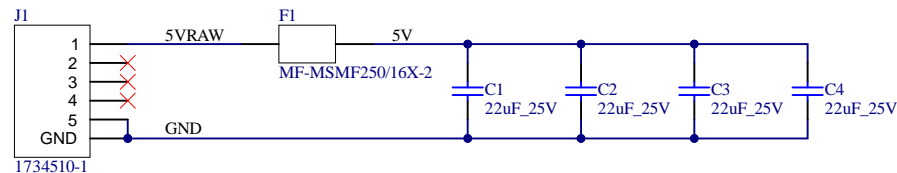
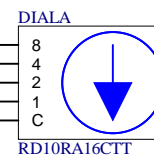
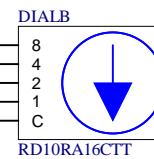
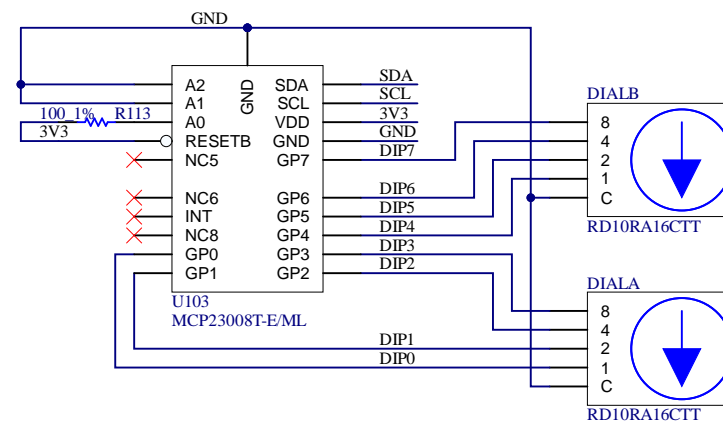
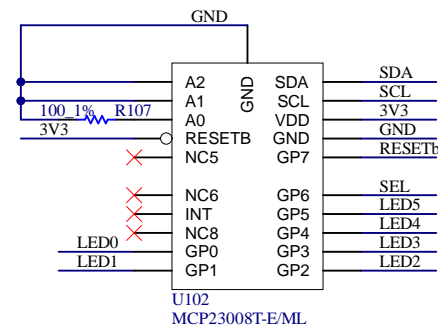
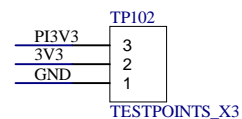
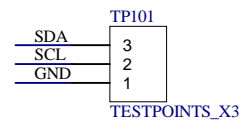
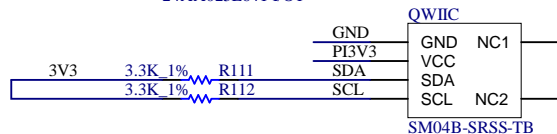
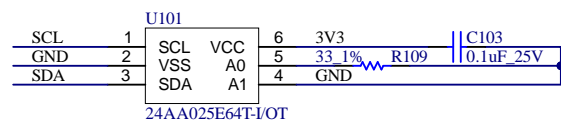
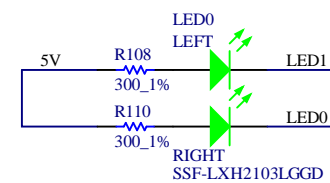
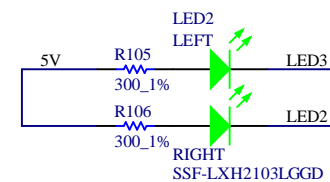
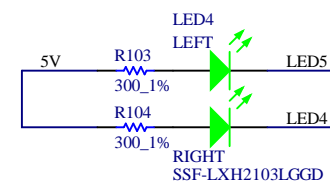
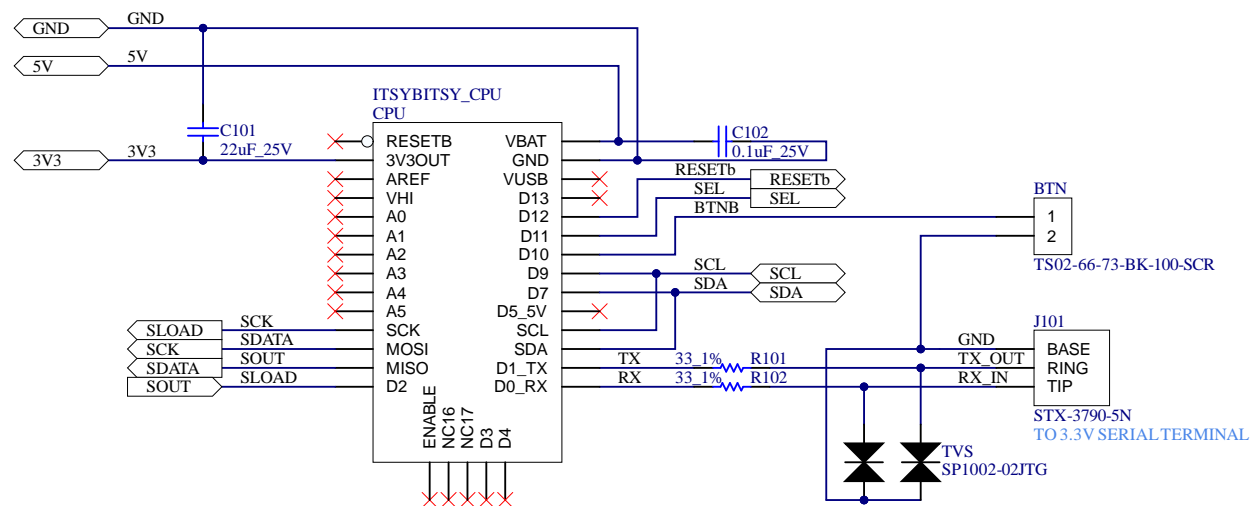


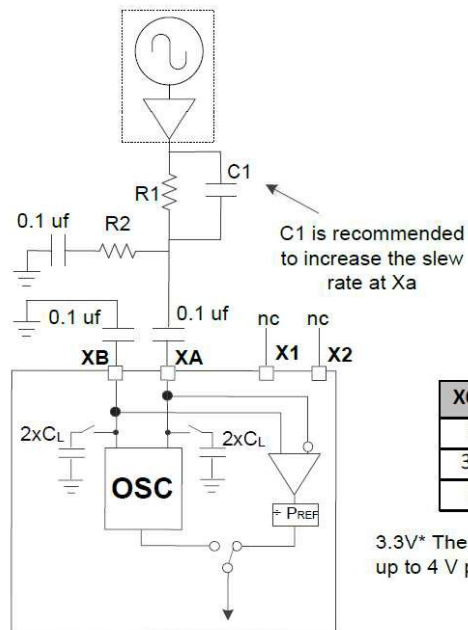
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CW_PLL1
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CW_PLL1
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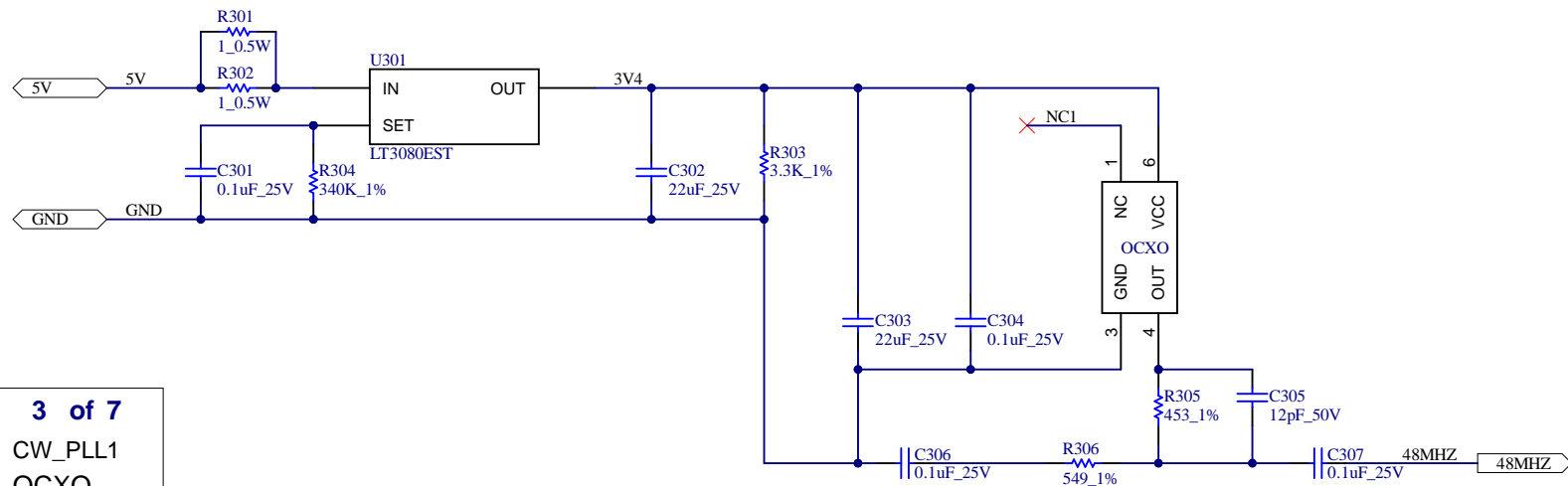
48-54 MHz
XO/Clock
LVCMOS



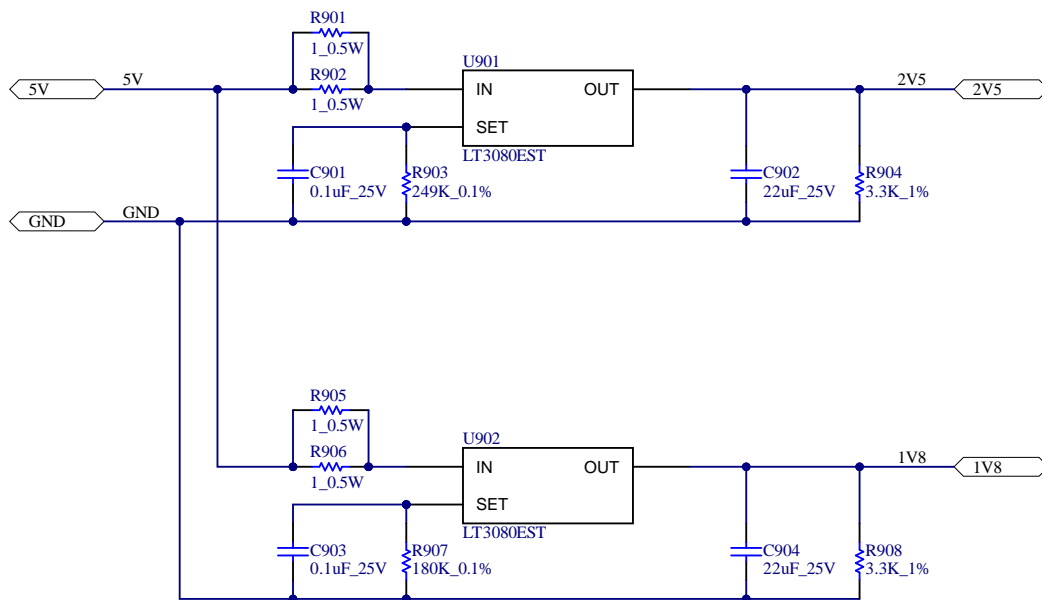
XO VDD	R1	R2	C1
3.3V	453 Ω	549 Ω	12 pF
3.3V *	665 Ω	549 Ω	10 pF
2.5V	274 Ω	732 Ω	30 pF

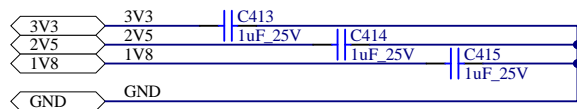
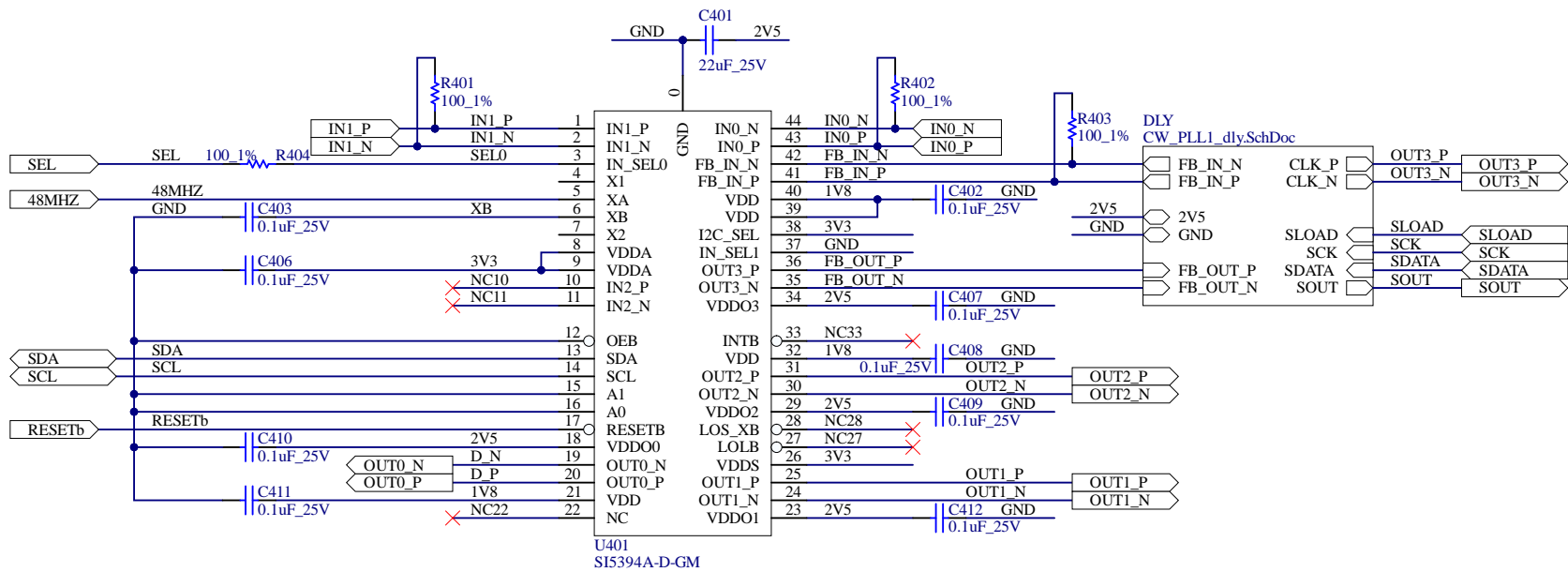
3.3V* These settings should be done if there CMOs level is up to 4 V pp to limit the input at Xa to less than 2V ppse

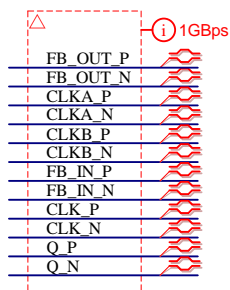
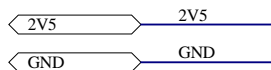
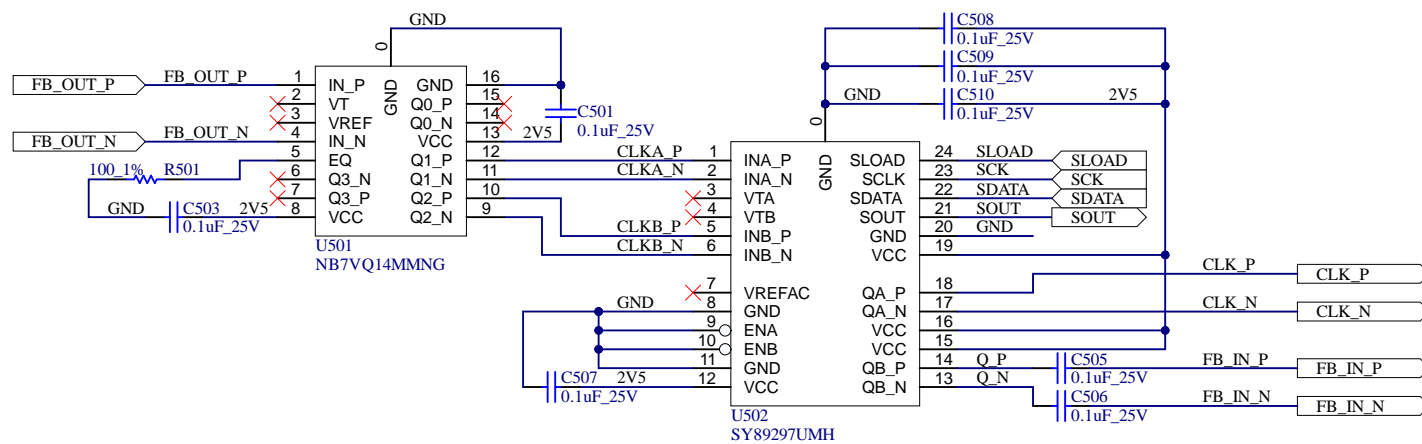
**LVCMOS XO/Clock
Connection
(Not Recommended)**



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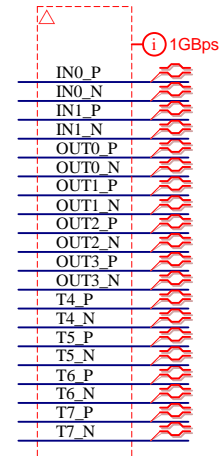
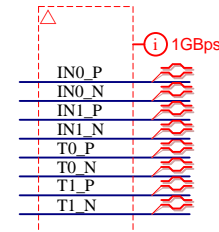
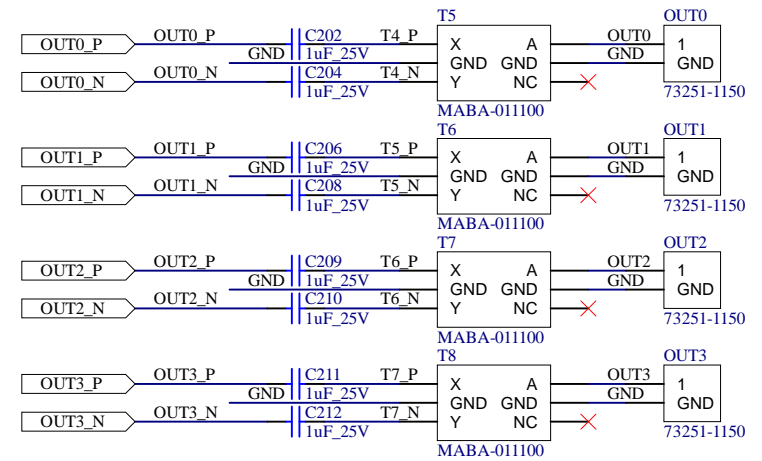
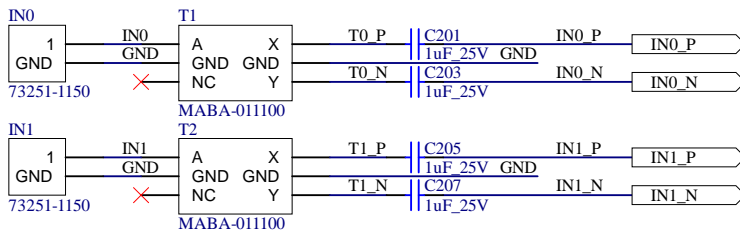






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CW_PLL1

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