Northeastern University

Department of Electrical and Computer Engineering

EECE2323: **Digital Systems Design Lab**

Lecturer: **Dr. Emad Aboelela**

TAs:
Ke Chen
Linbin Chen

Lab # 1-3: **8-Bit Adder, Partial Arithmetic Logic Unit, and Arithmetic Logic Unit**

Group # **???**:
Jin Hyeong Kim,
Timothy VanSlyke

Semester: Spring 2018
Date: February 6, 2018
Lab Session: Tuesday, 1:00PM
Lab Location: 9 Hayden Hall, Northeastern University,
Boston, MA 02115

Contents

1 Introduction

2 Design Approach

3 Results and Analysis

3.1 Design Simulation

3.2 Hardware Testing

4 Conclusions