

Northeastern University

**Department of Electrical and Computer
Engineering**

EECE2323: Digital Systems Design Lab

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**Lab # 1-3: 8-Bit Adder, Partial Arithmetic Logic
Unit, and Arithmetic Logic Unit**

Group # ???:

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**Lab Location: 9 Hayden Hall, Northeastern University,
Boston, MA 02115**

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1 Introduction

2 Design Approach

3 Results and Analysis

3.1 Design Simulation

3.2 Hardware Testing

4 Conclusions

A Lab 3 ALU Verilog Module

```
module eightbit_alu(
    input signed [7:0] a,
    input signed [7:0] b,
    input [2:0] s,
    output [7:0] f,
    output ovf,
    output take_branch
);
    // module-local registers
    reg [7:0] f_reg, ovf_reg, take_branch_reg;
    always @(a, b, s) begin
        // operations on 'f'
        case(s)
            0: f_reg = a + b;
            1: f_reg = ~b;
            2: f_reg = a & b;
            3: f_reg = a | b;
            4: f_reg = a >> 1;
            5: f_reg = a << 1;
            6: f_reg = 0;
            7: f_reg = 0;
        endcase
        // overflow check for addition
        ovf_reg = (s == 0) && ((f[7] != a[7]) || (f[7] != b[7]));
        // 'take_branch' special cases
        take_branch_reg = ((s == 6) && (a == b)) || ((s == 7) && (a != b));
    end
    // continuous assignment to outputs from module-local registers
    assign f = f_reg;
    assign ovf = ovf_reg;
    assign take_branch = take_branch_reg;
endmodule
```