Lab 5: Counters and Clocks

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1 Part I

1. Export the subcircuit schematic as an image and include it in your report.

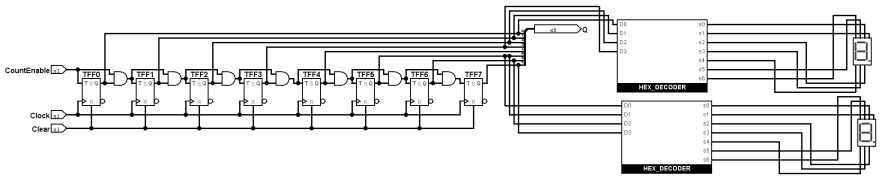

Figure 1: A schematic of counter8.

2. Provide screenshots of your circuit being tested by the poke tool.

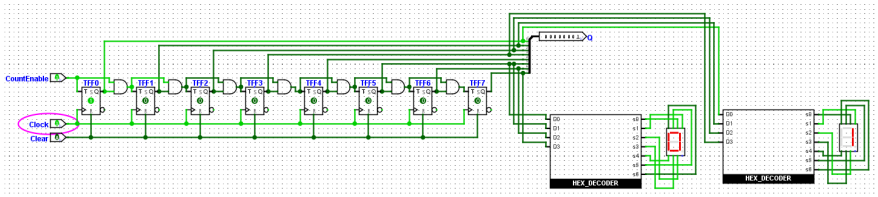

Figure 2: 8-bit Counter Test case 1.

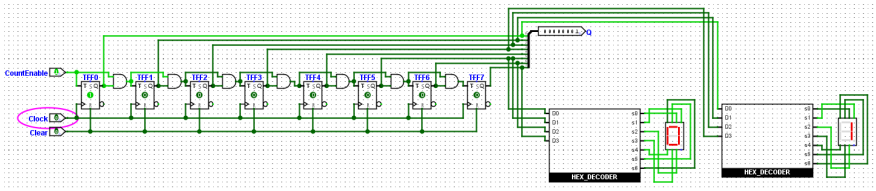

Figure 3: 8-bit Counter Test case 2.

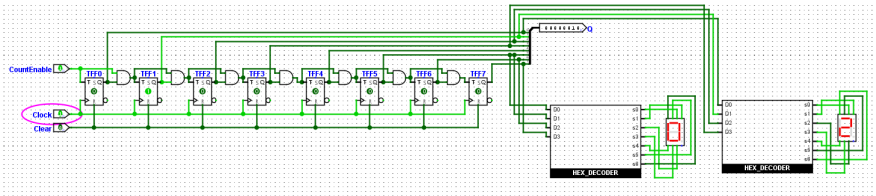

Figure 4: 8-bit Counter Test case 3.

2 Part II

2.1 The Counter Device

1. The check for the maximum value is not necessary in the example above. Explain why.
   The check for the maximum value is not necessary because it's a 4-bit counter, so it won't be able to exceed or count beyond the maximum value of f in hexadecimal or 15 in decimal.

2. If you wanted this 4-bit counter to count from 0-9, how would you adjust the circuit described in the handout?
   We have to change the "Maximum Value" property of the counter from "0xf" to "0x9" if we want this 4 bit counter to count from 0-9.

3. In *Properties* there is a setting called *Action On Overflow*. Explain how each value for this setting responds to overflow by experimenting with this setting and describing the results.
   The wrap around option wraps the values around, bringing the value back to zero after reaching F.

4. Calculate how large a counter would be required to count 50 million clock cycles, as illustrated in the handout. How many binary bits would that counter need to represent such a value?
   We would need a counter that can count from 0 to 49,999,999, that is 50 million. We would need a minimum of 2^{26}.

2.2 The Rate Divider

1. Export the subcircuit schematic as an image and include it in your report.

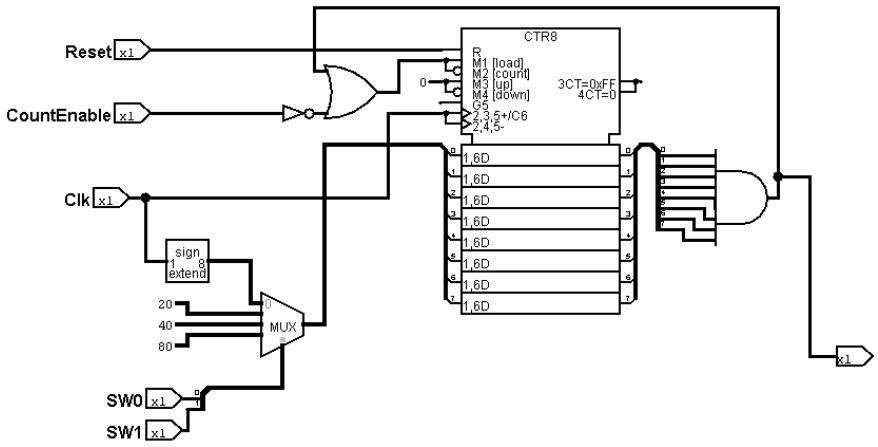

Figure 5: A schematic of rate_divider.

2. Export the timing diagram as an image and include it in your report.

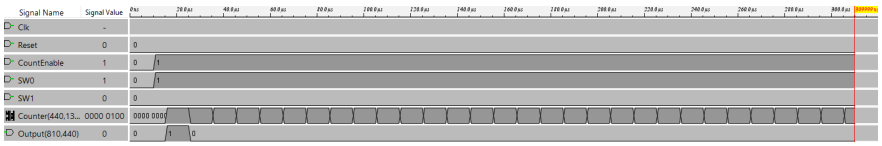

Figure 6: A timing simulation of rate_divider.

2.3 The Main Circuit

1. Include the schematic of the circuit you built. In particular, show how the outputs of the RateDivider feed into the inputs of the DisplayCounter, and how the high-level inputs and outputs connect to your entire circuit. Your main circuit should have one clock input, one reset input and two external switch inputs (SW[1] and SW[0]) for the RateDivider. The circuit should have a seven-segment display as output. HINT: You should

name the inputs and outputs of each module in a way that makes it easy to interpret your simulations (*e.g.* use input/output names from your schematic).

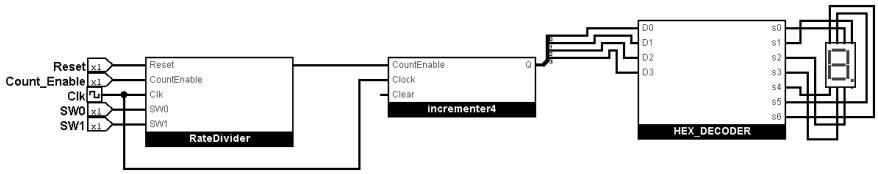

Figure 7: A schematic of the main circuit.

3 Part III

1. Fill in a table with your binary representation of each letter from S to Z.

Letter	Morse Code	Pattern Representation (pattern length is 14 bits)
S	• • •	10101000000000
T	—	11100000000000
U	• • —	10101110000000
V	• • • —	10101011100000
W	• — —	10111011100000
X	— • • —	11101010111000
Y	— • — —	11101011101110
Z	— — • •	11101110101000

Table 1: Morse Pattern Representation with fixed bit-width

2. Export the subcircuit schematic as an image and include it in your report.

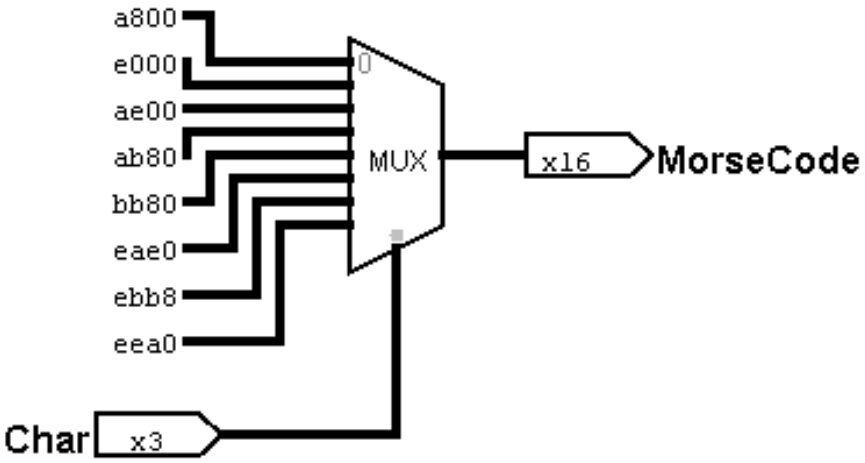

Figure 8: A schematic of MORSE_LUT.