JSS Mahavidyapeetha Sri Jayachamarajendra College of Engineering, Mysore 570 006 An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum





Minimum Register Instruction Sequencing

Report submitted in partial fulfillment of the curriculum prescribed for the award of the degree of

Bachelor of Engineering in Computer Science by

 $Rajkiran\ Anthapur\ Shashidhar\ G\ Vikram\ T.V$ (4JC07CS001) (4JC07CS104) (4JC07CS120)

Under the Guidance of Smt. Vasantha Raghavan Senior Scale Lecturer, Department of CS&E, SJCE, Mysore.

Department of Computer Science & Engineering June, 2011

JSS Mahavidyapeetha

Sri Jayachamarajendra College of Engineering, Mysore 570 006 An Autonomous Institution Affiliated to Visvesvaraya Technological University (VTU), Belgaum





CERTIFICATE

This is to certify that the work entitled "Minimum Register Instruction Sequencing using LLVM Compiler" is a bonafide work carried out by Vikram T.V bearing USN: 4JC07CS120 in partial fulfillment of the award of the degree of Bachelor of Engineering in Computer Science & Engineering of Visvesvaraya Technological University, Belgaum, during the year 2010-2011. It is certified that all corrections/suggestions indicated during CIE have been incorporated in the report. The project report has been approved as it satisfies the academic requirements in respect of the project work prescribed for the Bachelor of Engineering Degree.

Guide Smt. Vasantha Raghavan Senior Scale Lecturer Department of CS&E SJCE, Mysore 570 006 Head of the Department Dr. C.N. Ravi Kumar Professor and Head Department of CS&E SJCE, Mysore 570 006

Date:	Name of Examiner	Signature
Place:	1.	1
	2.	2
	3.	3