## **DECLARATION**

We, Rajkiran Anthapur, Shashidhar G and Vikram T.V, bearing USN: 4JC07CS001, USN: 4JC07CS104 & USN: 4JC07CS120 respectively, hereby declare that this dissertation work entitled "Minimum Register Instruction Sequencing using LLVM" was independently carried out by us under the guidance and supervision of Smt. Vasantha Raghavan, guide, Department of Computer Science and Engineering, Sri Jayachamarajendra of Engineering, Mysore and Shri. Prashantha Naduthota, Professor. This dissertation work is submitted to Visvesvaraya Technological University in partial fullment of the requirements for the award of Degree of Bachelor of Engineering in Computer Science during the academic year 2010 - 2011.

Place: Mysore

Date:

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