**微算機系統**

**小組專案報告**

實驗一

組別： 30

班級、姓名與學號：

資工二 林品緯111590012

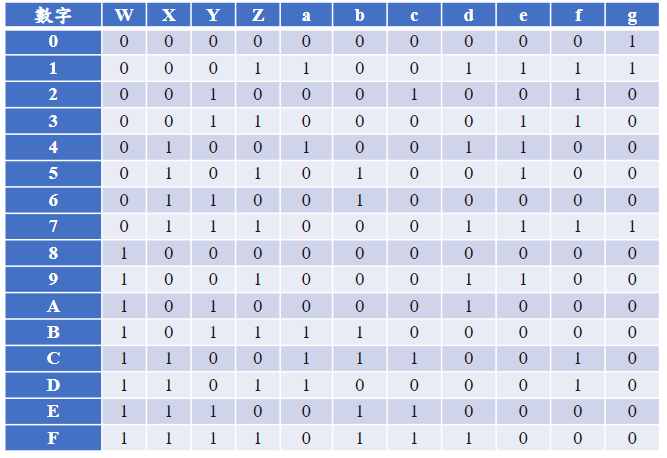
資工二 陳偉瑜111590020

1. 實驗內容：

控制配線，指撥開關控制，七段顯示器控制

1. 實驗過程及結果：

預期實驗結果的真值表

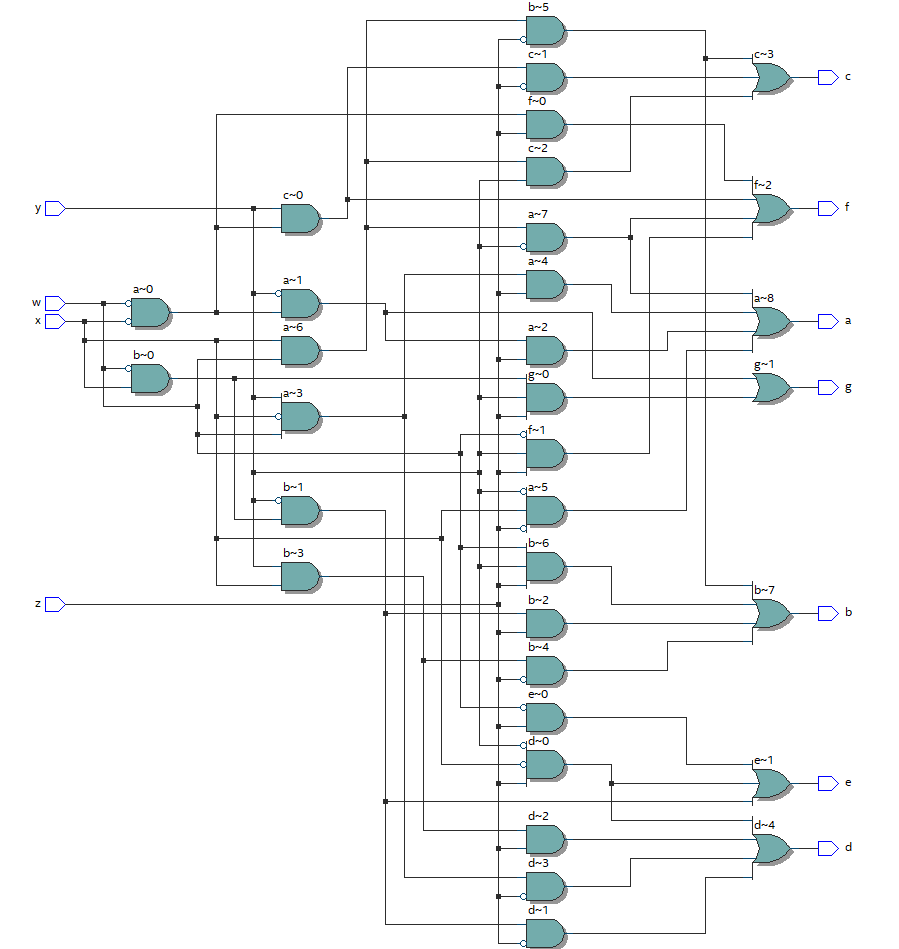


根據上方真值表使用卡諾圖來化簡並設計出電路

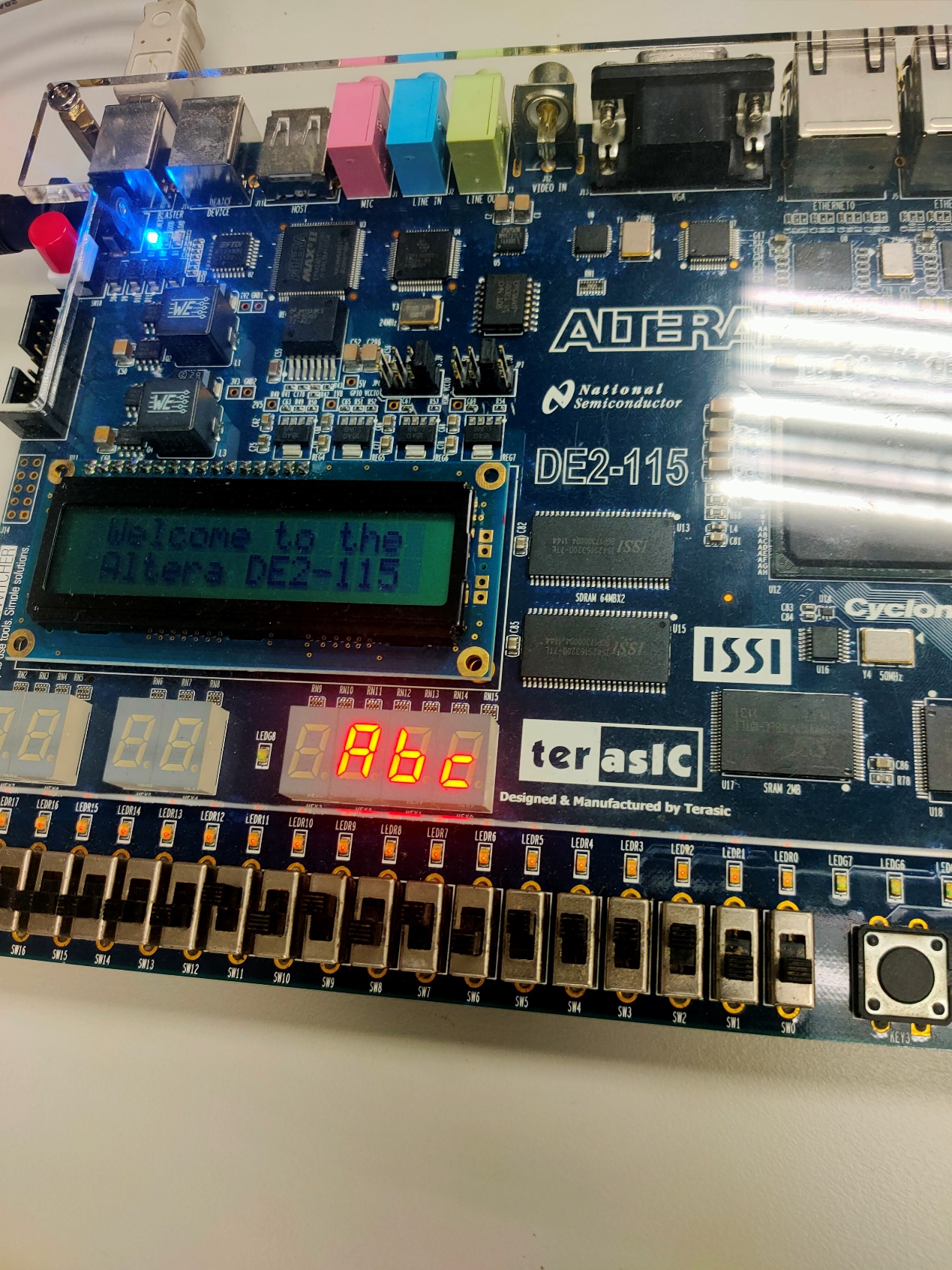
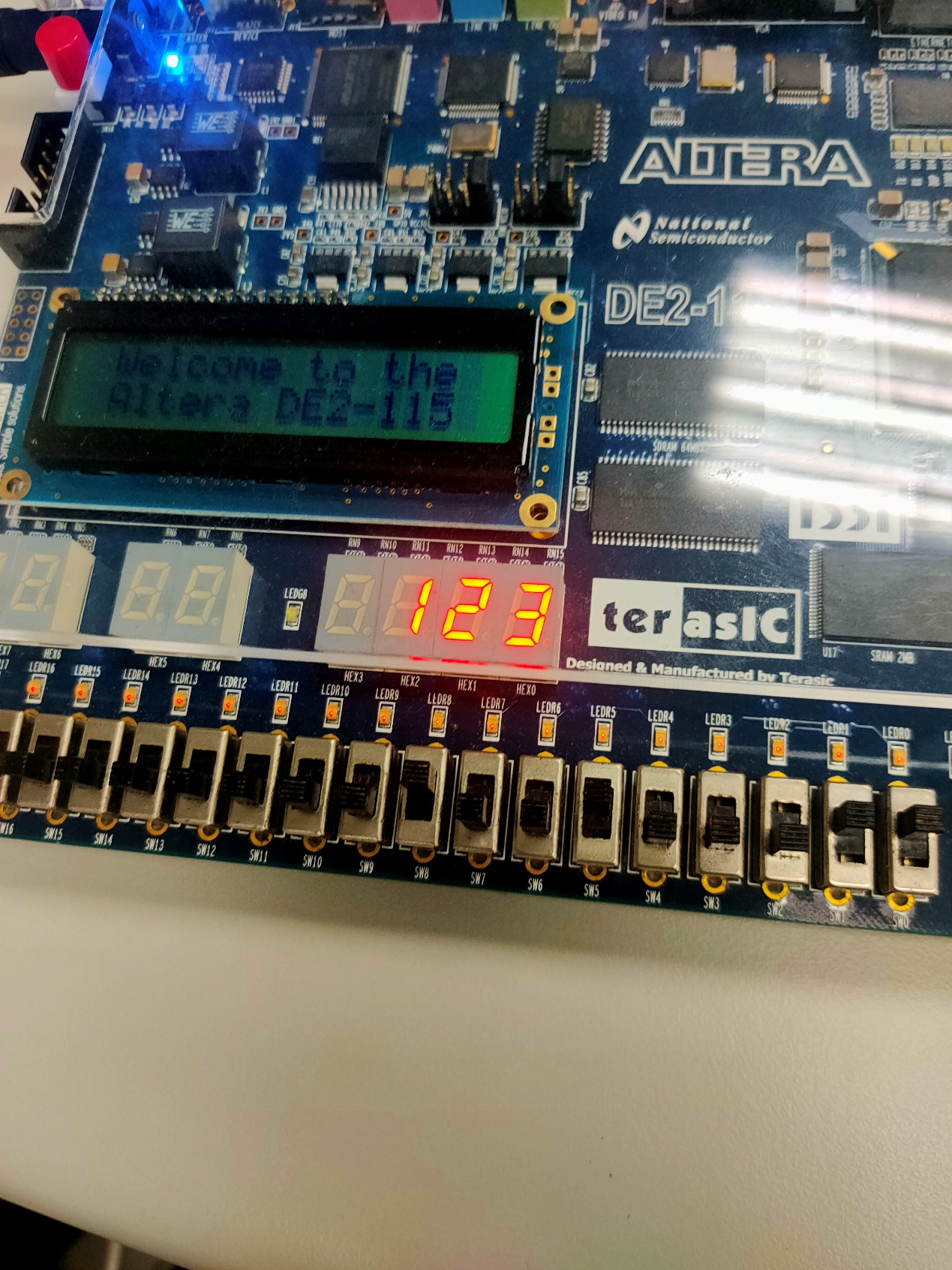
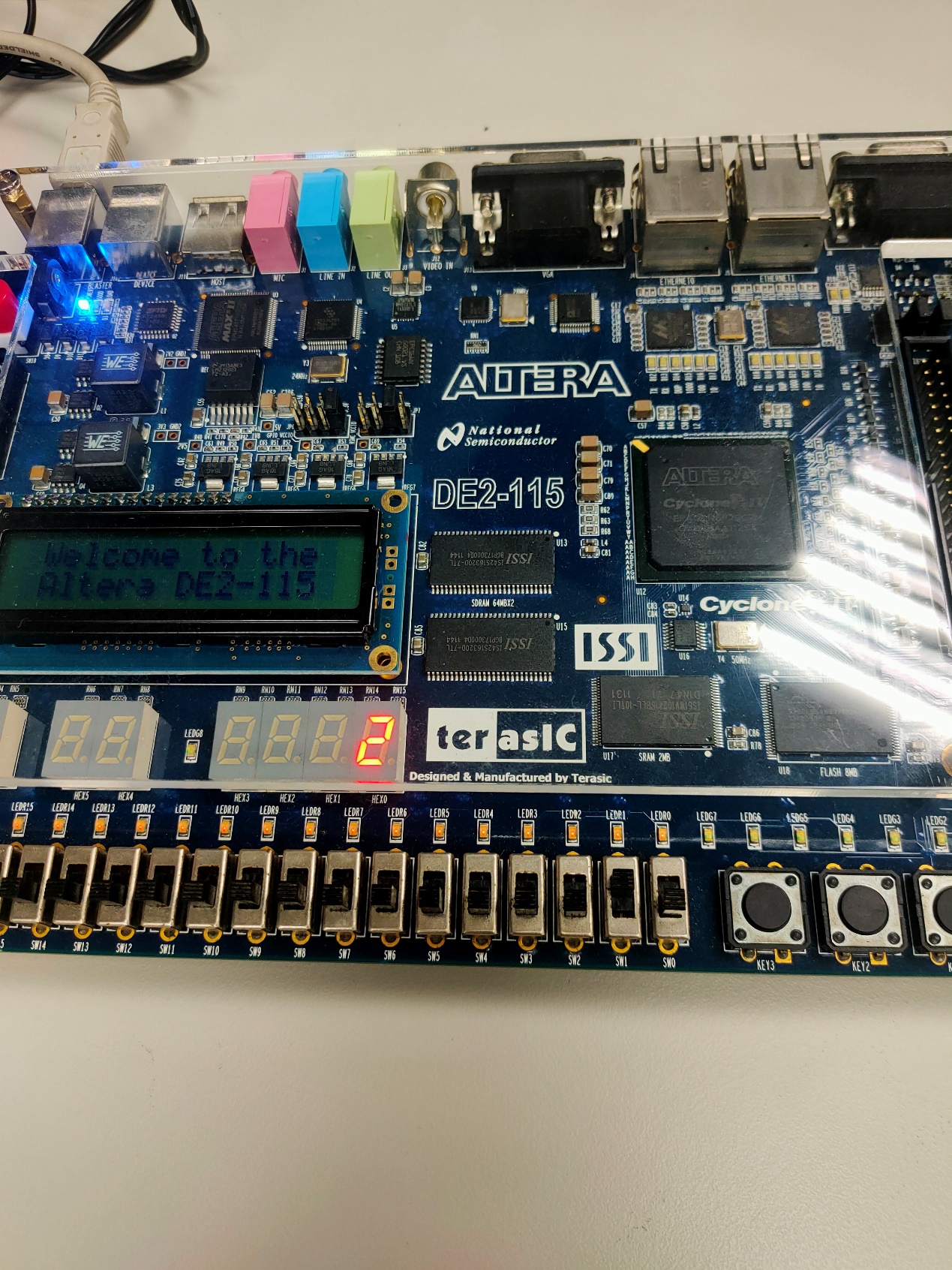
化簡a~g輸出布林代數如下:

電路設計:

下圖為以Quartus之RTL所viewer產生的電路圖



實驗的結果:



1. 程式碼

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| 基本題 |
| library IEEE;  use IEEE.std\_logic\_1164.all;  entity seven\_light is  port(w,x,y,z : in bit;  a,b,c,d,e,f,g:out bit);  end seven\_light;  architecture logic\_fun of seven\_light is  begin  a<=(not w and not x and not y and z) or (w and not x and y and z) or (x and not y and not z) or (w and x and not y);  b<=(not w and x and not y and z) or (x and y and not z) or (w and x and not z) or (w and y and z);  c<=(not w and not x and y and not z) or (w and x and not z)or (w and x and y);  d<=(not x and not y and z) or (not w and x and not y and not z)or (x and y and z)or (w and not x and y and not z);  e<=(not w and z) or(not w and x and not y)or(not x and not y and z);  f<=(not w and not x and z)or(not w and not x and y) or (not w and y and z)or(w and x and not y);  g<=(not w and not x and not y)or (not w and x and y and z);  end logic\_fun; |

|  |
| --- |
| 加分題 |
| library IEEE;  use IEEE.std\_logic\_1164.all;  entity seven\_light is  port(w,x,y,z : in std\_logic\_vector(0 to 2);  a,b,c,d,e,f,g:out std\_logic\_vector(0 to 2));  end seven\_light;  architecture logic\_fun of seven\_light is  begin  a(0)<=(not w(0) and not x(0) and not y(0) and z(0)) or (w(0) and not x(0) and y(0) and z(0)) or (x(0) and not y(0) and not z(0)) or (w(0) and x(0) and not y(0));  b(0)<=(not w(0) and x(0) and not y(0) and z(0)) or (x(0) and y(0) and not z(0)) or (w(0) and x(0) and not z(0)) or (w(0) and y(0) and z(0));  c(0)<=(not w(0) and not x(0) and y(0) and not z(0)) or (w(0) and x(0) and not z(0))or (w(0) and x(0) and y(0));  d(0)<=(not x(0) and not y(0) and z(0)) or (not w(0) and x(0) and not y(0) and not z(0))or (x(0) and y(0) and z(0))or (w(0) and not x(0) and y(0) and not z(0));  e(0)<=(not w(0) and z(0)) or(not w(0) and x(0) and not y(0))or(not x(0) and not y(0) and z(0));  f(0)<=(not w(0) and not x(0) and z(0))or(not w(0) and not x(0) and y(0)) or (not w(0) and y(0) and z(0))or(w(0) and x(0) and not y(0));  g(0)<=(not w(0) and not x(0) and not y(0))or (not w(0) and x(0) and y(0) and z(0));  a(1)<=(not w(1) and not x(1) and not y(1) and z(1)) or (w(1) and not x(1) and y(1) and z(1)) or (x(1) and not y(1) and not z(1)) or (w(1) and x(1) and not y(1));  b(1)<=(not w(1) and x(1) and not y(1) and z(1)) or (x(1) and y(1) and not z(1)) or (w(1) and x(1) and not z(1)) or (w(1) and y(1) and z(1));  c(1)<=(not w(1) and not x(1) and y(1) and not z(1)) or (w(1) and x(1) and not z(1))or (w(1) and x(1) and y(1));  d(1)<=(not x(1) and not y(1) and z(1)) or (not w(1) and x(1) and not y(1) and not z(1))or (x(1) and y(1) and z(1))or (w(1) and not x(1) and y(1) and not z(1));  e(1)<=(not w(1) and z(1)) or(not w(1) and x(1) and not y(1))or(not x(1) and not y(1) and z(1));  f(1)<=(not w(1) and not x(1) and z(1))or(not w(1) and not x(1) and y(1)) or (not w(1) and y(1) and z(1))or(w(1) and x(1) and not y(1));  g(1)<=(not w(1) and not x(1) and not y(1))or (not w(1) and x(1) and y(1) and z(1));  a(2)<=(not w(2) and not x(2) and not y(2) and z(2)) or (w(2) and not x(2) and y(2) and z(2)) or (x(2) and not y(2) and not z(2)) or (w(2) and x(2) and not y(2));  b(2)<=(not w(2) and x(2) and not y(2) and z(2)) or (x(2) and y(2) and not z(2)) or (w(2) and x(2) and not z(2)) or (w(2) and y(2) and z(2));  c(2)<=(not w(2) and not x(2) and y(2) and not z(2)) or (w(2) and x(2) and not z(2))or (w(2) and x(2) and y(2));  d(2)<=(not x(2) and not y(2) and z(2)) or (not w(2) and x(2) and not y(2) and not z(2))or (x(2) and y(2) and z(2))or (w(2) and not x(2) and y(2) and not z(2));  e(2)<=(not w(2) and z(2)) or(not w(2) and x(2) and not y(2))or(not x(2) and not y(2) and z(2));  f(2)<=(not w(2) and not x(2) and z(2))or(not w(2) and not x(2) and y(2)) or (not w(2) and y(2) and z(2))or(w(2) and x(2) and not y(2));  g(2)<=(not w(2) and not x(2) and not y(2))or (not w(2) and x(2) and y(2) and z(2));  end logic\_fun; |