Devansh Shah 1914078

15/04

ITC Tut - 8

Q) a) State table & state diagram:

states	
00	a
01	b
10	c
11	d

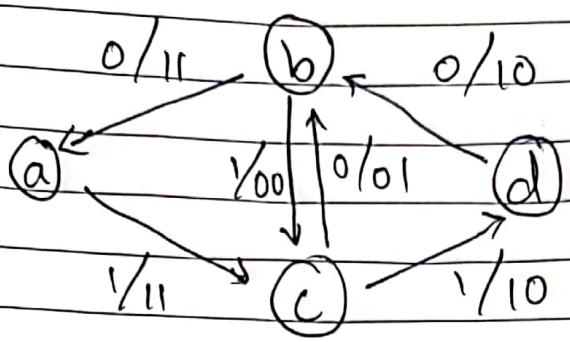
M_0 is the input
S_1 and S_2 are previous bits
V_1 and V_2 are the encoded output bits

$\therefore V_1 = m_0 \oplus S_2$
$V_2 = m_0 \oplus S_1 \oplus S_2$

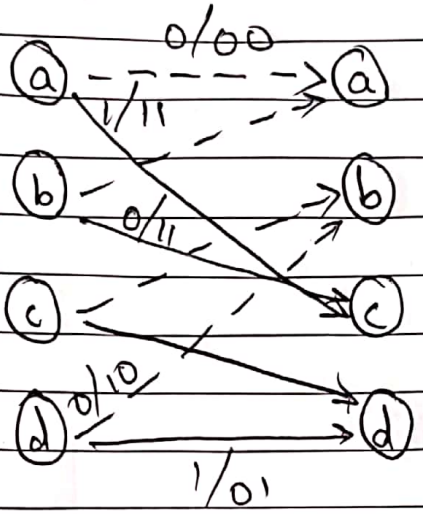
→ State table:

M_0	Previous state		Next state		Output	
	S_1	S_2	S_1	S_2	V_1	V_2
0	0	0	0	0	0	0
1	0	0	1	0	1	1
0	0	1	0	0	1	1
1	0	1	1	0	0	0
0	1	0	0	1	0	1
1	1	0	1	1	1	0
0	1	1	0	1	1	0
1	1	1	1	1	0	1

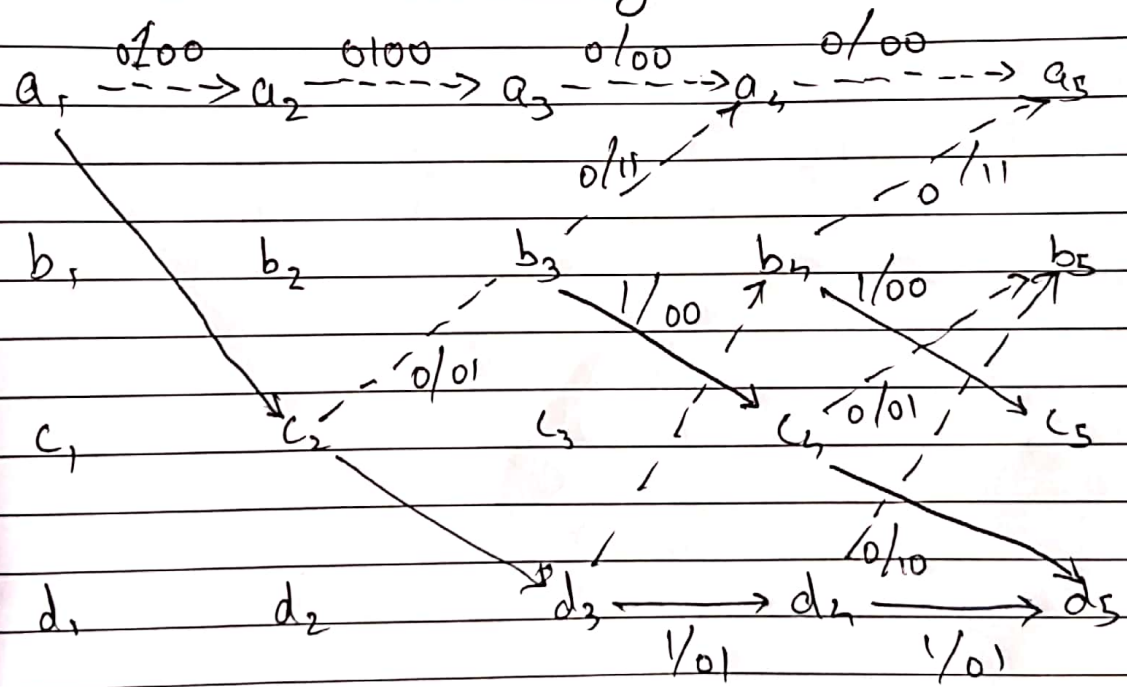
→ State diagram



b) Trellis diagram w.r.t state



c) [01 00 01 00] using viterbi algorithm



Decode message : 1101