Research & Vehicle Technology
"Infotainment Systems Product Development"

Feature – I2C over LVDS Communication Protocol for Camera

Version 1.0
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Revision History

Date	Ver	Notes	
June 2nd, 2017	1.0	Initial release	

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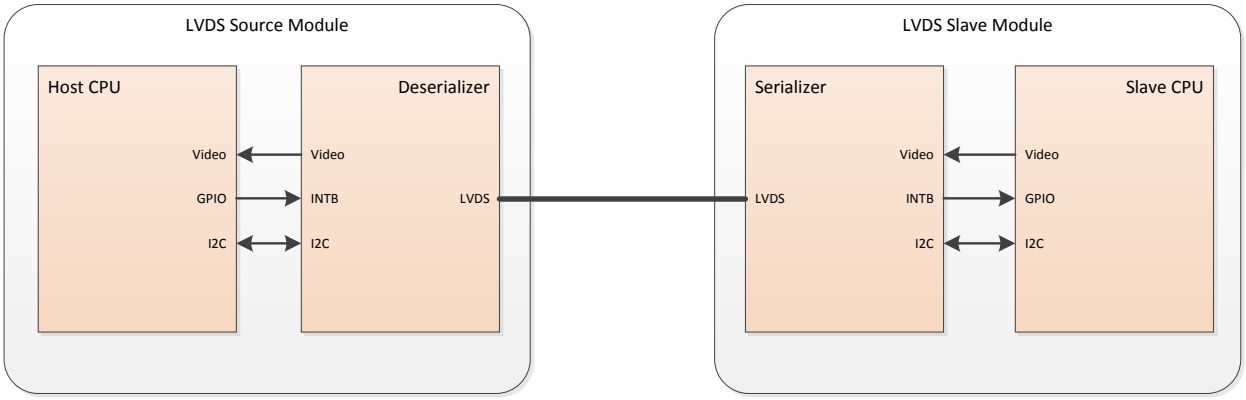
2.1 IFS-MMI2C-FUN-REQ-242752/A-I2C Interface Cameras/IPMB

2.1.1 IFS-MMI2C-SR-REQ-242928/A-System Overview Cameras/IPMB

The LVDS interface block diagram looks like:



The LVDS Source Module contains:

- Host CPU, which acts as an I^2C bus master
- LVDS Deserializer IC

The LVDS Slave Module contains:

- LVDS Serializer IC
- Microcontroller, which acts as an I^2C slave

2.1.2 IFS-MMI2C-SR-REQ-199141/B-Bus Frequency

The I^2C Master shall support a bus frequency of 400 kHz. All peripherals on the I^2C Slave shall support a bus frequency of 400 kHz.

The I^2C Master may configure the deserializer for, and operate at, any bitrate that meets overall system performance requirements. Refer to the TI user's guide for details on configuring the deserializer bitrate with "SCL High Time" and "SCL Low Time".

Note: Even if both sides use 400 kHz, the LVDS link has a lower effective-bitrate (~163 kHz) because each byte is buffered and regenerated. Refer to TI AN-2173 for a table of achievable net bitrates.

2.1.3 IFS-MMI2C-SR-REQ-199142/B-Slave Addresses

The following I^2C Slave addresses shall be used (7 bit format):

Device	Generation 1 Displays	Generation 2 Displays	Generation 2 Cameras
Serializer	0x15	0x15	0x5D
Deserializer	0x35	0x35	0x30
Touch Screen Controller (mXT641T)	---	0x4B	---
Touch Screen Controller (mXT449T)	---	0x4B	---

Touch Screen Controller (mXT1188S)	---	0x4A	---
Touch Screen Controller (mXT540E)	0x4D	---	---
Touch Screen Controller (CYAT81X)	---	0x24	---
Slave Microcontroller	0x70	0x71	0x5E

I^2C Slave shall not respond on any other slave address. All unspecified addresses are reserved for future expansion.

2.1.4 IFS-MMI2C-SR-REQ-199146/B-Clock Stretching

The I^2C Master shall support clock stretching as defined by the I^2C specification.

The I^2C Slave shall not stretch the clock for longer than 500 microseconds at a time.

2.1.5 IFS-MMI2C-SR-REQ-140554/C-Timer Settings

The timers described in this section shall have the following values:

Timer	Value
$t_{DISP\_EN(*1)}$	200ms
$t_{DISP\_DIS(*1)}$	200ms
t_{SHTDWN}	500ms
$t_{LVDSSlave\_RESET}$	1000ms

(*1) only valid in case of a display

- $t_{DISP\_EN(*1)}$: Maximum time to enable LCD Panel, LCD Backlight, and display an image on the LCD.
- $t_{DISP\_DIS(*1)}$: Maximum time to disable LCD Panel, LCD Backlight, and show a blank screen.
- t_{SHTDWN}: Maximum time to perform a controlled shutdown.

2.1.6 IFS-MMI2C-SR-REQ-199145/B-Time to Ready

All I^2C Slaves (e.g. TouchScreenController and display microcontroller) shall be capable of communicating on the I^2C bus 300ms after the filtered battery supply is enabled. Actual communication cannot begin until LOCK is achieved on the LVDS link between the LVDS Client and LVDS Source Module.

2.1.7 Diagnostics

This table summarizes the diagnostic requirements:

Requirement	DID	Byte	Bit	DTC	Name
REQ-197882	$FD1B	1	7	5001-02	Unexpected Reset
REQ-197881	$FD1B	1	6	5001-02	Reset Request
REQ-199371	$FD1B	1	5	5001-01	LVDS Link Fault
REQ-243376	-	-	-	5001-81	Loss of Lock
REQ-242770	-	-	-	5001-87	LostComm
REQ-258018	$FD1B	1	4	5001-01	General Electric Failure
REQ-258017	-	-	-	5001-4B	OverTemp
REQ-258019	-	-	-	5001-55	NoConfig

2.1.7.1 IFS-MMI2C-SR-REQ-197882/B-Unexpected Reset

Applicable: Gen2

The I^2C Slave module bit INIT is cleared (=0) at power-on, and set (=1) at I^2C Slave enable. Any transition from 1 -> 0 during normal operation indicates that I^2C Master Module was operating normally but:

1. The I^2C Slave was disconnected and same-or-different I^2C Slave was connected.

2. Or the I²C Slave reset, for example: low-voltage, watchdog, etc.

After a Gen2 I²C Slave is initialized, I²C Master Module shall monitor INIT and set DID Unexpected Reset if an unexpected reset was detected.

The I²C Master Module shall implement a counter and set DTC Unexpected Reset if there are greater than 5 events detected during any single ignition cycle.

2.1.7.2 IFS-MMI2C-SR-REQ-197881/B-Reset Request

Applicable: Gen1, Gen2

The I²C Slave module is permitted to set RST_RQ to request a full power-cycle. Gen1 I²C Slave s are known to make this request after detecting loss-of-lock, low-voltage dropout, and backlight fault. The I²C Slave shall only make this request if the fault can be fixed by cycling power.

The I²C Master Module shall monitor bit RST_RQ and set DID Reset Request: I²C Slave Micro Reset if a reset was requested.

The I²C Master Module shall implement a counter and set DTC Reset Request if there are greater than 5 reset requests during any single ignition cycle.

2.1.7.3 IFS-MMI2C-SR-REQ-199371/C-LVDS Link Detect Fault

Applicable: Gen1, Gen2

When the LVDS Source Module is providing power to the LVDS Slave Module, it shall monitor LVDS chip register “LINK Status“. If the LVDS Source Module detects an LVDS serial link fault it shall set DID “LVDS Link Fault”

The LVDS Source Module shall set DTC “LVDS Link Fault” based on this error. The diagnostic has detected a connection fault.

2.1.7.4 IFS-MMI2C-SR-REQ-243376/A-Loss of Lock

While enabled, the module containing the DES shall monitor the deserializer LOCK pin for any loss-of-lock and set DID “Loss of Lock” if the deserializer reports a loss-of-lock event.

It shall implement a counter and set DTC “Loss of Lock” if there are greater than 5 loss-of-lock events during any single ignition cycle. The diagnostic has detected a signal-quality problem with communication to the LVDS Slave Module.

2.1.7.5 IFS-MMI2C-SR-REQ-242770/A-Loss of Communication with I2C Slave Microcontroller

During normal operation, the I²C Master Module driver shall determine loss-of-communication by monitoring for persistent I²C NAK response.

If the I²C Master Module detects a condition where the LVDS link is operational but the I²C Slave microcontroller has a persistent NAK response (> 500ms), it shall set an Error: Lost Communication with I²C Slave Microprocessor.

The I²C Master Module shall set DTC LostComm for this error. The diagnostic has detected a failure inside the I²C Slave Module, and the recommended action is to replace the I²C Slave Module

2.1.7.6 IFS-MMI2C-SR-REQ-258017/A-Over Temperature

If the I2C Slave Module detects an over temperature condition it shall set related status.

If the I2C Master Module receives an over temperature it shall set DTC OverTemp for this error.

2.1.7.7 IFS-MMI2C-SR-REQ-258018/A-General Electric Failure

If the I2C Slave Module detects errors that result in a general electric failure condition it shall set related status.

If the I2C Master Module receives a general electric failure it shall set DTC General Electric Failure for this error.

2.1.7.8 IFS-MMI2C-SR-REQ-258019/A-No Configuration

If the I2C Slave Module detects errors that result in a no configuration condition it shall set related status.

If the I2C Master Module receives a general electric failure it shall set DTC NoConfig for this error.

2.1.8 Failure Mode Avoidance

2.1.8.1 IFS-MMI2C-SR-REQ-202030/B-Reset Request

The LVDS Slave module is permitted to set RST_RQ to request a full power-cycle. The LVDS Slave shall only make this request if the fault can be fixed by cycling power (e.g. Gen1 displays are known to make this request after detecting loss-of-lock, low-voltage dropout, and backlight fault).

The LVDS Source Module shall monitor bit RST_RQ. If bit RST_RQ=1, the LVDS Source Module shall perform a controlled power shutdown. After $t_{LVDSSlave\_RESET}$ expires the LVDS Source Module shall re-enable power to the LVDS Slave and perform a normal re-initialization sequence.

2.1.8.2 IFS-MMI2C-SR-REQ-202033/B-Loss of Communication

During normal operation, if the LVDS Source Module detects a condition where the LVDS Slave has become non-functional, either Link Detect Fault or Loss of Communication, it shall perform a full power-cycle as an attempt to recover the LVDS Slave.

The full power-cycle sequence is: disable power, wait $t_{LVDSSlave\_RESET}$, then perform a full re-initialization sequence.

2.1.8.3 IFS-MMI2C-SR-REQ-199134/B-Restart AEQ Algorithm

The LVDS chipset has an undocumented auto equalization (AEQ) behavior. When attempting to establish an LVDS link, the deserializer will begin with the minimum EQ setting and try to lock. If unsuccessful, it increments EQ and tries again. It repeats this routine until lock is established. Resetting the deserializer forces a restart at the beginning of the algorithm.

In any situation where deserializer is powered and running the search algorithm before the serializer is ready, the EQ setting could lock to a larger-than-necessary value.

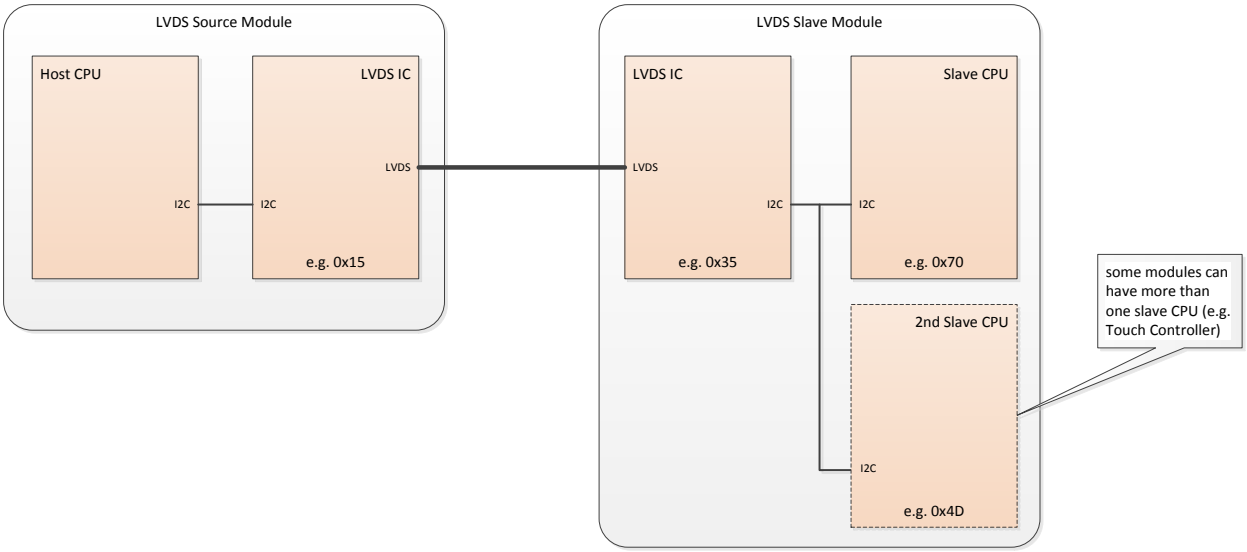
Therefore, the LVDS Source Module shall reset the deserializer:

- After resetting the serializer
- After changing LFMODE

2.1.8.4 IFS-MMI2C-SR-REQ-199348/B-Atomic Transaction

The LVDS chipset as an undocumented requirement regarding the sequence of I^2C messages across the LVDS link. Any transaction to the SER or DES must be performed in an “atomic” manner, because any I^2C message that flows across the link will overwrite the register offset.

For example:



The following sequences are permissible:

- Write offset to 0x15, read 0x15, write offset to 0x4D, read 0x4D
- Write offset to 0x4D, write offset to 0x70, read 0x4D, read 0x70

The following sequences are not permissible and result in **incorrect transactions**:

- Write offset to 0x15, write offset to 0x4D, **read 0x15**, read 0x4D
- Write offset to 0x35, write offset to 0x4D, **read 0x35**, read 0x4D

Note: All addresses mentioned in this requirement are just examples to be more descriptive.

2.2 IFS-MMI2C-FUN-REQ-242623/A-Generation 2 Camera/IPMB Modules

2.2.1 Periodicity

In this design, multiple functions within the I^2C Slave need to send data to the I^2C Master module some others needs to be updated periodic.

Since the I^2C Slave is not allowed to send any data unrequested, the I^2C Master needs to poll some registers like e.g. Status register. Polling rate and which ones are defined in extra requirements.

Some others need to be sent by the I^2C Master in a periodic manner to keep the I^2C Slave updated with actual values. Periodic rate and which ones are defined in extra requirements.

2.2.1.1 IFS-MMI2C-SR-REQ-243371/A-Camera Status polling

Register defined in REQ-242534 (0x00 Camera Status) shall be polled by the I^2C Master at a periodic rate of at least 1000ms.

2.2.1.2 IFS-MMI2C-SR-REQ-243372/A-Current Displayed View polling

Register defined in REQ-242111 (0x10 Current Displayed View) shall be polled by the I^2C Master at a periodic rate of at least 1000ms.

2.2.1.3 IFS-MMI2C-SR-REQ-243373/A-Vehicle Steering Angle periodicity

Register defined in REQ-242281 (0x11 Vehicle Steering Angle) shall be sent by the I^2C Master at a periodic rate of at least 160ms.

2.2.2 IFS-MMI2C-SR-REQ-242751/A-Loss of Lock

The module containing the DES shall monitor the deserializer LOCK pin for any loss-of-lock:

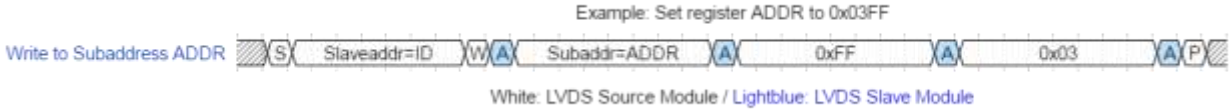
- Automatically turn-off showing video signal to prevent showing bad video.
- Latch that a loss-of-lock was detected.
- If lock is regained, consider the commanded settings and determine if the video signal need to be automatically turned back on.

This strategy allows the system to recover quickly and automatically from a momentary loss-of-lock, without a full power-cycle. It also allows the LVDS Source Module to distinguish between signal-quality problems and a fault that requires full reset.

2.2.3 I2C Bus Interface

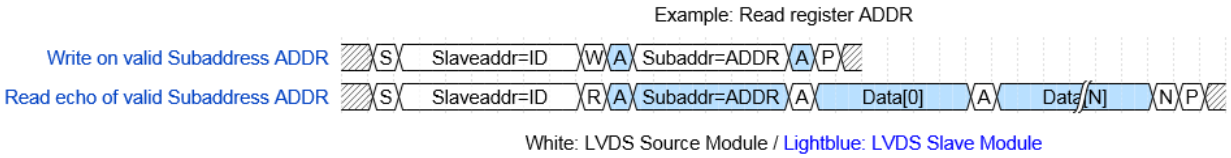
2.2.3.1 IFS-MMI2C-SR-REQ-140564/C-Write to Subaddress

This diagram shows a typical write by the I^2C Master. Writes are implemented by writing the subaddress then one-or-more bytes of data:



2.2.3.2 IFS-MMI2C-SR-REQ-140561/C-Read from Subaddress

This diagram shows a typical read by the I^2C Master. Reads are implemented by writing the subaddress, then reading an echo of the subaddress followed-by the data:

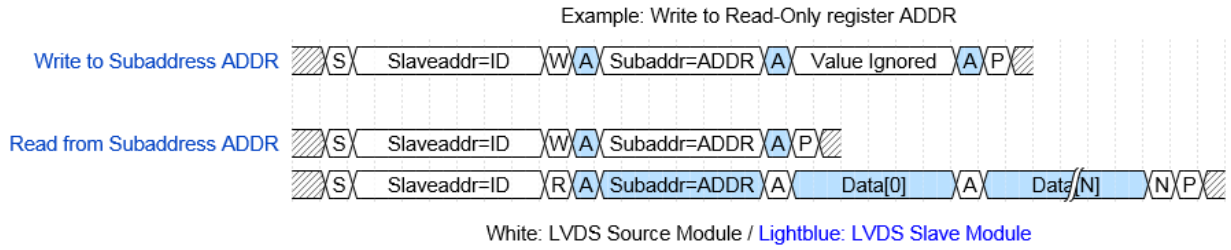


I^2C Slave is not required to support I^2C repeated-start bus cycle. The I^2C Master shall not use an I^2C repeated-start bus cycle to communicate with the I^2C Slave microcontroller.

2.2.3.3 IFS-MMI2C-SR-REQ-197857/B-Write to Read-Only Subaddress

If I^2C Master Module attempts to write to a read-only subaddress, the I^2C Slave shall send ACK to indicate the bytes are received but make no state-change.

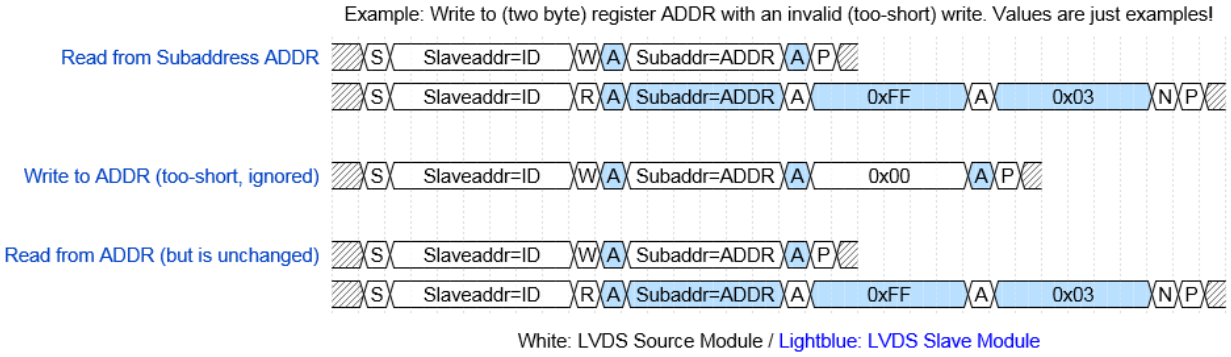
As an example with subaddress ADDR that will be read-only. This diagram shows that the I^2C Slave ignores an attempt to write to the subaddress:



2.2.3.4 IFS-MMI2C-SR-REQ-140569/C-Write Underflow

If the I^2C Master writes too-few bytes, the I^2C Slave shall make no state-change.

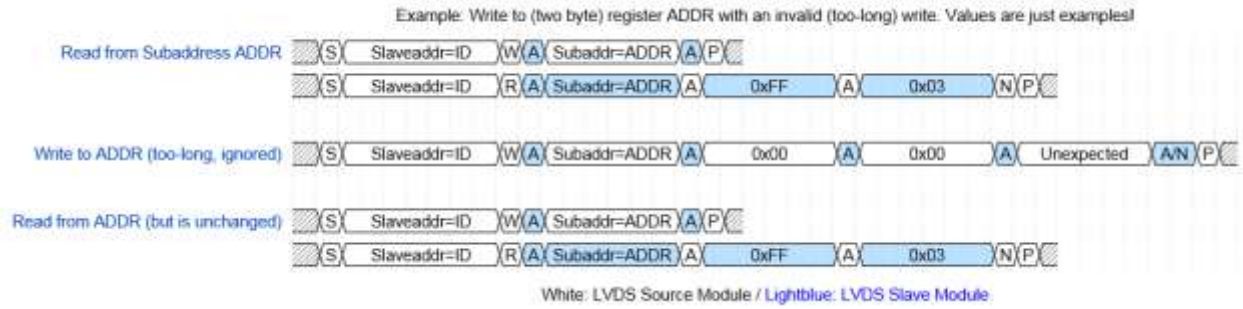
As an example with subaddress ADDR that will accept exactly two bytes of data. This diagram shows I^2C Master attempting to write only one byte of data, and the I^2C Slave making no state-change:



2.2.3.5 IFS-MMI2C-SR-REQ-140570/C-Write Overflow

If the I^2C Master attempts to write too-many bytes, the I^2C Slave shall continue sending ACK to indicate the bytes are received, and make no state-change.

As an example with subaddress ADDR that will accept exactly two bytes of data. This diagram shows I^2C Master attempting to write three bytes, and the I^2C Slave making no state-change:



2.2.3.6 IFS-MMI2C-SR-REQ-197875/B-Read from Subaddress Beyond Defined Length

If I^{2}C Master continues reading beyond the defined data-length of a subaddress, I^{2}C Slave shall leave SDA undriven resulting in Data = 0xFF.

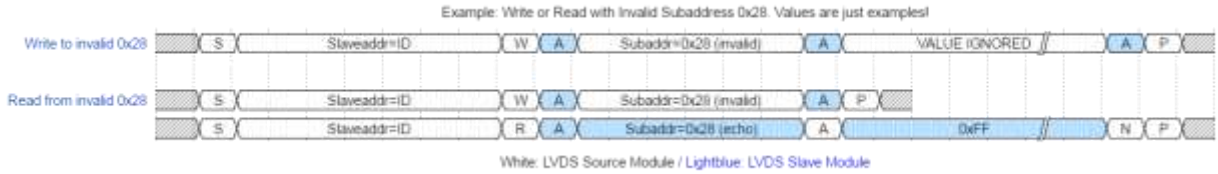
2.2.3.7 IFS-MMI2C-SR-REQ-140565/C-Undefined / Unsupported Subaddress

If the I^{2}C Master attempts to write to an undefined subaddress, the I^{2}C Slave shall:

- ACK to indicate the byte was received
- Update the internal subaddress register (for echo purposes)
- Take no other action because the request was unrecognized.

If I^{2}C Master attempts to read from an undefined subaddress, the I^{2}C Slave shall leave SDA undriven resulting in Data = 0xFF.

For example, subaddress 0x28 is undefined. This diagram shows the I^{2}C Master attempting to write to, and read from, the undefined subaddress:



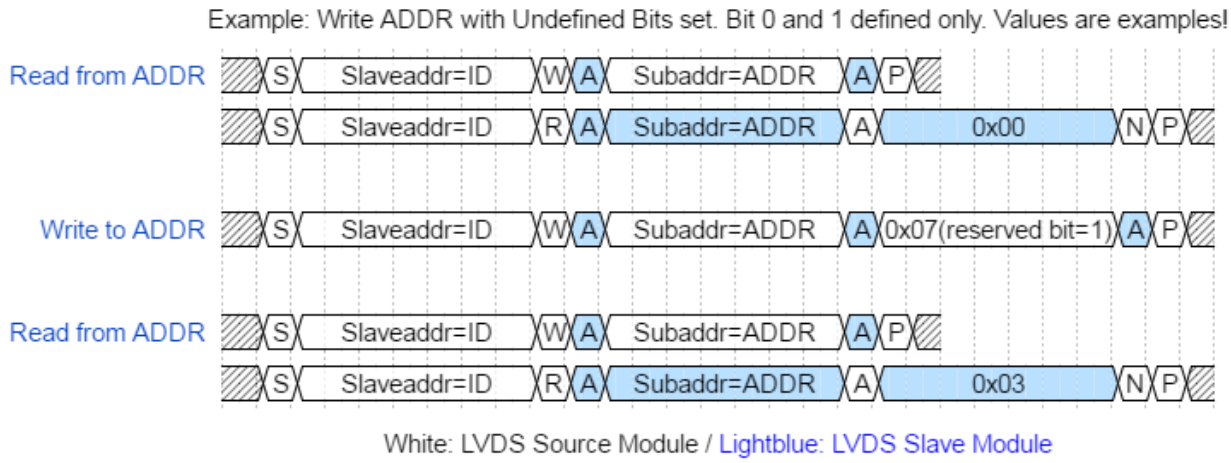
2.2.3.8 IFS-MMI2C-SR-REQ-140611/C-Reserved Bits

I^{2}C Slave shall respond with “reserved” bits equal to zero.

2.2.3.9 IFS-MMI2C-SR-REQ-140566/C-Reserved Bits

If I^{2}C Master writes to a subaddress and any reserved bit is set, the I^{2}C Slave shall treat the reserved bit as “don’t care” and shall act upon the defined bits.

As an example with subaddress ADDR that has several undefined bits. This diagram shows the I^{2}C Slave changing value from 0x00 to 0x03, and ignoring a reserved bit:



2.2.4 I2C Messages

0x00	R	Camera Status
0x10	R	Current Displayed View
0x11	R/W	Vehicle Steering Angle
0x12	R/W	Overlay Request
0x13	R/W	View Request
0x14	R/W	Configuration Data
0x31	R	Core Assembly
0x32	R	Delivery Assembly
0x33	R	Software Ford Part Number
0x34	R	Serial Number
0x35	R	Main Calibration Ford Part Number
0xB0-0xFF	R/W	Reserved for Supplier

2.2.4.1 IFS-MMI2C-SR-REQ-242534/A-0x00 Camera Status

The Camera Status message provides a mechanism to transmit general camera related status's back to the I^2C Master.

Subaddress: 0x00
Access: Read-Only
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	-	-	-	**RST_RQ**	**GELECFAIL**	**OVRTMP**	**NOCONF**	**INIT**

- RST_RQ: Reset Request
  This bit defaults clear and is set when there has been detected an unrecoverable fault and a full power-cycle reset is required to resolve some problem.
  0 Normal operation
  1 Request is requested
- GELECFAIL: General Electric failure (latched)
  This bit defaults clear and reports latched status if an internal failure has been detected (e.g. flash is corrupt).
  0 No Fault
  1 Fault
- OVRTMP: Over temperature
  This bit defaults clear and is set if the camera has shut down due to an over temperature condition.
  0 Inactive
  1 Active
- NOCONF: No Configuration
  This bit defaults clear and is set if there is no valid configuration written.
  0 No Fault
  1 Fault
- INIT: Camera Initialized
  This bit defaults clear, and is set after the camera has been enabled.
  0 Camera has not been enabled during this power-cycle.
  1 Camera has been enabled at least once during this power-cycle.
  This bit is used by the host to detect an unexpected reset. Any transition from 1 -> 0 during normal operation indicates that the camera may need a complete re-initialization.

Several bits in this I^2C message have latched behavior, allowing the camera to inform the host of a momentary event. The camera microcontroller shall latch any value change until this subaddress is read by the host, then re-evaluate the current state.

Note: See REQ-243371 for possible polling rate.

2.2.4.2 IFS-MMI2C-SR-REQ-242111/A-0x10 Current Displayed View

This signal is used to synchronize the current displayed view.

Subaddress: 0x10
Access: Read-Only
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	-	-	-	-	reserved	reserved	CurDispView [1:0]	

Logical Value	Encoded Value	Usage/Meaning
Off	0x00	Image Off
Normal	0x01	Normal View
Zoom	0x02	Zoom View
Split	0x03	Split View

Note: See REQ-243372 for possible polling rate.

2.2.4.3 IFS-MMI2C-SR-REQ-242281/A-0x11 Vehicle Steering Angle

The steering angle is used to select the dynamic overlay that corresponds to the path of intended motion.

Subaddress: 0x11
Access: Read-Write
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	SteAngle [7:0]							
[1]	-	SteAngle [8:15]						

Encoded Value	Logical Value	Usage/Meaning
[0x00 – 0x7FFF]	Angle	0.1*value – 1600 to yield angle

Note: See REQ-243373 for possible polling rate.

2.2.4.4 IFS-MMI2C-SR-REQ-242110/A-0x12 Overlay Request

This signal determines which type of overlay is displayed in the view.

Subaddress: 0x12
Access: Read-Write
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	-	-	-	-	reserved	reserved	OvrlsRq [1:0]	

Encoded Value	Logical Value	Usage/Meaning
0x00	Inactive	Overlays inactive
0x01	Static	Static Overlays Active
0x02	Dynamic	Static and dynamic Overlays are Active
0x03	Not Used	Unused Value

2.2.4.5 IFS-MMI2C-SR-REQ-242283/A-0x13 View Request

This signal is used to change the View.

Subaddress: 0x13
Access: Read-Write
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	-	-	-	-	reserved	reserved	ViewRq [1:0]	

Encoded Value	Logical Value	Usage/Meaning
0x00	Off	Turn off
0x01	Normal	Put in Normal view
0x02	Zoom	Put in Zoom View
0x03	Split	Put in Split View

2.2.4.6 IFS-MMI2C-SR-REQ-242284/A-0x14 Configuration Data

This signal is used to transfer configuration data.

Subaddress: 0x14
Access: Read-Write
Default Value: 0x02

	7	6	5	4	3	2	1	0
[0]	-	**OvlSet [6:1]**						**DynAvl**

- DynAvl: Dynamic Available.
  0 Vehicle configuration does not support dynamic guidelines.
  1 Vehicle configuration does support dynamic guidelines.

- OvlSet: Overlay Set.

Logical Value	Usage/Meaning
0x00	Overlay Set 1
0x01	Overlay Set 2
0x02	Overlay Set 3
0x03	Overlay Set 4
0x04	Overlay Set 5
0x05	Overlay Set 6
0x06	Overlay Set 7
0x07	Overlay Set 8
0x08	Overlay Set 9
0x09	Overlay Set 10
0x0A	Overlay Set 11
0x0B	Overlay Set 12
0x0C	Overlay Set 13
0x0D	Overlay Set 14
0x0E	Overlay Set 15
0x0F	Overlay Set 16
0x10	Overlay Set 17
0x11	Overlay Set 18
0x12	Overlay Set 19
0x13	Overlay Set 20
0x14	Overlay Set 21
0x15	Overlay Set 22
0x16	Overlay Set 23
0x17	Overlay Set 24
0x18	Overlay Set 25
0x19	Overlay Set 26
0x1A	Overlay Set 27
0x1B	Overlay Set 28
0x1C	Overlay Set 29
0x1D	Overlay Set 30
0x1E	Overlay Set 31
0x1F	Overlay Set 32
0x20	Overlay Set 33
0x21	Overlay Set 34
0x22	Overlay Set 35

0x23	Overlay Set 36
0x24	Overlay Set 37
0x25	Overlay Set 38
0x26	Overlay Set 39
0x27	Overlay Set 40
0x28	Overlay Set 41
0x29	Overlay Set 42
0x2A	Overlay Set 43
0x2B	Overlay Set 44
0x2C	Overlay Set 45
0x2D	Overlay Set 46
0x2E	Overlay Set 47
0x2F	Overlay Set 48
0x30	Overlay Set 49
0x31	Overlay Set 50
0x32	Overlay Set 51
0x33	Overlay Set 52
0x34	Overlay Set 53
0x35	Overlay Set 54
0x36	Overlay Set 55
0x37	Overlay Set 56
0x38	Overlay Set 57
0x39	Overlay Set 58
0x3A	Overlay Set 59
0x3B	Overlay Set 60
0x3C	Overlay Set 61
0x3D	Overlay Set 62
0x3E	Overlay Set 63
0x3F	Overlay Set 64

2.2.4.7 IFS-MMI2C-SR-REQ-140624/C-0x31 Core Assembly FPN

The I^{2}C Slave Core Assembly message provides a mechanism to transmit a Ford Part Number back to the I^{2}C Master.

Subaddress: 0x31
Access: Read-Only
Default: n/a

	7	6	5	4	3	2	1	0
[0]	Core Assembly character[0]							
…	…							
[24]	Core Assembly character[24]							

- Core Assembly: Released (or prototype) Ford Part Number
  Null-terminated string. For example “H1BT-14F180-FA”.
  Maximum length 24 characters plus NULL.

The I^{2}C Master shall read a maximum of 25 bytes, be robust to receiving non-ASCII bytes, and be robust to receiving non-NULL terminated data.

If the I2C Slave is not released with this kind of Ford Part Number, the I^{2}C Slave shall indicate that the subaddress is unsupported as described in REQ-140565. In this case the I^{2}C Slave would leave SDA undriven resulting in Data = 0xFF.

2.2.4.8 IFS-MMI2C-SR-REQ-140625/C-0x32 Delivery Assembly FPN

The Delivery Assembly message provides a mechanism to transmit a Ford Part Number back to the I²C Master.

Subaddress: 0x32
Access: Read-Only
Default: n/a

	7	6	5	4	3	2	1	0
[0]	Delivery Assembly FPN character[0]							
…	…							
[24]	Delivery Assembly FPN character[24]							

- Delivery Assembly FPN: Released (or prototype) Ford Part Number
  Null-terminated string. . For example “H1BT-18B955-FA”
  Maximum length 24 characters plus NULL.

The I²C Master shall read a maximum of 25 bytes, be robust to receiving non-ASCII bytes, and be robust to receiving non-NULL terminated data.

If the I²C Slave is not released with this kind of Ford Part Number, the I²C Slave shall indicate that the subaddress is unsupported as described in REQ-140565. In this case the I²C Slave would leave SDA undriven resulting in Data = 0xFF.

2.2.4.9 IFS-MMI2C-SR-REQ-140626/C-0x33 Software FPN

The Software Part Number message provides a mechanism to transmit a Ford Part Number back to the I²C Master.

Subaddress: 0x33
Access: Read-Only
Default: n/a

	7	6	5	4	3	2	1	0
[0]	Software FPN character[0]							
…	…							
[24]	Software FPN character[24]							

- Software FPN: Released (or prototype) Ford Part Number
  Null-terminated string. For example “H1BT-14D358-FA”
  Maximum length 24 characters plus NULL.

The I²C Master shall read a maximum of 25 bytes, be robust to receiving non-ASCII bytes, and be robust to receiving non-NULL terminated data.

If the I²C Slave is not released with this kind of Ford Part Number, the I²C Slave shall indicate that the subaddress is unsupported as described in REQ-140565. In this case the I²C Slave would leave SDA undriven resulting in Data = 0xFF.

2.2.4.10 IFS-MMI2C-SR-REQ-140627/C-0x34 Serial Number

The Serial Number message provides a mechanism to transmit an electronic serial number back to the I²C Master.

Subaddress: 0x34
Access: Read-Only
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	Serial Number character[0]							

…	…
[25]	Serial Number character[25]

- Serial Number:
  Null-terminated string.
  Maximum length 24 characters plus NULL.

Note: This specification contains no functional requirement about the format of the serial number.

The I^2C Master shall read a maximum of 25 bytes, be robust to receiving non-ASCII bytes, and be robust to receiving non-NULL terminated data.

If the I^2C Slave contains no serial number, the I^2C Slave shall indicate that the subaddress is unsupported as described in REQ-140565. In this case the I^2C Slave would leave SDA undriven resulting in Data = 0xFF.

2.2.4.11 IFS-MMI2C-SR-REQ-140628/C-0x35 Main Calibration Data FPN

The Main Calibration Data message provides a mechanism to transmit a Ford Part Number back to the I^2C Master.

Subaddress: 0x35
Access: Read-Only
Default Value: n/a

	7	6	5	4	3	2	1	0
[0]	Main Calibration Data FPN character[0]							
…	…							
[24]	Main Calibration Data FPN character[24]							

- Main Calibration Data FPN: Released (or prototype) Ford Part Number
  Null-terminated string. No example provided.
  Maximum length 24 characters plus NULL.

The I^2C Master shall read a maximum of 25 bytes, be robust to receiving non-ASCII bytes, and be robust to receiving non-NULL terminated data.

If the I^2C Slave is not released with this kind of Ford Part Number, the I^2C Slave shall indicate that the subaddress is unsupported as described in REQ-140565. In this case the I^2C Slave would leave SDA undriven resulting in Data = 0xFF.

2.2.4.12 IFS-MMI2C-SR-REQ-140629/B-I2C Reserved Subaddresses

The read and write messages at subaddress 0xB0-0xFF shall be reserved for internal supplier uses.

3 Appendix A: Definitions / Acronyms

DES – LVDS Deserializer
DM – Display Module
DTC – Diagnostic Trouble Code
ESN – Electronic Serial Number
FPC – Flexible Printed Circuit
FPN – Ford Part Number
Gen2 Cameras – e.g. Digital Rear View Camera
IPMB – Image Processing Module B, Rear View Camera
ISR – Interrupt Status Register
SDM – Slim Display Module
SER – LVDS Serializer
TSC – Touch Screen Controller

4 Appendix B: Reference Documents

Reference #	Document Title
1	Bezel Diagnostics SPSS
2	Digital Camera Functional Specification
3	NXP UM102104, I2C-bus specification and user manual
4	TI AN-2173 I2C Communication Over FPD-Link III with Bidirectional Control Channel (Application Note)
5	TI SNLS546 DS90UB933 (User's Guide)
6	TI DS90UB936 (User's Guide)

The requirements of the documents listed in the reference table above, of the latest revision level, form a part of this Engineering Specification