

Tsung-Wun Wang (王琮文)

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Education

National Yang Ming Chiao Tung University, Hsinchu, Taiwan

Completeness of Electronics and AI Training Program (230 hours) Sep. 2025 – Nov. 2025

- Relevant Coursework: Digital Design with FPGA, Electronic Circuit Design, Microelectronics Labs

National Taiwan University, Taipei, Taiwan

Master of Science in Mechanical Engineering (Overall GPA: 4.0/4.3) Mar. 2021 – Aug. 2023

- Thesis Title: Development of 3D Reconstruction and Navigation for Mobile Robots
- Relevant Coursework: Advanced Computer Vision, 3D Computer Vision with Deep Learning Applications, Operating Systems, Adaptive Signal Processing, System Identification

Bachelor of Science in Mechanical Engineering (Overall GPA: 3.7/4.3) Sep. 2016 – Jun. 2020

- Relevant Coursework: Robot Vision, Introduction to Robotics, Machine Learning

Professional Experience

Vecow Co., Ltd., Taipei, Taiwan

Engineer Oct. 2023 – Sep. 2025

- Brought up MIPI/CSI-2 and configured video pipeline IP in Vivado on Zynq UltraScale+ MPSoC.
- Validated signals and formats (video_out_tuser, YUV422 8-bit) using ILA and oscilloscope.
- Implemented multi-camera control over I2C in Vitis to deliver streams from MIPI sensors.
- Automated Vivado design flows with Tcl to create reproducible builds and shorten team iteration cycles.
- Ported ROS2 Humble EKF localization and gPTP time sync into PetaLinux using a meta-ros layer.
- Implemented Python test automation to reduce regression time and accelerate releases.
- Configured device tree bindings and produced Debian 11 builds for rapid, standardized deployment.

Aeroprobing Inc., Taipei, Taiwan

Firmware Engineering Intern Jun. 2021 – Aug. 2022

- Implemented FreeRTOS to synchronize multiple tasks in drone control systems.
- Managed sensor modules using SPI, I2C, and UART protocols on STM32 microcontrollers.
- Applied extended Kalman filter for sensor fusion, estimating drone orientation, altitude, and position.
- Designed and fine-tuned PID control loops for precise flight control.

Course Projects

Real-time FPGA Edge Detection Pipeline on Basys 3 Dec. 2025

- Designed video pipeline with frame buffer read/write, synchronized HS/VS, and pixel clock handling.

Circuit Simulation of A 4-bit Synchronous Up-counter in LTspice/ModelSim/XSim Nov. 2025

- Implemented J-K flip-flop timing and an R-2R D/A converter to visualize state transitions in LTspice.

Skills & Certificates

- **Programming:** C/C++, Python, VHDL, HTML/CSS, LaTeX
- **Embedded Systems Tools:** Quartus, Vivado, Petalinux, Vitis, STM32, FreeRTOS, Git
- **Design & Simulation:** ModelSim, LTspice, Matlab (Simulink), AutoCAD, Solidworks, PTC Creo
- **Certification:** Robotics Engineer (Taiwan Automation Intelligence and Robotics Association, No. 2017-3-0034)
- **Coursera Courses:** VLSI CAD, FPGA Computing Systems, Computer & Peripheral Hardware

Publications

- Tsung-Wun Wang, Han-Pang Huang, Yu-Lin Zhao. Vision-Guided Autonomous Robot Navigation in Realistic 3D Dynamic Scenarios. *Applied Sciences*. 2025; 15(5):2323. <https://doi.org/10.3390/app15052323>
- Tsung-Wun Wang, Han-Pang Huang, Yu-Lin Zhao, and Cheng-Chi Lee, "Search-based Path Replanning for Autonomous Navigation and Obstacle Avoidance," Best Student Paper Award, in *Proc. of the 21th International Conference on Automation Technology*, Taipei, Taiwan, Nov. 2024.
- Tsung-Wun Wang, Han-Pang Huang, Chiou-Shann Fuh, "Improved Real-Time Dense ORB SLAM with GPU Implementation," in *Proc. of the 36th IPPR Conference on Computer Vision, Graphics, and Image Processing*, Kinmen, Taiwan, Aug. 2023.