Tsung-Wun Wang（王琮文）

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Summary

Designed Verilog/VHDL FPGA systems on Zynq/Artix/UltraScale+; Vivado/Quartus flows; hardware verification and board bring-up; demo-ready projects with testbenches (ModelSim/XSim); Python/Tcl test automation.

Professional Experience

Vecow Co., Ltd., Taipei, Taiwan
Engineer *Oct. 2023 – Sep. 2025*

- Brought up MIPI/CSI-2 and configured video pipeline IP in Vivado on Zynq UltraScale+ MPSoC.
- Controls multiple cameras via I2C in Vitis and validated video (AXI-S tuser, YUV422) using ILA.
- Automated Vivado design flows with Tcl to create reproducible builds and shorten team iteration cycles.
- Automated project setup with Tcl to enable repeatable hardware (Vivado) builds and CI-friendly workflows.
- Ported ROS2 Humble EKF localization and gPTP time sync into PetaLinux using a meta-ros layer.
- Implemented Python test automation to reduce regression time and accelerate releases.
- Configured device tree bindings and produced Debian 11 builds for rapid, standardized deployment.

Aeroprobing Inc., Taipei, Taiwan
Firmware Engineering Intern *Jun. 2021 – Aug. 2022*

- Implemented FreeRTOS to synchronize multiple tasks in drone control systems.
- Managed sensor modules using SPI, I2C, and UART protocols on STM32 microcontrollers.
- Applied extended Kalman filter (EKF) for sensor fusion, estimating drone orientation, altitude, and position.

Training & Education

National Yang Ming Chiao Tung University, Hsinchu, Taiwan
Completeness of Electronics and AI Training Program (230 hours) *Sep. 2025 – Nov. 2025*

- Relevant Coursework: Digital Design with FPGA, Electronic Circuit Design, Microelectronics Labs

National Taiwan University, Taipei, Taiwan
Master of Science in Mechanical Engineering *Mar. 2021 – Aug. 2023*

- Thesis Title: Development of 3D Reconstruction and Navigation for Mobile Robots

Bachelor of Science in Mechanical Engineering *Sep. 2016 – Jun. 2020*

Course Projects

Real-time FPGA Edge Detection Pipeline on Basys 3 *Dec. 2025*

- Designed video pipeline with frame buffer read/write, synchronized HS/VS, and pixel clock handling.
- Established SCCB camera control and integrated OV7670 capture with VGA timing for video display.

Circuit Simulation of A 4-bit Synchronous Up-counter in LTspice/ModelSim/XSim *Nov. 2025*

- Designed J-K flip-flop timing and an R-2R D/A converter to visualize state transitions in LTspice.
- Validated designs with ModelSim/XSim testbenches and debounce the button on Altera DE2.

Skills

- **Embedded Systems Tools**: Quartus, Vivado, Petalinux, Vitis, STM32, FreeRTOS, Git
- **Design & Simulation**: ModelSim, LTspice, Matlab (Simulink), AutoCAD, Solidworks, PTC Creo
- **Programming**: C/C++, Python, Verilog/VHDL, HTML/CSS, LaTeX

Publications

- Tsung-Wun Wang, Han-Pang Huang, Yu-Lin Zhao. Vision-Guided Autonomous Robot Navigation in Realistic 3D Dynamic Scenarios. Applied Sciences. 2025; 15(5):2323. https://doi.org/10.3390/app15052323
- Tsung-Wun Wang, Han-Pang Huang, Yu-Lin Zhao, and Cheng-Chi Lee, "Search-based Path Replanning for Autonomous Navigation and Obstacle Avoidance," Best Student Paper Award, in *Proc. of the 21th International Conference on Automation Technology*, Taipei, Taiwan, Nov. 2024.
- Tsung-Wun Wang, Han-Pang Huang, Chiou-Shann Fuh, "Improved Real-Time Dense ORB SLAM with GPU Implementation," in *Proc. of the 36th IPPR Conference on Computer Vision, Graphics, and Image Processing*, Kinmen, Taiwan, Aug. 2023.