Logic Design

EECS101001

Lab 1: Fibonacci Detector – Report

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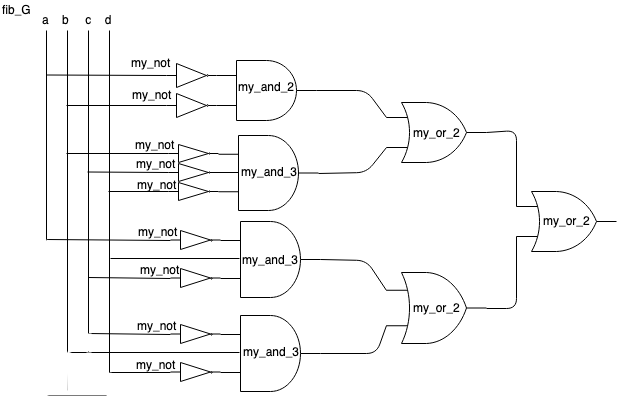
1. K-Map

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自動產生的描述

In the K-Map the input abcd was storing in array {in[3], in[2], in[1], in[0]}. Since we consider the Hazard-Free, we need to add OR gate to .

1. Graph

* Schematic Graph

my\_not GATE, my\_and\_2 GATE, my\_and\_3 GATE, my\_or\_2 GATE will describe later on.

* Truth Table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Dec | **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 0 |
| 10 | 1 | 0 | 1 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | 0 |
| 12 | 1 | 1 | 0 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 | 1 |
| 14 | 1 | 1 | 1 | 0 | 0 |
| 15 | 1 | 1 | 1 | 1 | 0 |

* GATE Description

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自動產生的描述

-Explanation-

Module fib\_G is start with parameter n = 4, since we just consider 0~15 in decimal. Then we describe the circuit using my own gate which is implemented by **NAND** gate.

* Data Flow Description

( !in[3] & !in[2] ) |

( !in[2] & !in[1] & !in[0] ) |

( !in[3] & !in[1] & in[0] ) |

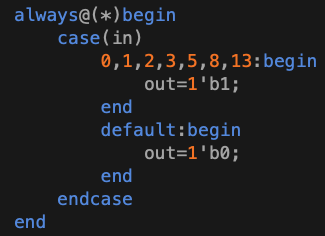
( in[2] & !in[1] & in[0] )

-Explanation-

4-bit input and 1-bit output, if input is 0, 1, 2, 3, 5, 8, or 13 (Fibonacci Number) output should be 1, otherwise, output should be 0.

So we got the Behavior Description below…

* Behavior Description



1. Implementation Details

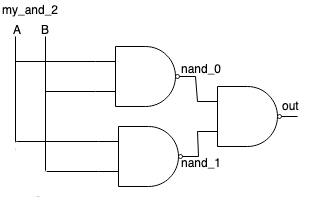
Since Lab1 can only use **NAND** Gate to implement **AND, OR, NOT** GATE, I implement some GATE for me.

* AND GATE for 2-inputs

∵ A · B =[(A·B)’]’

=[(A·B)’·(A·B)’]’

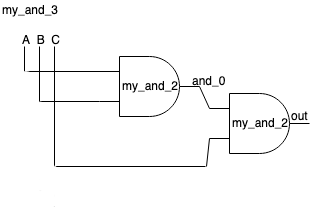
Hence, we can use **NAND** GATE to get **my\_and\_2** GATE.

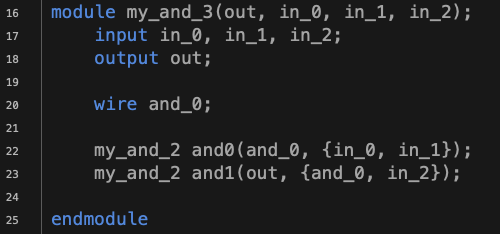


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For 3-inputs **AND GATE** is easy deriving from **my\_and\_2** GATE.



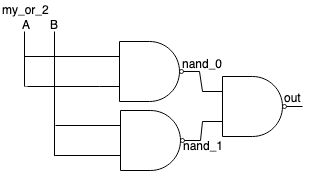
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* OR GATE for 2-inputs

∵ A + B =[(A+B)’]’

=[(A·A)’·(B·B)’]’

Hence

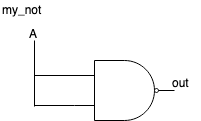




* NOT GATE

∵ A’ =(A·A)’

Hence





1. Simulation Result

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自動產生的描述

1. Encountered Problems and Solving

* It’s my very first time writing VERILOG, there are a lot of unfamiliar things. The first problem I got is how to compile a Verilog program. But I solved it later on.
* Only can using NAND GATE is a little bit challenging, but only need some Law from Boolean algebra can easily implement the GATE needed.
* The “parameter” in module. The first time I saw it I had no idea what it is, and then I saw something like *input [n-1:0]in* , *in[3]* , *in[2]* , … I thought maybe its mean the input may be an array. Therefore, I try to use in my GATE *my\_and\_2*.
* Finally, when I almost finish and get this error

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I just put my function’s parameter in wrong order. So when input isn’t array will get this error.

* It’s really good opening in Verilog, hoping that I will keep enjoy in this class. Thanks to all TAs and Professor!!