Logic Design

EECS101001

Lab 2: Applications of Multiplexer – Report

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1. K-Map
2. Graph
3. Implementation Details
4. Simulation Result
5. Encountered Problems and Solving

* It’s my very first time writing VERILOG, there are a lot of unfamiliar things. The first problem I got is how to compile a Verilog program. But I solved it later on.
* Only can using NAND GATE is a little bit challenging, but only need some Law from Boolean algebra can easily implement the GATE needed.
* The “parameter” in module. The first time I saw it I had no idea what it is, and then I saw something like *input [n-1:0]in* , *in[3]* , *in[2]* , … I thought maybe its mean the input may be an array. Therefore, I try to use in my GATE *my\_and\_2*.
* Finally, when I almost finish and get this error

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自動產生的描述

I just put my function’s parameter in wrong order. So when input isn’t array will get this error.

* It’s really good opening in Verilog, hoping that I will keep enjoy in this class. Thanks to all TAs and Professor!!