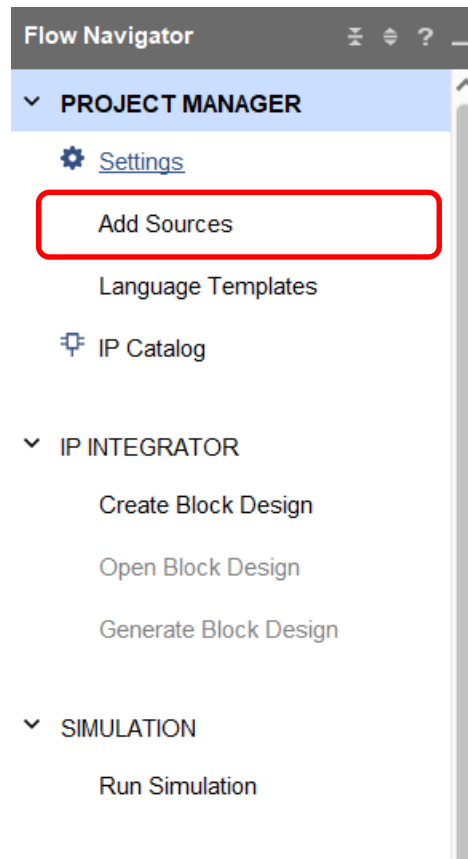


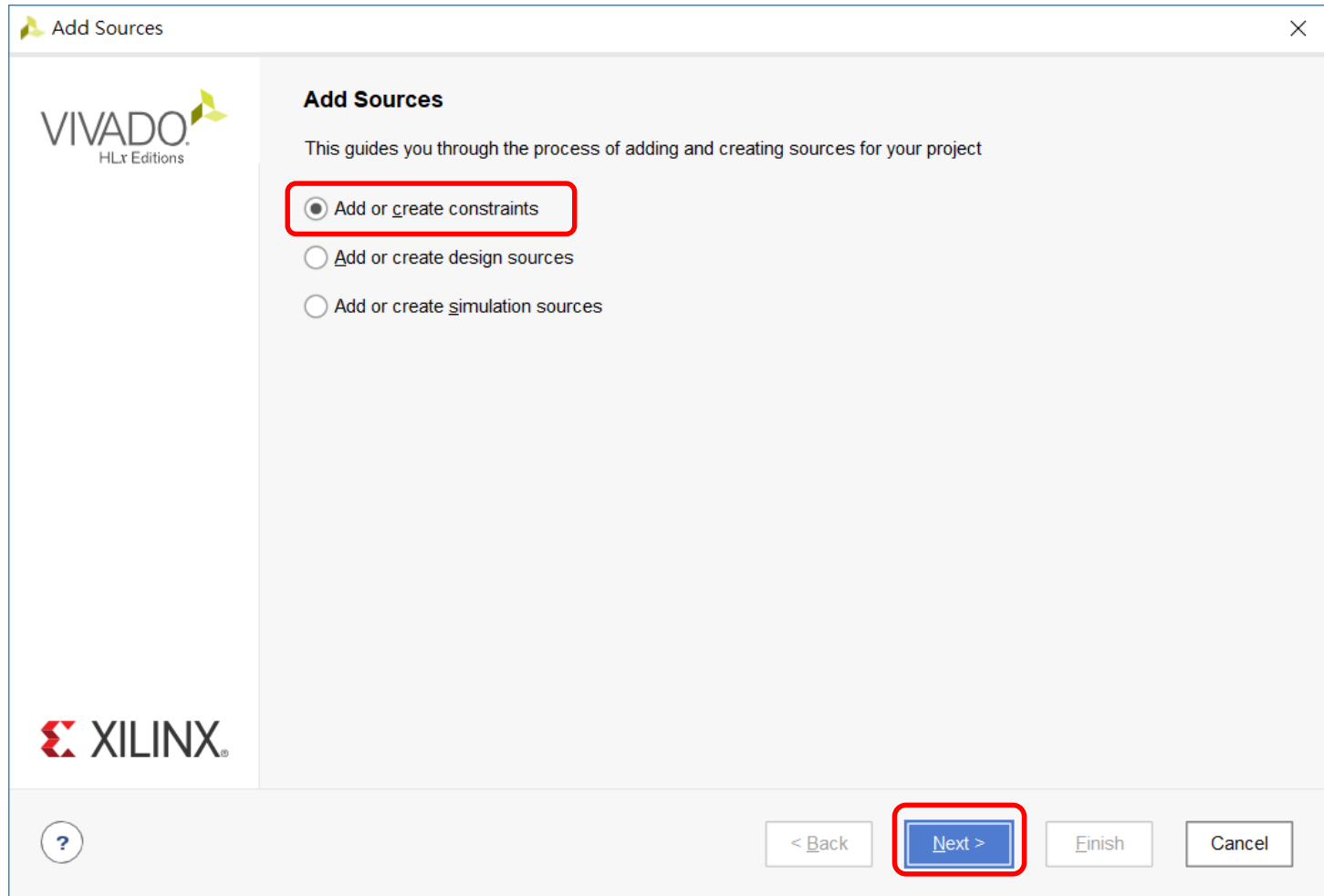
# Lab03.1

# Add Sources

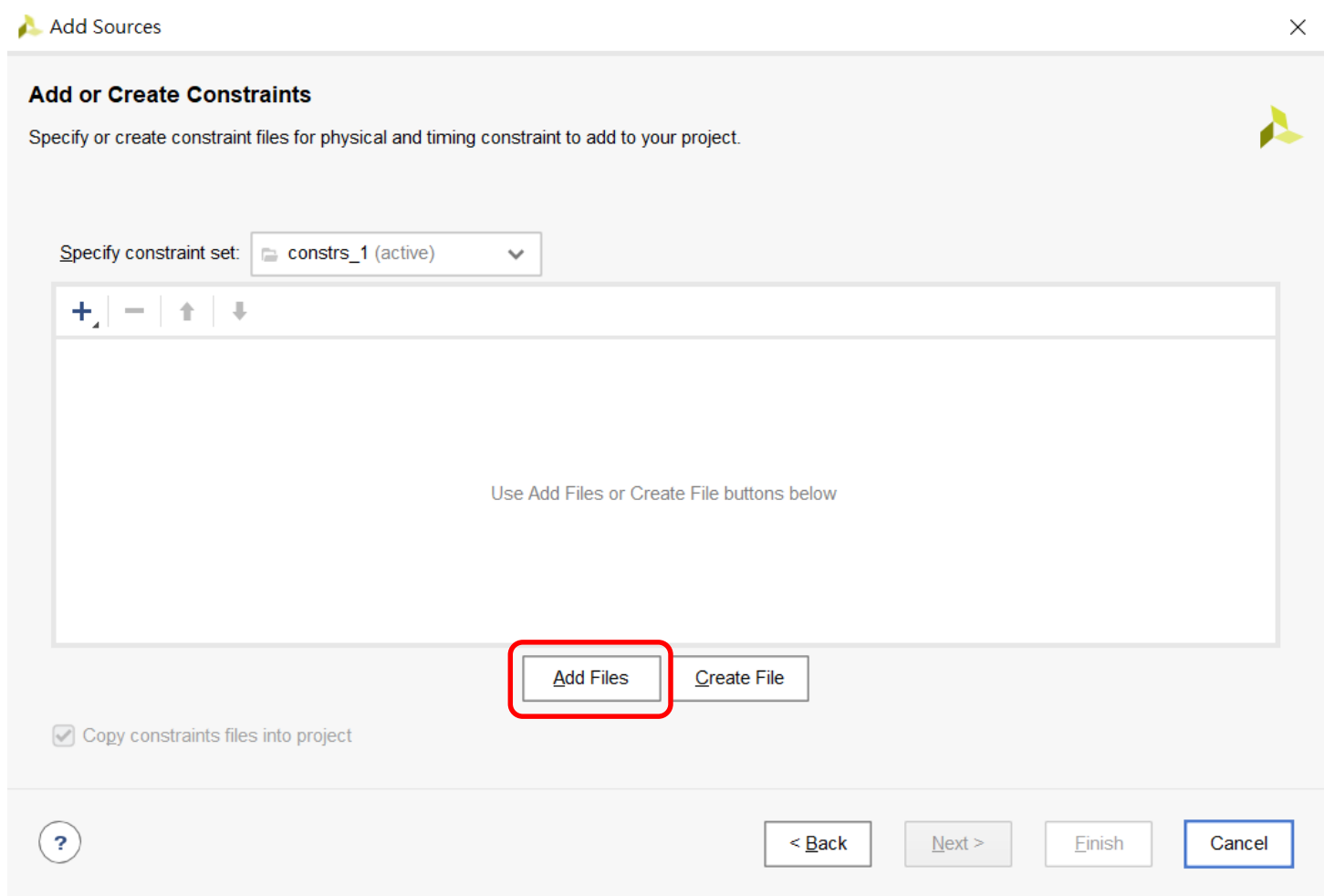
---



# Add Constraints



# Add Files(1/3)



**Add Sources**

**Add or Create Constraints**

Specify or create constraint files for physical and timing constraint to add to your project.

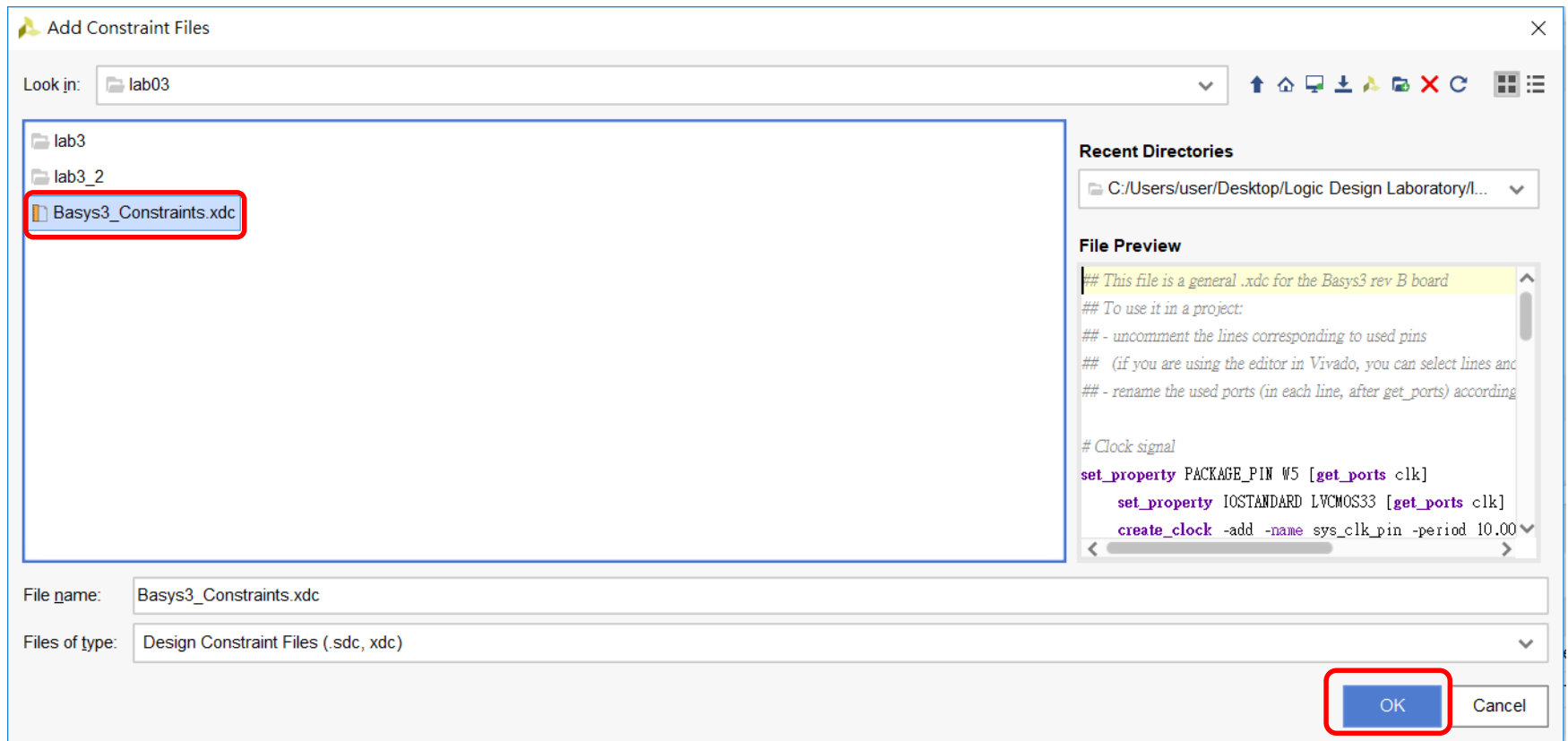
Specify constraint set: constrs\_1 (active)

Use Add Files or Create File buttons below


☒ Copy constraints files into project

? < Back Next > Finish Cancel

# Add Files(2/3)



# Add Files(3/3)

 Add Sources ×

**Add or Create Constraints**

Specify or create constraint files for physical and timing constraint to add to your project.

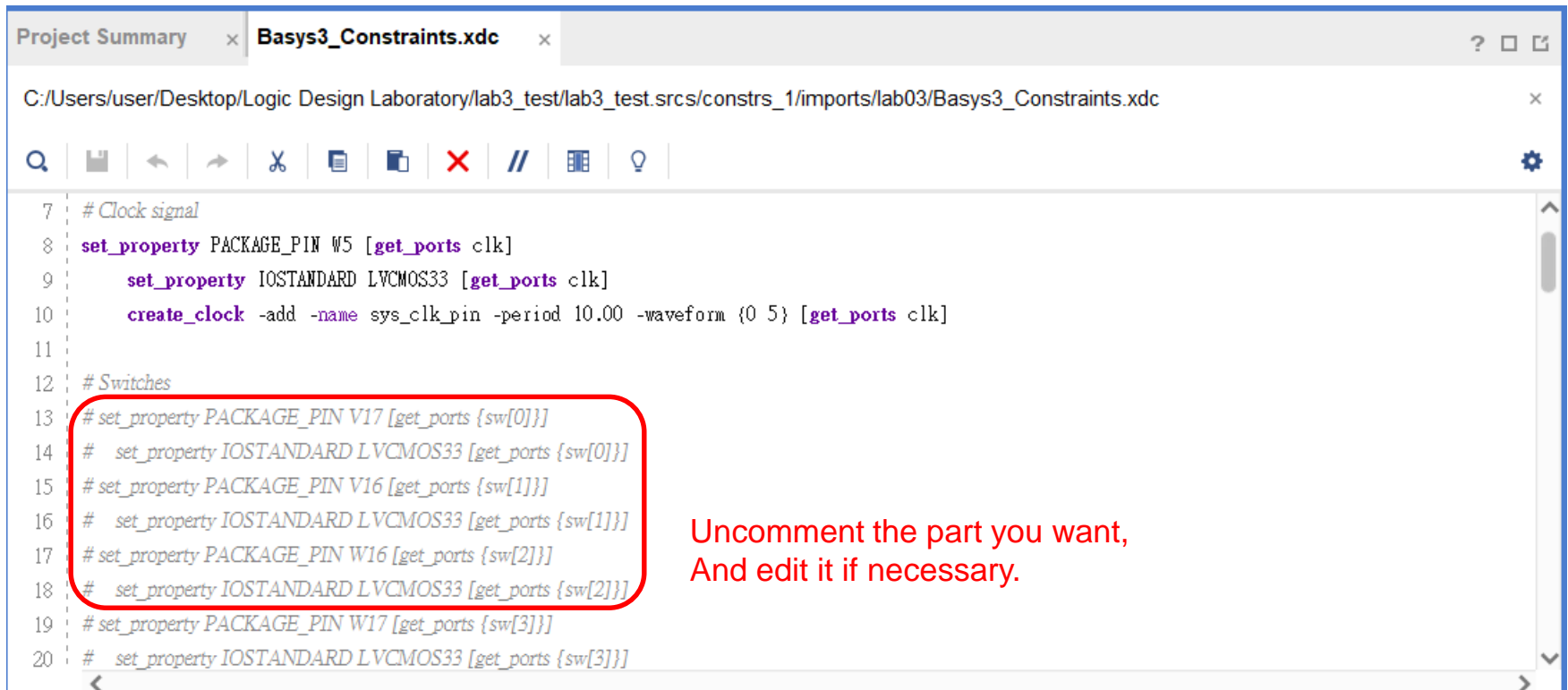
Specify constraint set: constrs\_1 (active) ▼

Constraint File	Location
Basys3_Constraints.xdc	C:\Users\user\Desktop\Logic Design Laboratory\lab03

☒ Copy constraints files into project

? < Back Next > **Finish** Cancel

# Constraints File (\*.xdc)

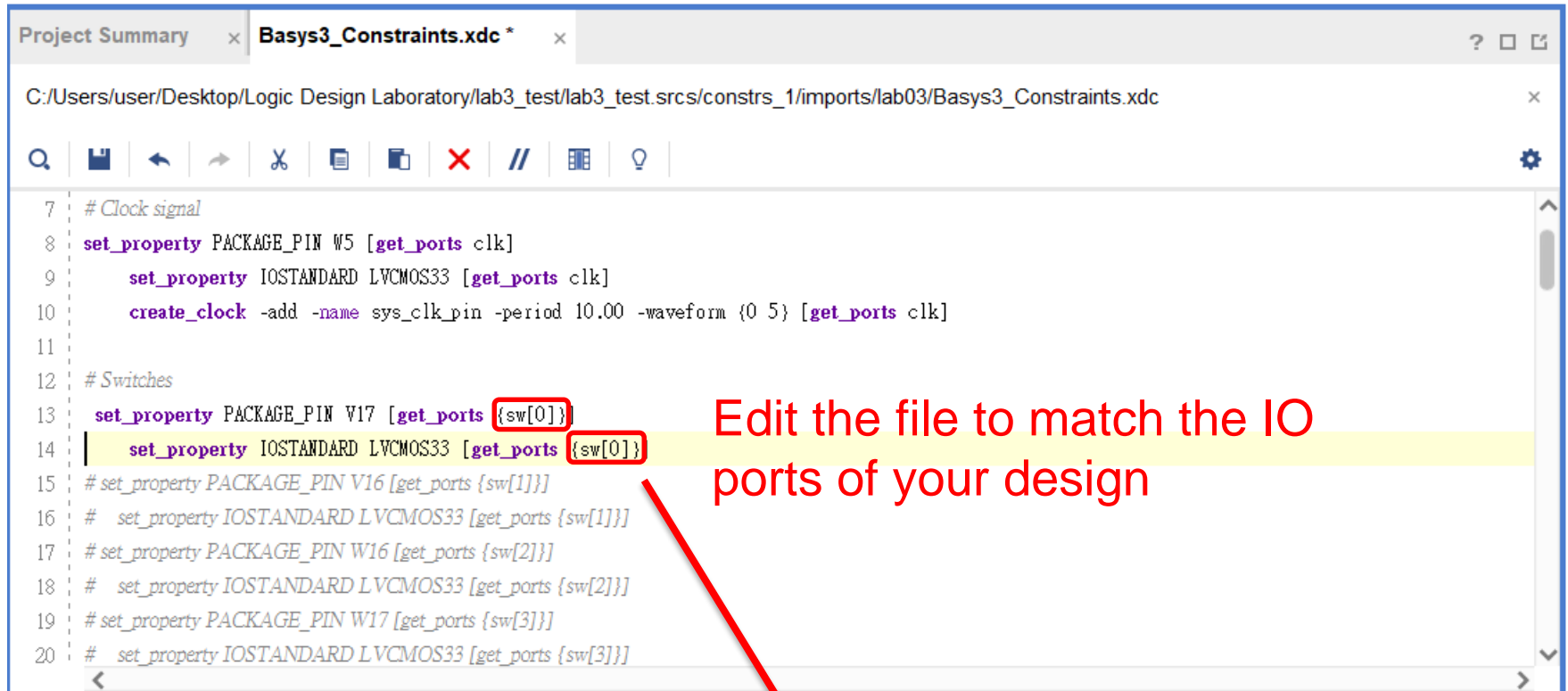


```
Project Summary x Basys3_Constraints.xdc x
C:/Users/user/Desktop/Logic Design Laboratory/lab3_test/lab3_test.srcs/constrs_1/imports/lab03/Basys3_Constraints.xdc

7  # Clock signal
8  set_property PACKAGE_PIN W5 [get_ports clk]
9      set_property IOSTANDARD LVCMOS33 [get_ports clk]
10     create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
11
12  # Switches
13  # set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
14  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
15  # set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
16  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
17  # set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
18  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
19  # set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
20  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
```

Uncomment the part you want,  
And edit it if necessary.

# Constraints File



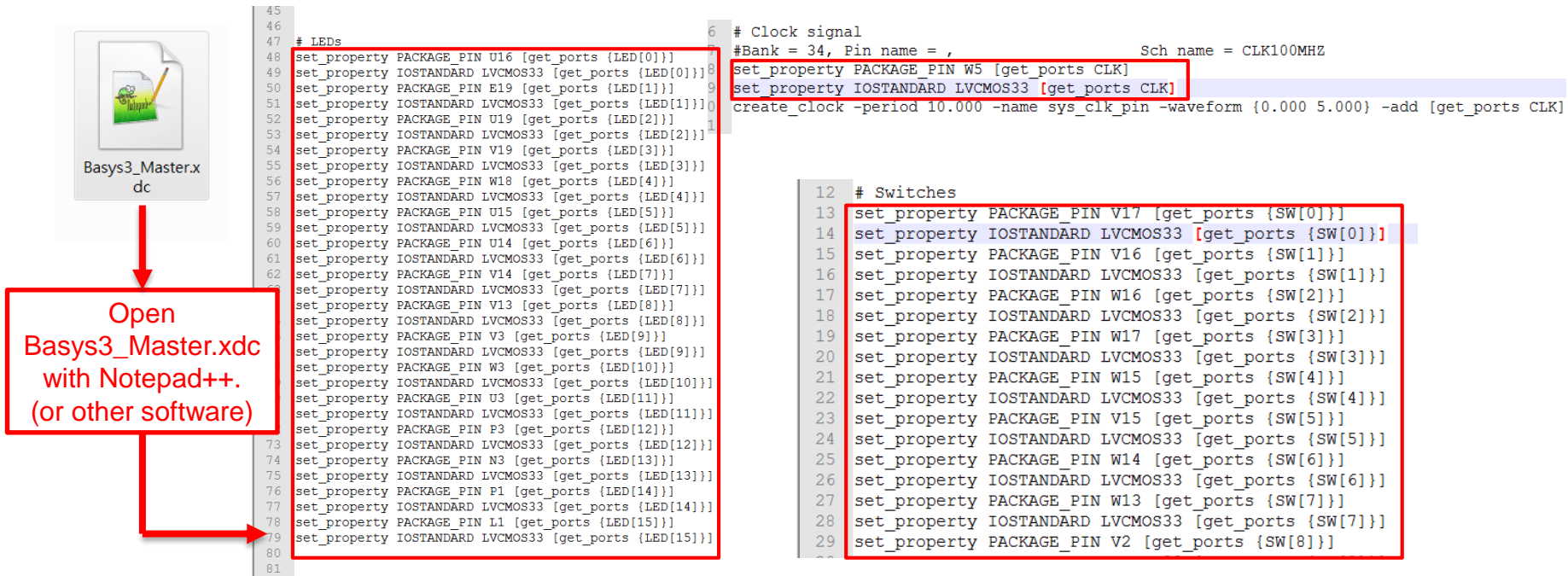
```
7  # Clock signal
8  set_property PACKAGE_PIN W5 [get_ports clk]
9      set_property IOSTANDARD LVCMOS33 [get_ports clk]
10     create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
11
12  # Switches
13  set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
14  set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
15  # set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
16  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
17  # set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
18  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
19  # set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
20  # set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
```

Edit the file to match the IO ports of your design

```
12  # Switches
13  set_property PACKAGE_PIN V17 [get_ports en]
14  set_property IOSTANDARD LVCMOS33 [get_ports en]
```



# You Can Edit XDC File with Other Text Editor



Basys3\_Master.xdc

Open Basys3\_Master.xdc with Notepad++ (or other software)

```
45
46
47 # LEDs
48 set_property PACKAGE_PIN U16 [get_ports {LED[0]}]
49 set_property IOSTANDARD LVCMOS33 [get_ports {LED[0]}]
50 set_property PACKAGE_PIN E19 [get_ports {LED[1]}]
51 set_property IOSTANDARD LVCMOS33 [get_ports {LED[1]}]
52 set_property PACKAGE_PIN U19 [get_ports {LED[2]}]
53 set_property IOSTANDARD LVCMOS33 [get_ports {LED[2]}]
54 set_property PACKAGE_PIN V19 [get_ports {LED[3]}]
55 set_property IOSTANDARD LVCMOS33 [get_ports {LED[3]}]
56 set_property PACKAGE_PIN W18 [get_ports {LED[4]}]
57 set_property IOSTANDARD LVCMOS33 [get_ports {LED[4]}]
58 set_property PACKAGE_PIN U15 [get_ports {LED[5]}]
59 set_property IOSTANDARD LVCMOS33 [get_ports {LED[5]}]
60 set_property PACKAGE_PIN U14 [get_ports {LED[6]}]
61 set_property IOSTANDARD LVCMOS33 [get_ports {LED[6]}]
62 set_property PACKAGE_PIN V14 [get_ports {LED[7]}]
63 set_property IOSTANDARD LVCMOS33 [get_ports {LED[7]}]
64 set_property PACKAGE_PIN V13 [get_ports {LED[8]}]
65 set_property IOSTANDARD LVCMOS33 [get_ports {LED[8]}]
66 set_property PACKAGE_PIN V3 [get_ports {LED[9]}]
67 set_property IOSTANDARD LVCMOS33 [get_ports {LED[9]}]
68 set_property PACKAGE_PIN W3 [get_ports {LED[10]}]
69 set_property IOSTANDARD LVCMOS33 [get_ports {LED[10]}]
70 set_property PACKAGE_PIN U3 [get_ports {LED[11]}]
71 set_property IOSTANDARD LVCMOS33 [get_ports {LED[11]}]
72 set_property PACKAGE_PIN P3 [get_ports {LED[12]}]
73 set_property IOSTANDARD LVCMOS33 [get_ports {LED[12]}]
74 set_property PACKAGE_PIN N3 [get_ports {LED[13]}]
75 set_property IOSTANDARD LVCMOS33 [get_ports {LED[13]}]
76 set_property PACKAGE_PIN P1 [get_ports {LED[14]}]
77 set_property IOSTANDARD LVCMOS33 [get_ports {LED[14]}]
78 set_property PACKAGE_PIN L1 [get_ports {LED[15]}]
79 set_property IOSTANDARD LVCMOS33 [get_ports {LED[15]}]
80
81
6 # Clock signal
#Bank = 34, Pin name = , Sch name = CLK100MHZ
set_property PACKAGE_PIN W5 [get_ports CLK]
set_property IOSTANDARD LVCMOS33 [get_ports CLK]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports CLK]

12 # Switches
13 set_property PACKAGE_PIN V17 [get_ports {SW[0]}]
14 set_property IOSTANDARD LVCMOS33 [get_ports {SW[0]}]
15 set_property PACKAGE_PIN V16 [get_ports {SW[1]}]
16 set_property IOSTANDARD LVCMOS33 [get_ports {SW[1]}]
17 set_property PACKAGE_PIN W16 [get_ports {SW[2]}]
18 set_property IOSTANDARD LVCMOS33 [get_ports {SW[2]}]
19 set_property PACKAGE_PIN W17 [get_ports {SW[3]}]
20 set_property IOSTANDARD LVCMOS33 [get_ports {SW[3]}]
21 set_property PACKAGE_PIN W15 [get_ports {SW[4]}]
22 set_property IOSTANDARD LVCMOS33 [get_ports {SW[4]}]
23 set_property PACKAGE_PIN V15 [get_ports {SW[5]}]
24 set_property IOSTANDARD LVCMOS33 [get_ports {SW[5]}]
25 set_property PACKAGE_PIN W14 [get_ports {SW[6]}]
26 set_property IOSTANDARD LVCMOS33 [get_ports {SW[6]}]
27 set_property PACKAGE_PIN W13 [get_ports {SW[7]}]
28 set_property IOSTANDARD LVCMOS33 [get_ports {SW[7]}]
29 set_property PACKAGE_PIN V2 [get_ports {SW[8]}]
```

# FPGA I/O Assignment

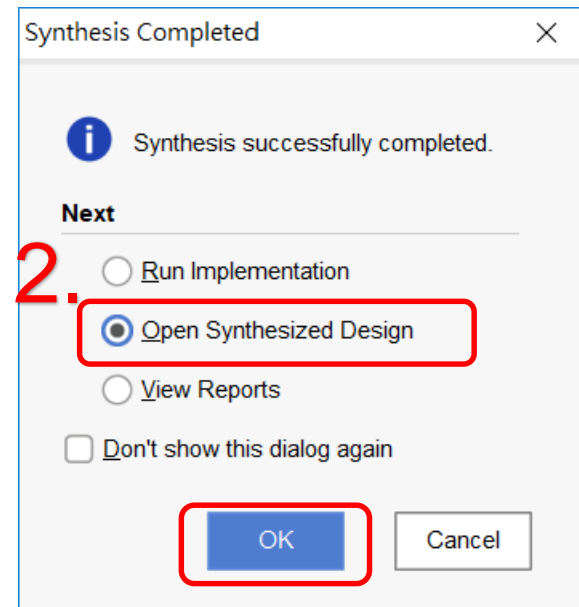
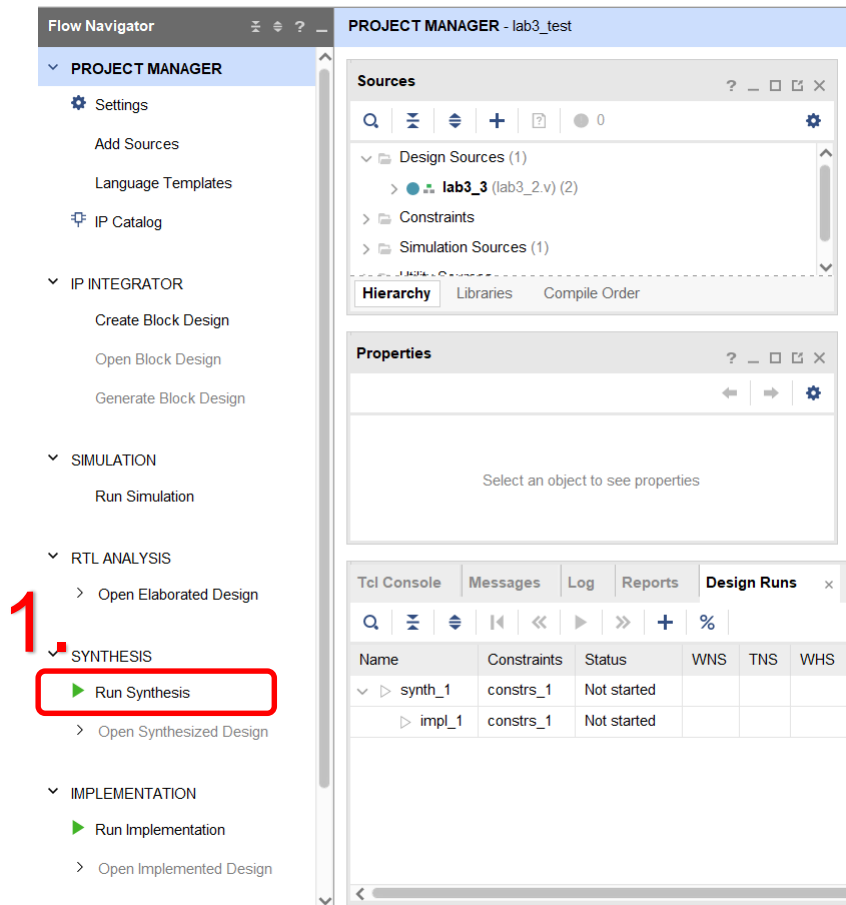


LD15	LD14	LD13	LD12	LD11	LD10	LD9	LD8	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
L1	P1	N3	P3	U3	W3	V3	V13	V14	U14	U15	W18	V19	U19	E19	U16

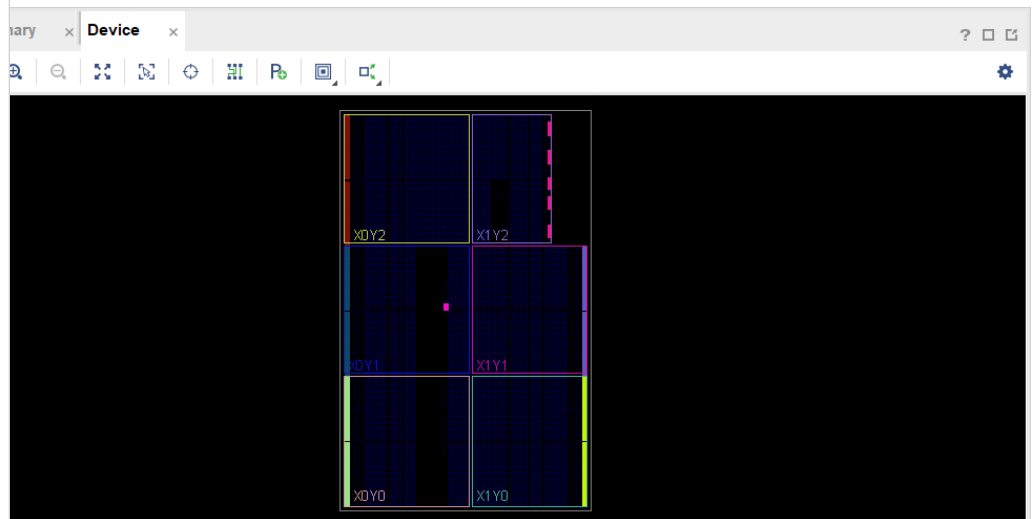
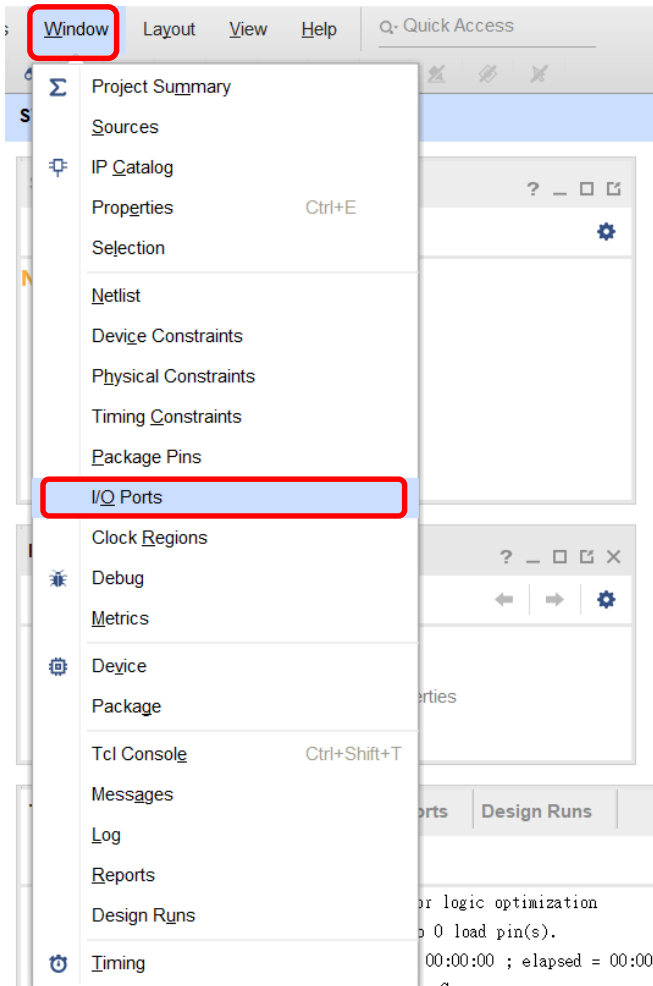
SW15	SW14	SW13	SW12	SW11	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
R2	T1	U1	W2	R3	T2	T3	V2	W13	W14	V15	W15	W17	W16	V16	V17

# Alternative Method to Edit XDC

# Edit XDC File (1/7)



# Edit XDC File (2/7)



# Edit XDC File (3/7)

-----

Tcl Console Messages Log Reports Design Runs **I/O Ports** x

Q Z A + H

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
▼ All ports (20)											
> led (16)	OUT			<input type="checkbox"/>		default (LVCMOS18)	1.800		12	▼ SLOW	▼ NONE
> Scalar ports (4)											

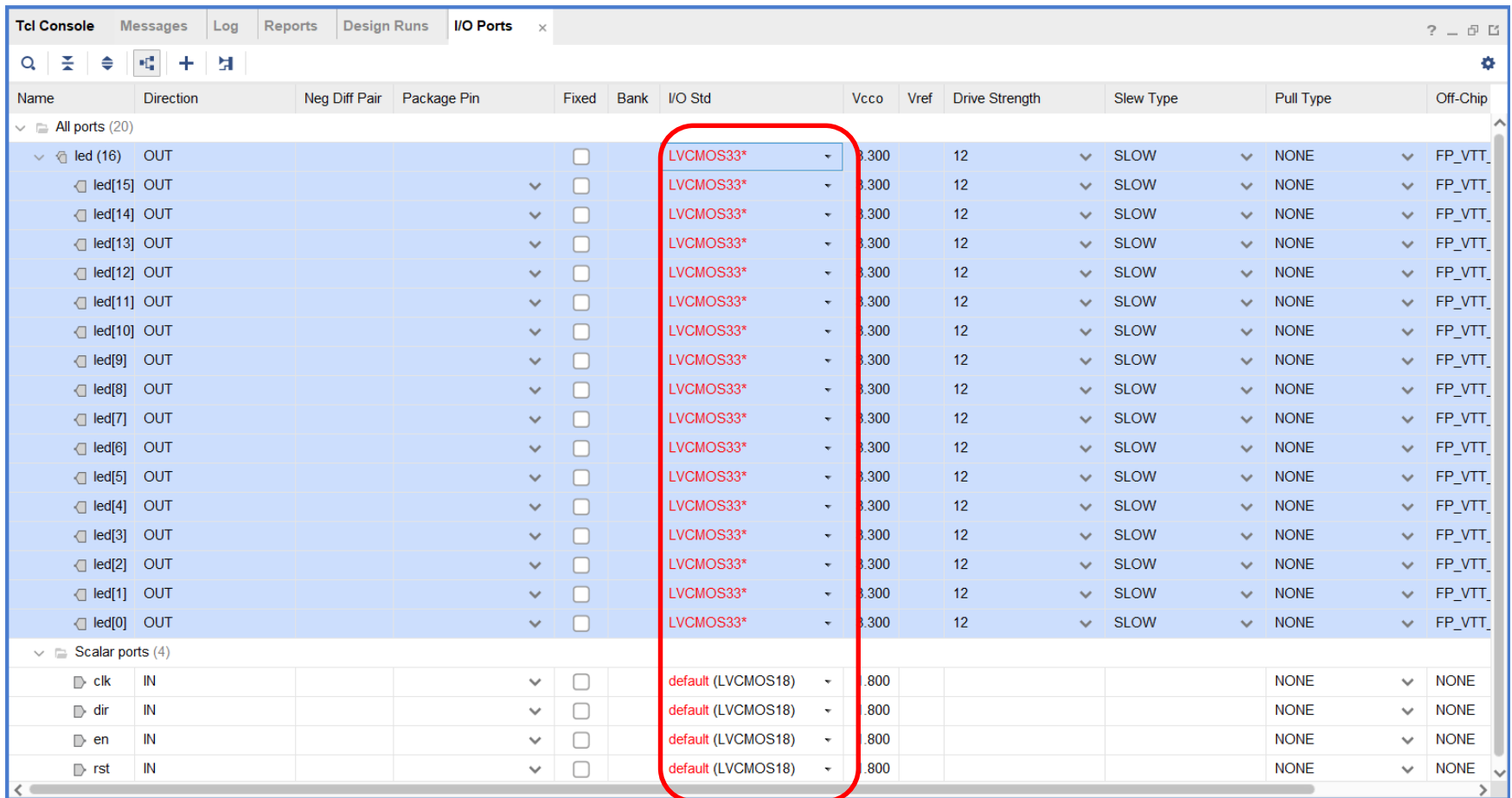
< -----

# Edit XDC File (4/7)

Tcl ConsoleMessagesLogReportsDesign RunsI/O Ports x

# Edit XDC File (5/7)

Select LVCMOS33



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip
led (16)	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[15]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[14]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[13]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[12]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[11]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[10]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[9]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[8]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[7]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[6]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[5]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[4]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[3]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[2]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[1]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[0]	OUT			<input type="checkbox"/>		LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
clk	IN			<input type="checkbox"/>		default (LVCMOS18)	1.800				NONE	NONE
dir	IN			<input type="checkbox"/>		default (LVCMOS18)	1.800				NONE	NONE
en	IN			<input type="checkbox"/>		default (LVCMOS18)	1.800				NONE	NONE
rst	IN			<input type="checkbox"/>		default (LVCMOS18)	1.800				NONE	NONE



# Edit XDC File (6/7)

**Ctrl + S**

Out of Date Design


Saving the current constraints to the target project constraints file may cause your synthesis to go out-of-date. To avoid re-running synthesis, you can force the design up-to-date by selecting the run in the Design Runs tab, right clicking, and selecting 'Force Up-to-Date'.


☐ Don't show this dialog again

OK


Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip
All ports (20)												
led (16)	OUT			<input checked="" type="checkbox"/>	(Multiple)	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[15]	OUT		L1	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[14]	OUT		P1	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[13]	OUT		N3	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[12]	OUT		P3	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[11]	OUT		U3	<input checked="" type="checkbox"/>	34	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[10]	OUT		W3	<input checked="" type="checkbox"/>	34	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[9]	OUT		V3	<input checked="" type="checkbox"/>	34	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[8]	OUT		V13	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[7]	OUT		V14	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[6]	OUT		U14	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[5]	OUT		U15	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[4]	OUT		W18	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[3]	OUT		V19	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[2]	OUT		U19	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[1]	OUT		E19	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
led[0]	OUT		U16	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT
Scalar ports (4)												
clk	IN		W5	<input checked="" type="checkbox"/>	34	LVC MOS33*	3.300				NONE	NONE
dir	IN		V16	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300				NONE	NONE
en	IN		V17	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300				NONE	NONE
rst	IN		W16	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300				NONE	NONE

# Edit XDC File (7/7)


 Save Constraints ✕

Select a target file to write new unsaved constraints to. Choosing an existing file will update that file with the new constraints. 

☒ Create a new file

File type:  XDC ▼

File name:  ✕

File location:  <Local to Project> ▼

☐ Select an existing file

▼

? OK Cancel