EECS2070 02
Lab 03.1: How to Add The Constraint File of The Project

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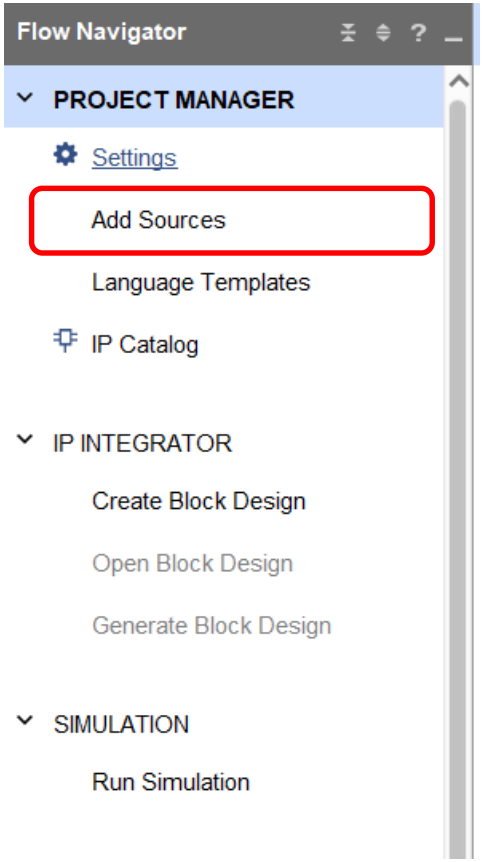
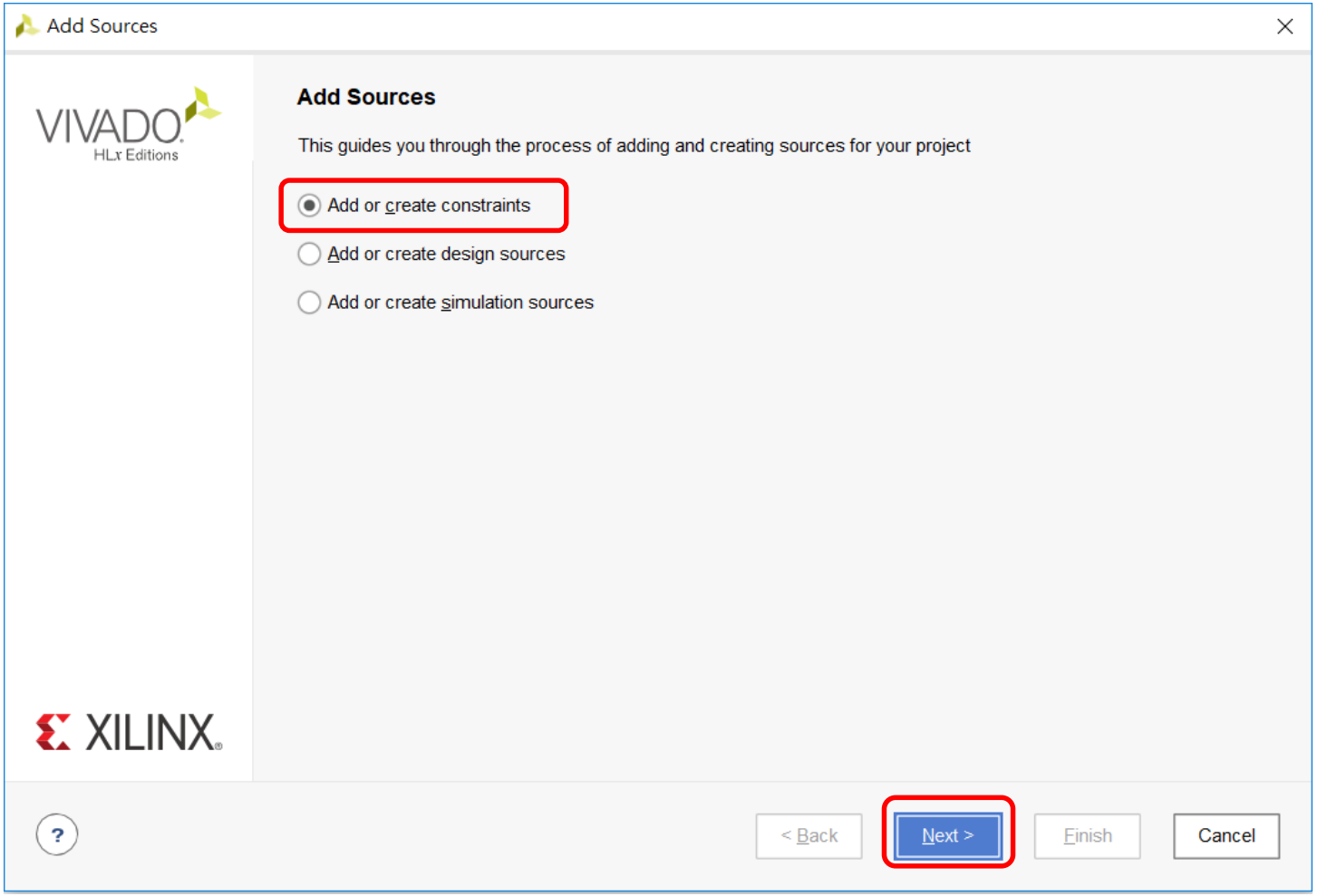
Lab03.1

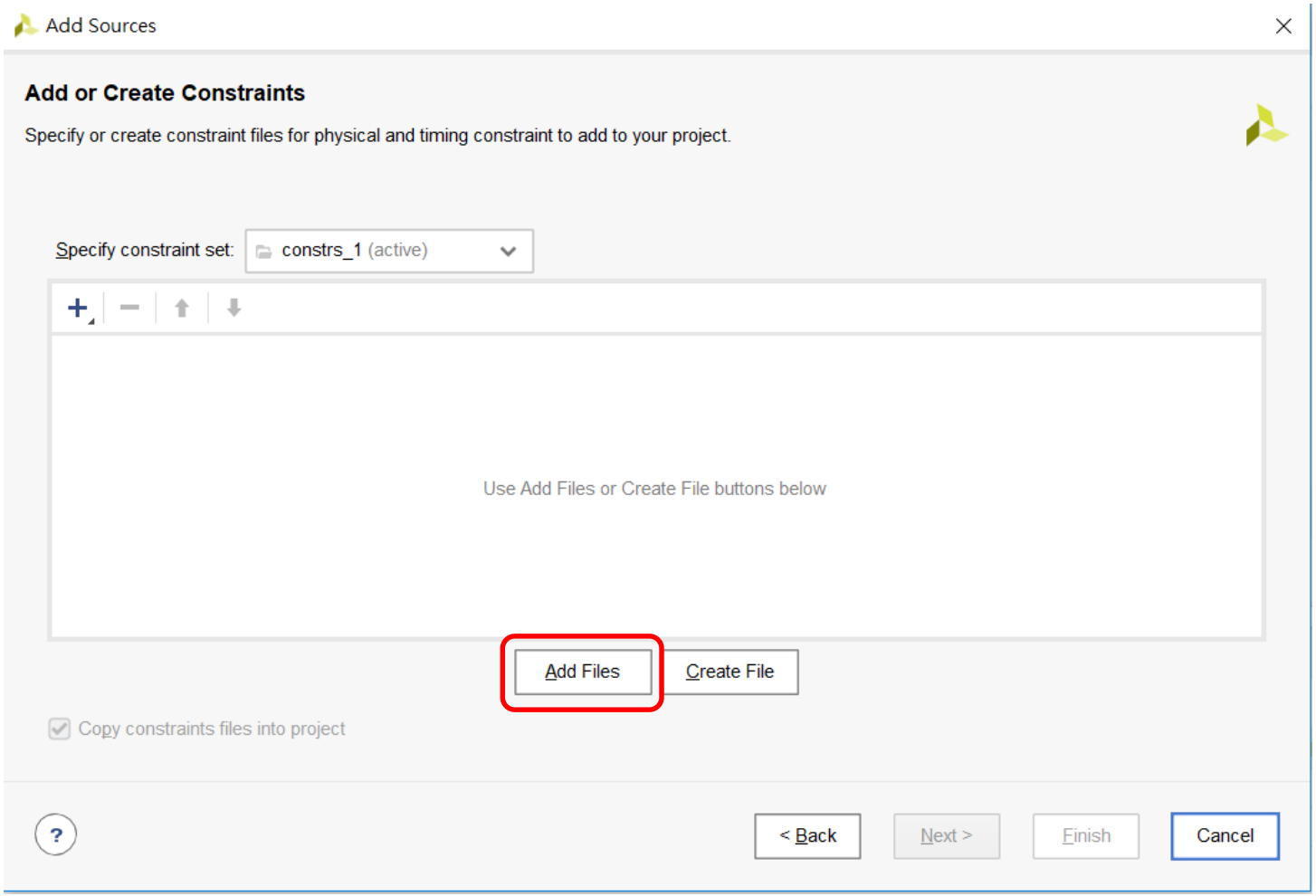
Add Sources


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation

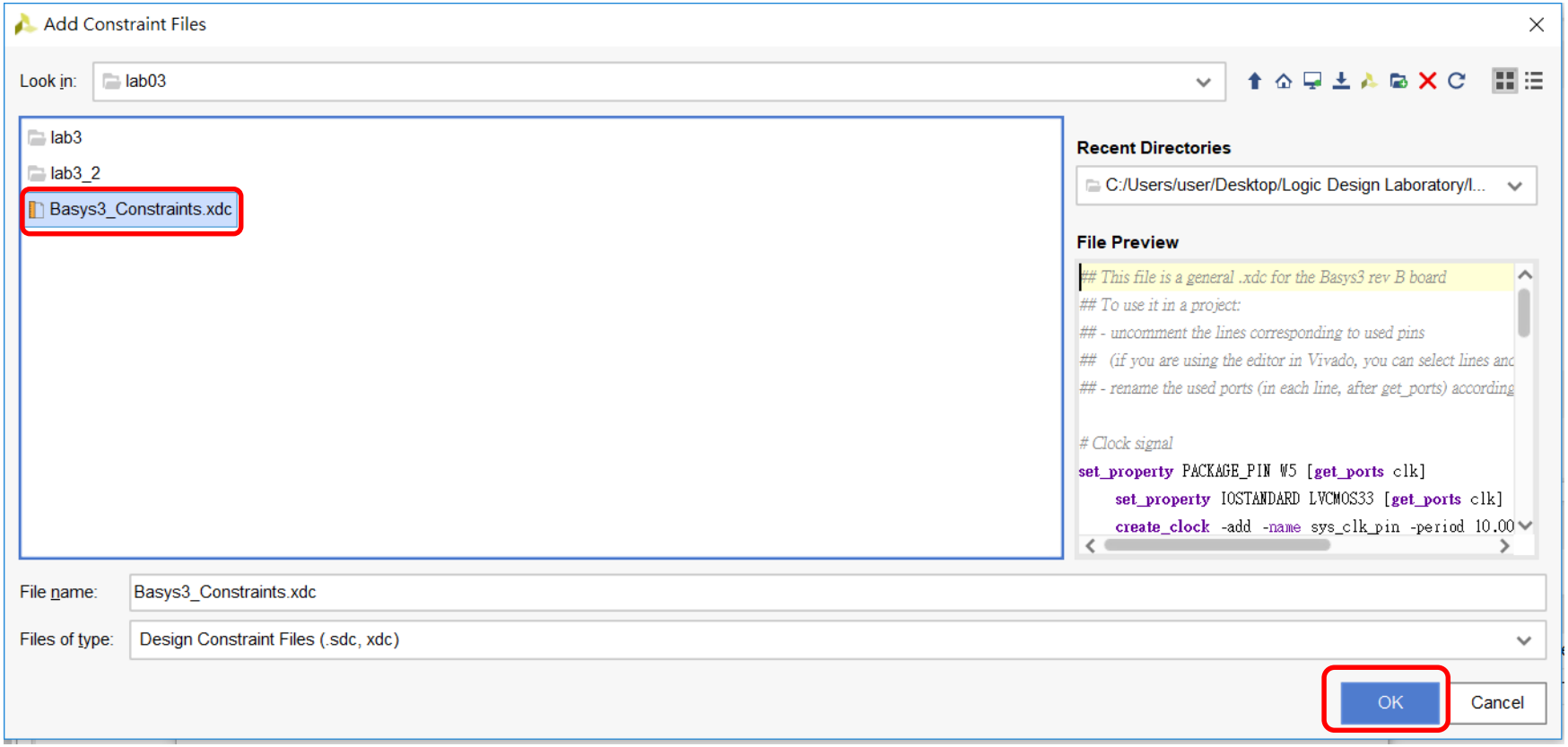
Add Constraints



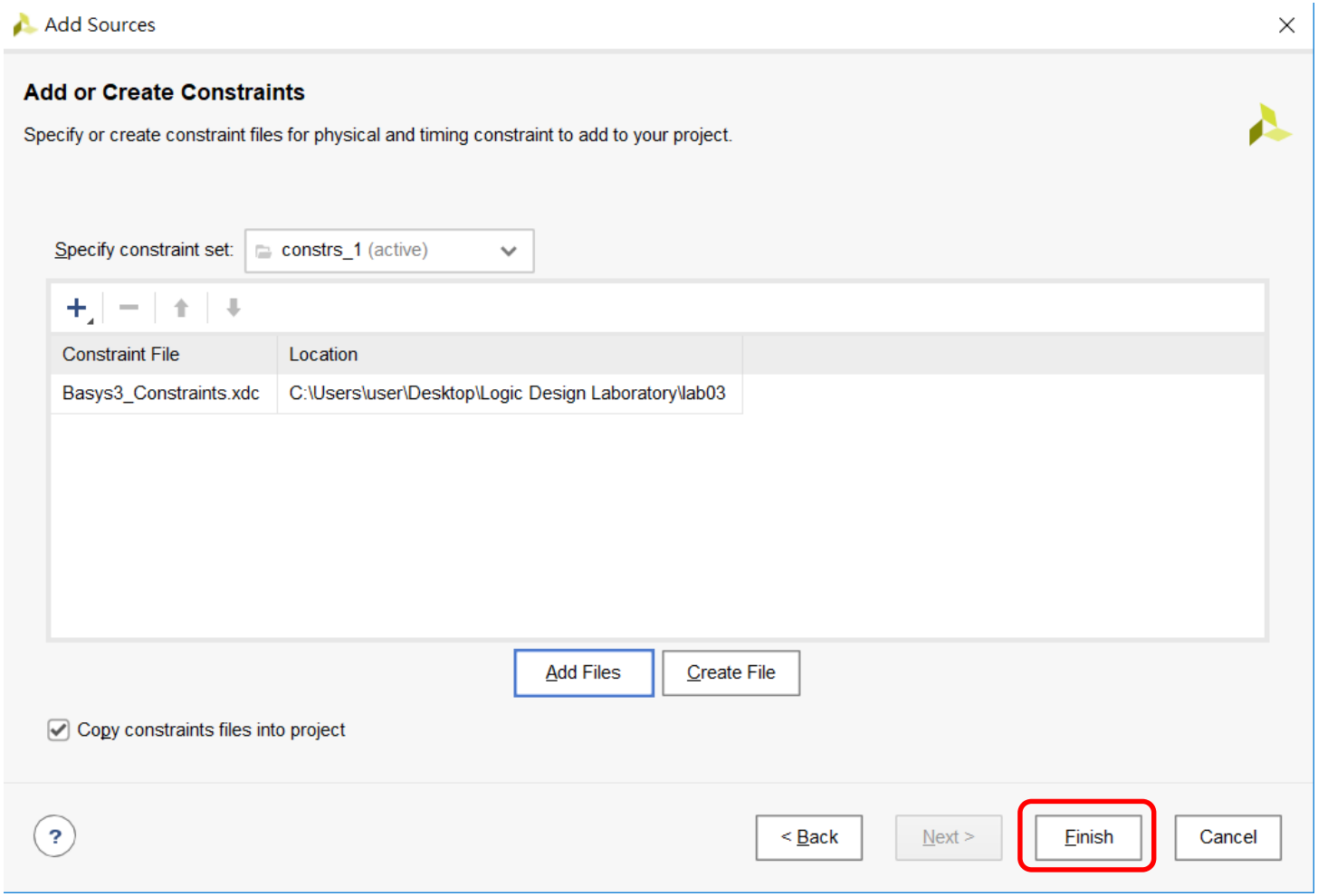
Add Files(1/3)


Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
?
< Back
Next >
Finish
Cancel

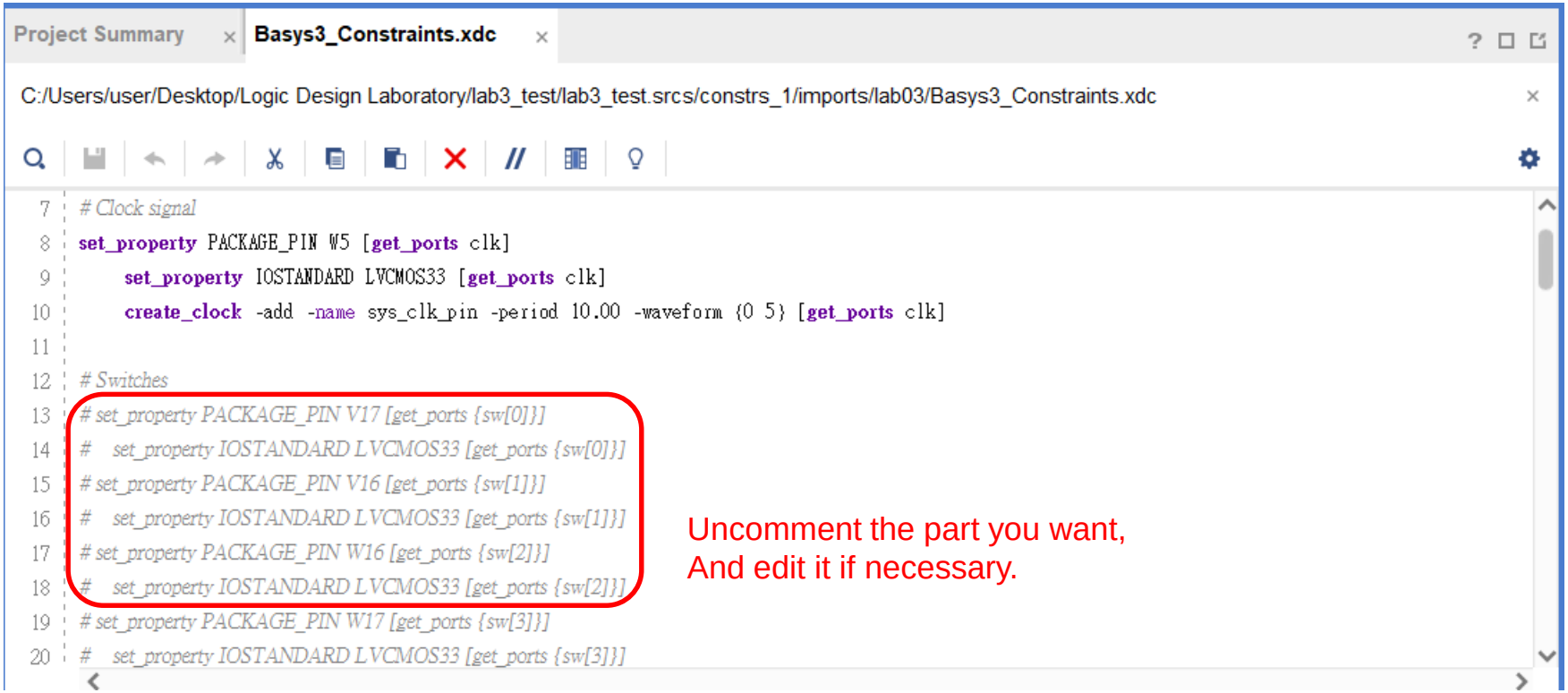
Add Files(2/3)


Add Constraint Files
Look in:
lab03
lab3
lab3_2
Basys3_Constraints.xdc
Recent Directories
C:/Users/user/Desktop/Logic Design Laboratory/l...
File Preview
This file is a general .xdc for the Basys3 rev B board
To use it in a project:
- uncomment the lines corresponding to used pins
(if you are using the editor in Vivado, you can select lines and
- rename the used ports (in each line, after get_ports) according
Clock signal
set_property PACKAGE_PIN W5 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00
File name:
Basys3_Constraints.xdc
Files of type:
Design Constraint Files (.sdc, xdc)
OK
Cancel

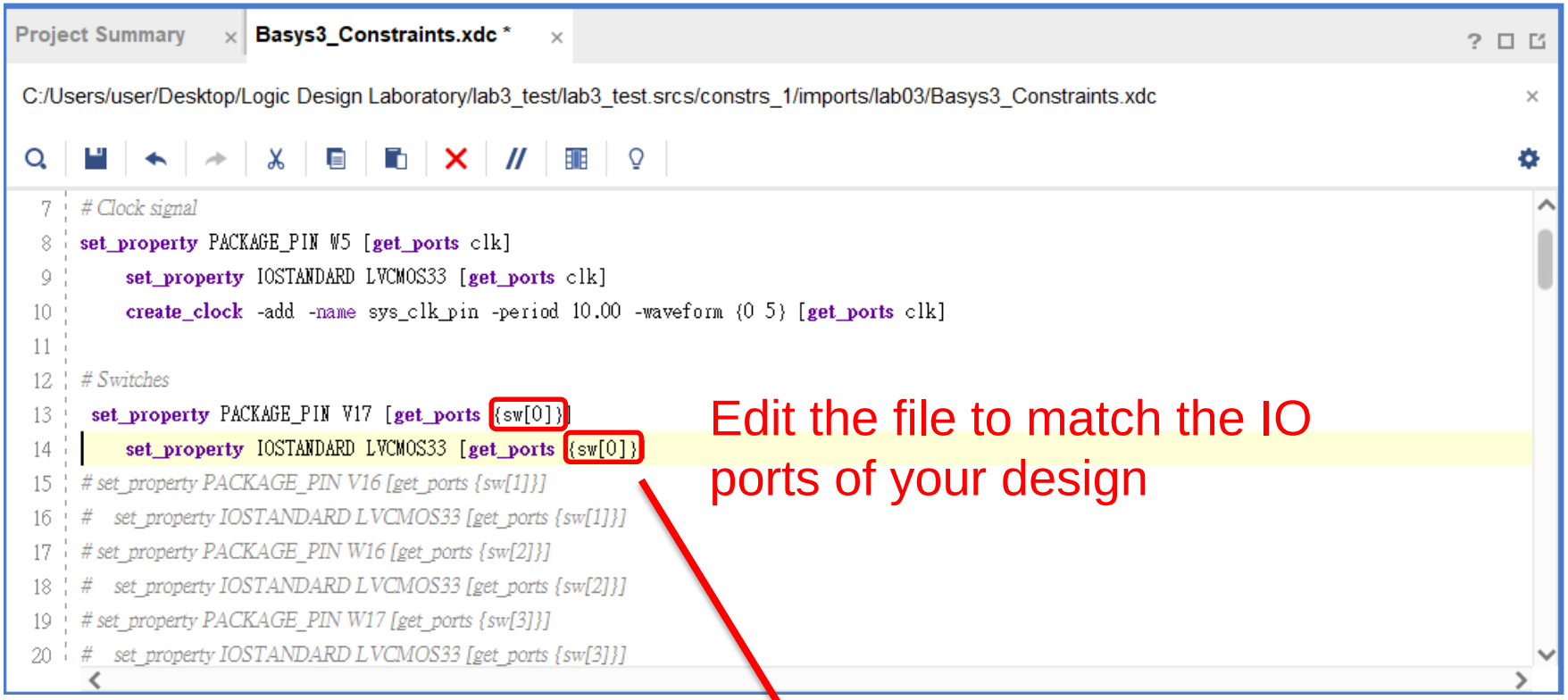
Add Files(3/3)


Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Constraint File
Location
Basys3_Constraints.xdc
C:\Users\user\Desktop\Logic Design Laboratory\lab03
Add Files
Create File
Copy constraints files into project
?
< Back
Next >
Finish
Cancel

Constraints File (*.xdc)



Constraints File



You Can Edit XDC File with Other Text Editor

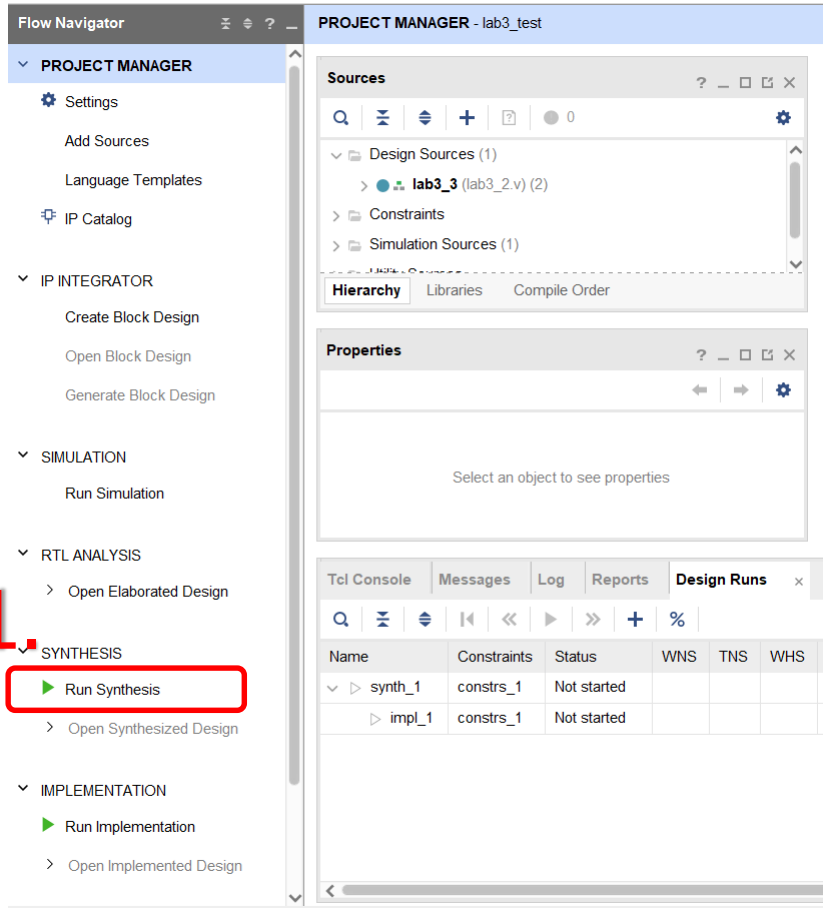
FPGA I/O Assignment

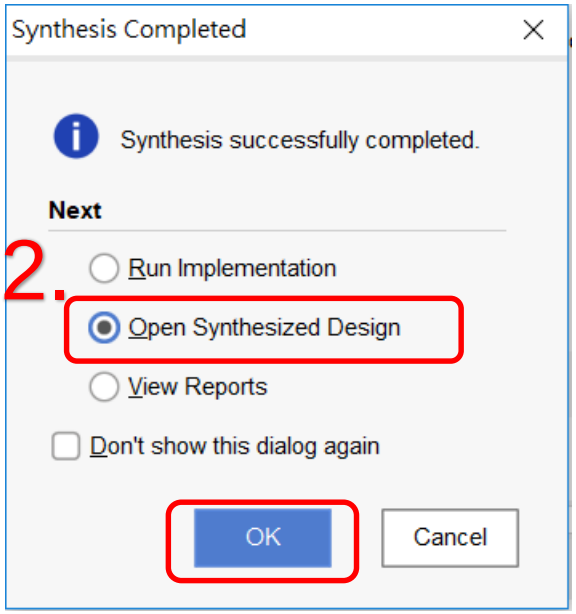
LD15	LD14	LD13	LD12	LD11	LD10	LD9	LD8	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
L1	P1	N3	P3	U3	W3	V3	V13	V14	U14	U15	W18	V19	U19	E19	U16

SW15	SW14	SW13	SW12	SW11	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
R2	T1	U1	W2	R3	T2	T3	V2	W13	W14	V15	W15	W17	W16	V16	V17

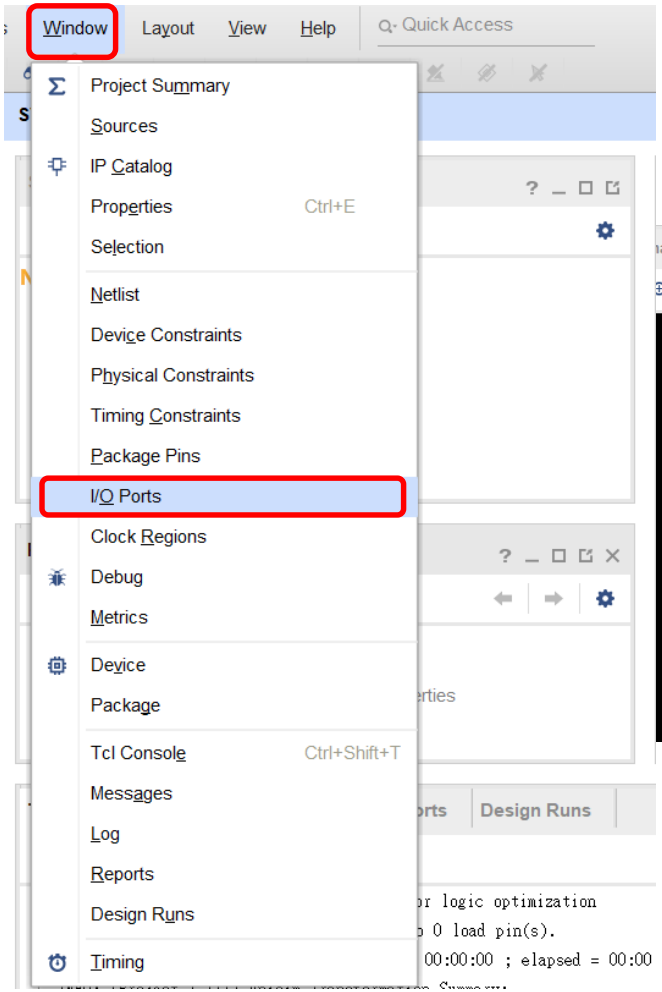
Alternative Method to Edit XDC

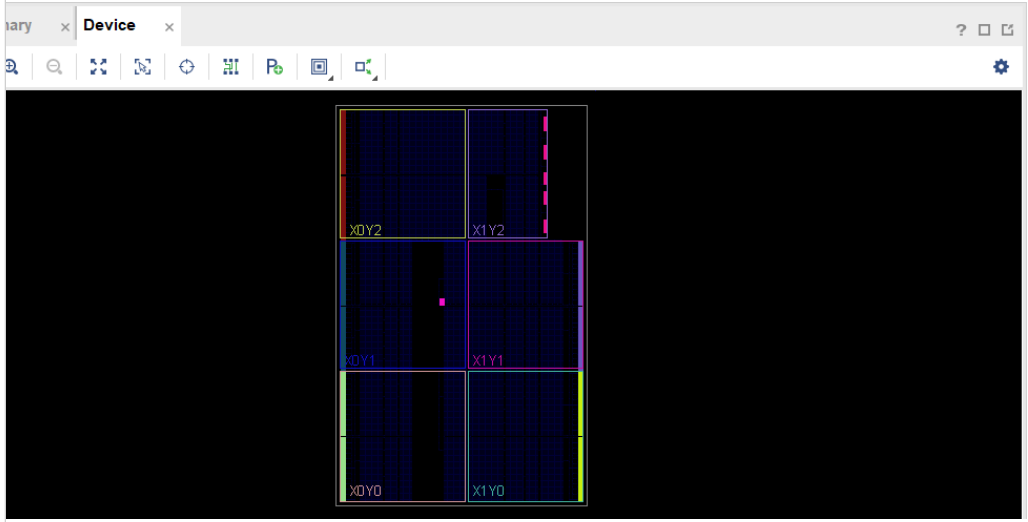
Edit XDC File (1/7)



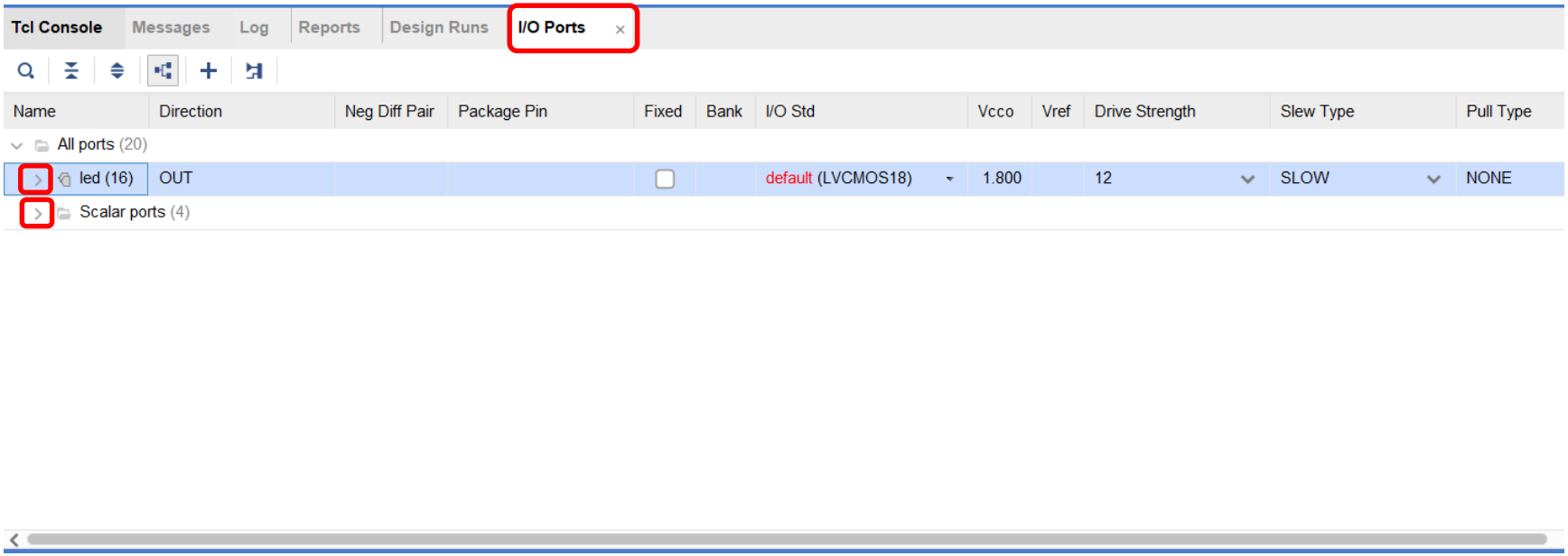


Edit XDC File (2/7)

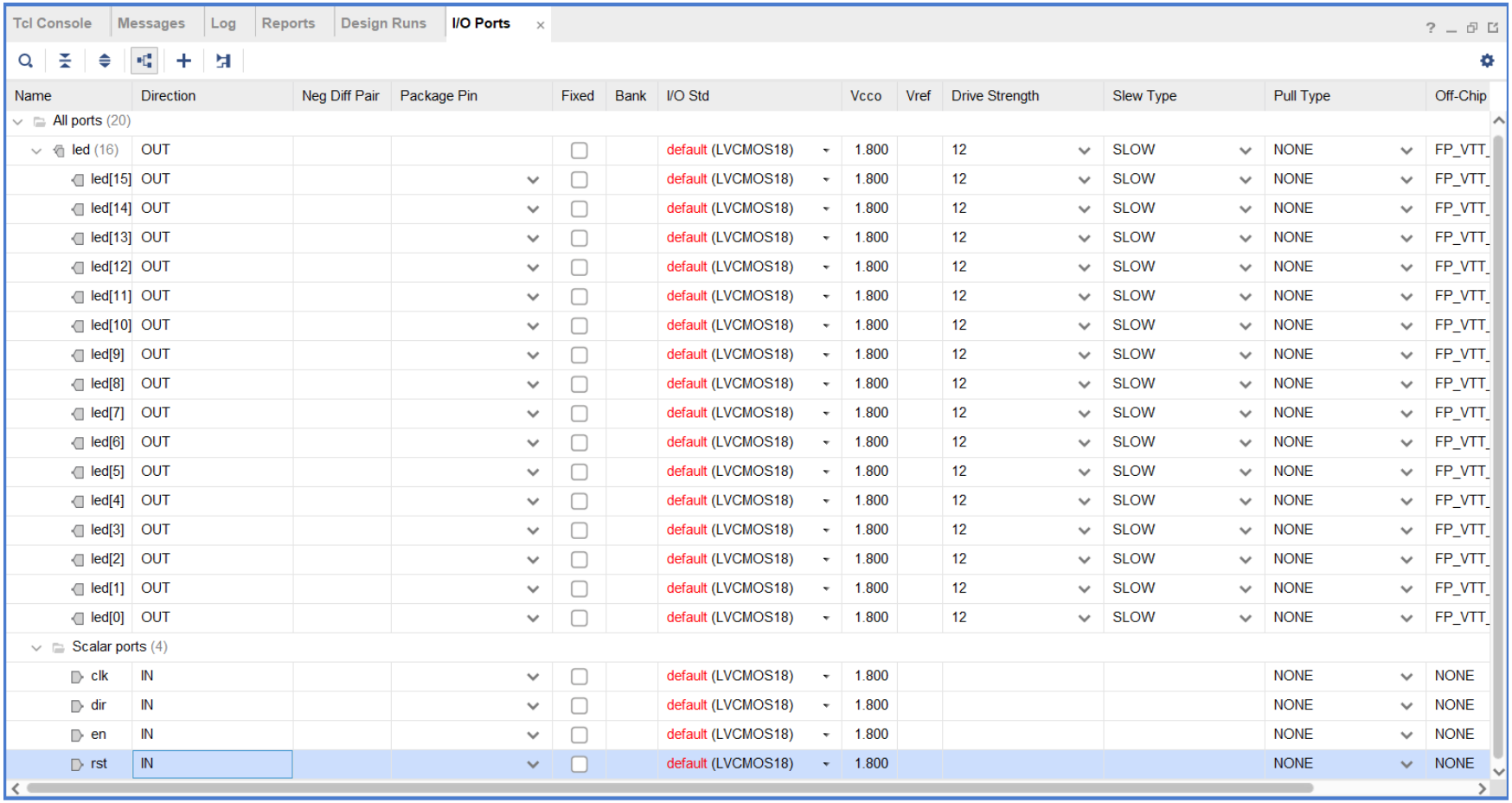




Edit XDC File (3/7)



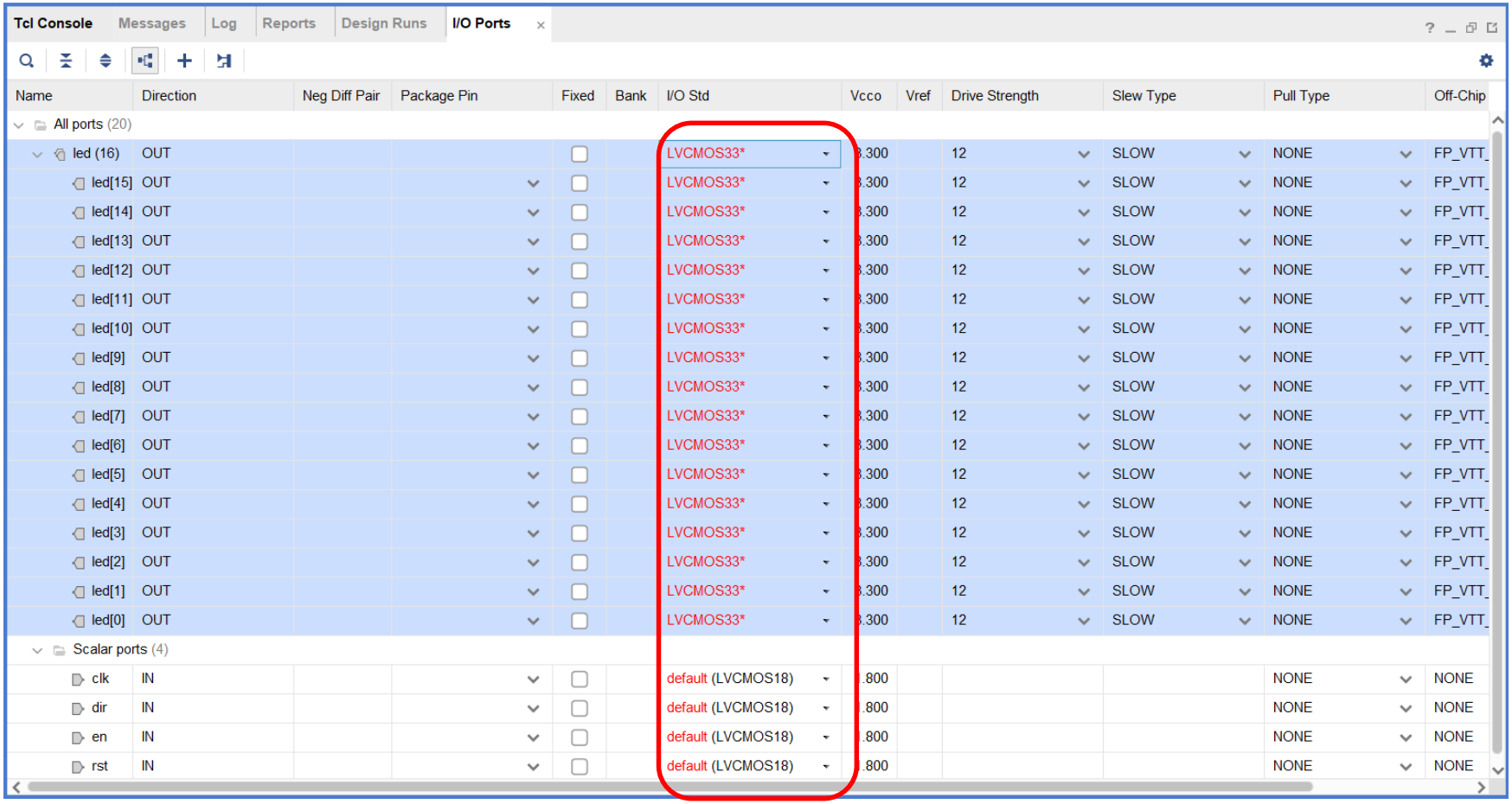
Edit XDC File (4/7)



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip
All ports (20)												
led (16)	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[15]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[14]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[13]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[12]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[11]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[10]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[9]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[8]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[7]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[6]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[5]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[4]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[3]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[2]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[1]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
led[0]	OUT					default (LVCMOS18)	1.800		12	SLOW	NONE	FP_VTT_
Scalar ports (4)												
clk	IN					default (LVCMOS18)	1.800				NONE	NONE
dir	IN					default (LVCMOS18)	1.800				NONE	NONE
en	IN					default (LVCMOS18)	1.800				NONE	NONE
rst	IN					default (LVCMOS18)	1.800				NONE	NONE

Edit XDC File (5/7)

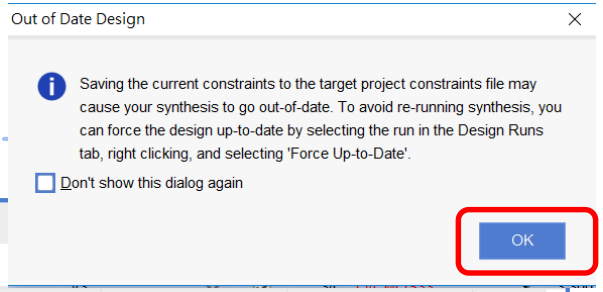
Select LVCMOS33



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip
All ports (20)												
led (16)	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[15]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[14]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[13]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[12]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[11]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[10]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[9]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[8]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[7]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[6]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[5]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[4]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[3]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[2]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[1]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[0]	OUT					LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
Scalar ports (4)												
clk	IN					default (LVCMOS18)	1.800				NONE	NONE
dir	IN					default (LVCMOS18)	1.800				NONE	NONE
en	IN					default (LVCMOS18)	1.800				NONE	NONE
rst	IN					default (LVCMOS18)	1.800				NONE	NONE

Edit XDC File (6/7)

Ctrl + S



Tcl Console | Messages | Log | Reports | Design Runs | I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip
All ports (20)												
led (16)	OUT			☑	(Multipl	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[15]	OUT		L1	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[14]	OUT		P1	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[13]	OUT		N3	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[12]	OUT		P3	☑	35	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[11]	OUT		U3	☑	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[10]	OUT		W3	☑	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[9]	OUT		V3	☑	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[8]	OUT		V13	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[7]	OUT		V14	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[6]	OUT		U14	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[5]	OUT		U15	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[4]	OUT		W18	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[3]	OUT		V19	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[2]	OUT		U19	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[1]	OUT		E19	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
led[0]	OUT		U16	☑	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_
Scalar ports (4)												
clk	IN		W5	☑	34	LVCMOS33*	3.300				NONE	NONE
dir	IN		V16	☑	14	LVCMOS33*	3.300				NONE	NONE
en	IN		V17	☑	14	LVCMOS33*	3.300				NONE	NONE
rst	IN		W16	☑	14	LVCMOS33*	3.300				NONE	NONE

Edit XDC File (7/7)