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Perspective

Integrated Photonic Neural Networks: Opportunities and Challenges

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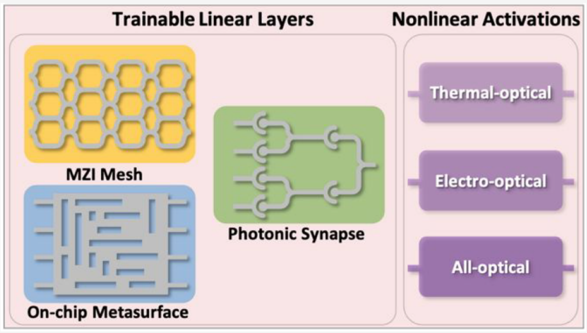
ABSTRACT: Photonic neural networks benefit from the use of photons to perform intelligent inference computing with ultrafast and ultralow energy consumption in ultra-high-throughput, providing the efficient photonic hardware for the new generation of intelligent computing, and the effective way to support large-scale integration for on-chip all-optical computing chips. With the rapid development of photonic neural networks, demands for efficient computation power have increased dramatically. However, the weak and impractical optical nonlinear activations, the lack of suitable configurations for integrated photonic hardware, and proper optical storage mediums pose challenges to this field. In this Perspective, we propose our current point of view and a suggestive roadmap in the field of integrated photonic platform for optical neural networks. Throughout the discussion, we highlight recent progresses meeting with major challenges. We also identify some next challenges still ahead to realize integrated photonic neural networks capable of matching the current computational power of graphic cards.



KEYWORDS: *integrated photonics, optical neural network, metasurface, spiking neural network, optical nonlinear activation, on-chip training*

■ INTRODUCTION

Inspired by biological brains, as one of the artificial intelligence algorithms, neural networks have the excellent inference performance in the execution of inference tasks due to the superior learning ability.[1,2] So far, neural networks have shown the outstanding performance and vigorous application prospect in various fields such as speech recognition,[3,4] image classification,[5,6] computer vision,[7,8] and natural language processing.[9,10] Nearly two decades past the realization of the limits for Moore's law,[11−14] processors based on electronic hardware have finally hit the bottleneck of unsustainable performance growth. Yet, demands for high-performance computing have dramatically increased due to the proliferation of artificial intelligence.[15−17] Such demands have resulted in significantly increased energy consumption in this field,[18−21] which is becoming the primary limitation for deployment and further development. In fact, one of the largest neural networks required 3.14E23 floating-point operations per second (FLOPS) of computation[22] to train. These computations usually take the form of a matrix multiplication,[23] which is greatly limited in speed and energy efficiency by the nature of the electronic devices due to the limited bandwidth and electronic signals easy to interfere with each other,[24,25] forcing a binary form of low level operations with careful consideration of signal integrity. In contrast, photonic processors that compute with photons instead of electrons display some extraordinary properties, such as an ultrawide communication bandwidth, ultrahigh processing frequency, and ultralow energy consumption.[26−28] Apart from these single-threaded advantages, additional dimensions division multiplexing of light field such as wavelength[29,30] and spatial mode[31−33] enable multithread processing with almost no extra computing overhead, leading to a significant acceleration against traditional electronic computers.

The conventional photonic computing framework under the von-Neumann architecture aims to form individual photonic devices with a preoptimized performance to a photonic integrated circuit and, further, to construct the photonic computing chip, which owns regular physical structures and clear physical principles, but a single function and a large integrated crosstalk.[34−37] In addition, the trade-off between ultrafast response time and ultralow energy consumption has brought great challenges to the large-scale integration of

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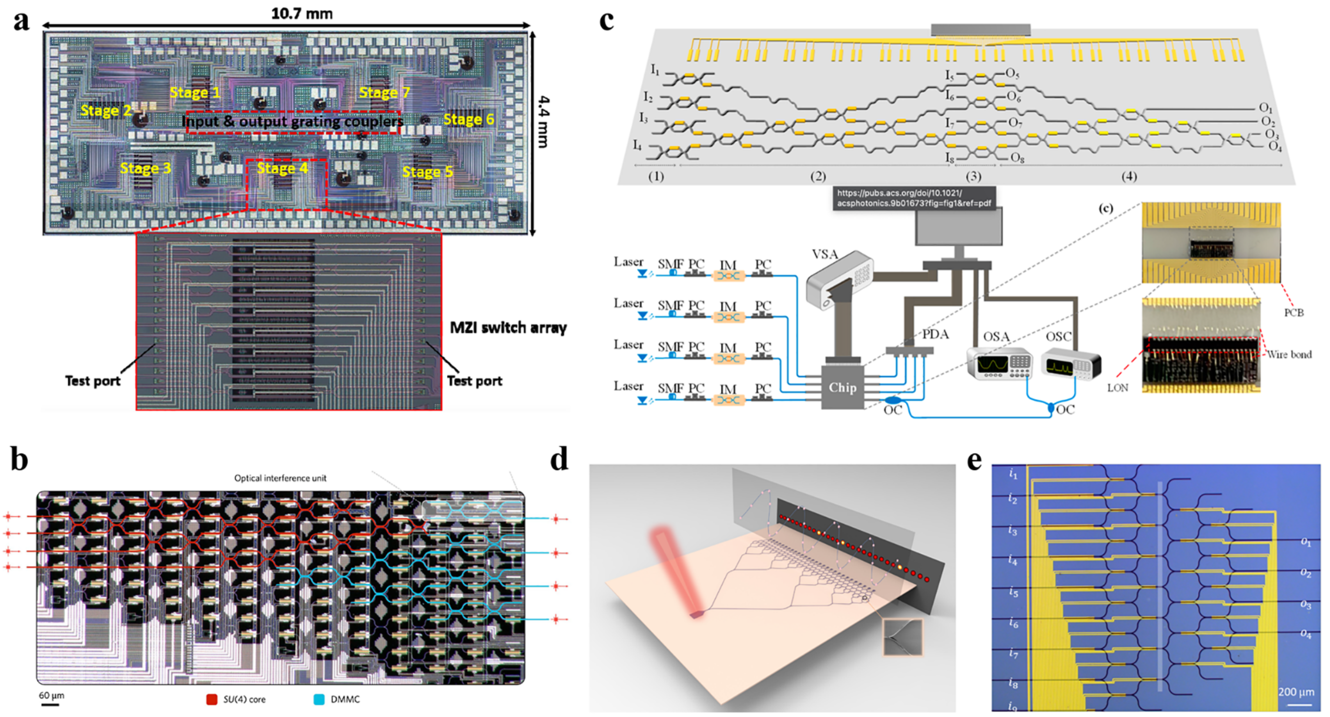

Figure 1. On-chip waveguide-based IPNNs. (a) Optical image of the fabricated 16 × 16 optical switch after an electrical and optical package. Reprinted with permission from ref 53. Copyright 2016 Optical Society of America. https://creativecommons.org/licenses/by/4.0/. (b) Optical micrograph illustration of the experimentally demonstrated optical interference unit, realizing both matrix multiplication (red highlighted) and attenuation (blue highlighted) fully optically. Reprinted with permission from ref 54. Copyright 2017 Springer Nature. (c) Reconfigurable optical signal processing circuits capable dynamically configuring functions and schematic of the experimental setup. Reprinted with permission from ref 55. Copyright 2020 American Chemical Society. (d) Schematic diagram of the all-optical transcendental equation solver based on the convolutional neural network. Reprinted with permission from ref 56. Copyright 2021 Chinese Academy of Sciences. https://creativecommons.org/licenses/by/4.0/. (e) Optical micrograph of the locally connected IPNNs with nine input ports (i_1−i_9) and four output ports (o_1−o_4). Reprinted with permission from ref 57. Copyright 2022 De Gruyter. https://creativecommons.org/licenses/by/4.0/.

conventional photonic chips following the von Neumann architecture. Thus, conventional photonic computing is more suitable for processing computing tasks with specific functions.[38,39] Compared with the conventional photonic computing scheme, the emerging photonic computing framework, the neural network, which came into being under the non-von Neumann framework has the characteristics of processing, in memory, multiple functions and the ability to perform intelligent inference tasks.[30,40,41] Many schemes for optical neural networks (ONNs) have been explored in the past decades. Before the rising trend of integrated waveguides made possible by advances in complementary metal oxide semiconductor (CMOS) fabrication,[42] ONNs usually take the form of free-space diffractions.[43−46] The core component for reconfigurable free space diffractive ONNs is spatial light modulator (SLM),[47] which operates as the programmable input light controller for the neural network. For free-space ONNs, crosstalk noise is normally negligible, thus enabling analogue computation,[48,49] which gives birth to the earliest steps of optical computing, including optical matrix multipliers and optical diffractive neural networks.[50−52] However, such implementations are not viable for deployment due to the requirement for SLM and free space.

Integrated photonic neural networks (IPNNs) are much more compact for high integration, yet face their own problems as well, including a weak optical nonlinearity, the lack of suitable configurations for photonic hardware, and proper optical storage mediums. In this Perspective, we highlight the recent advancements of IPNNs in China from aspects of different proposed configurations for photonic hardware, implementations of on-chip optical nonlinear activations, and training methods of IPNNs, and we also discuss some next challenges still ahead to realize high performance IPNNs with strong computing power.

CONFIGURATIONS FOR IPNNS

IPNNs display the possibility of miniaturizing and integrating with current computational devices. The on-chip integrated photonic platform provides promising configurations available for computation with great scalability, high computational density, and easy fabrication. Although simple structures such as fixed couplers are often explored on a larger scale, they are usually of lower density and are hard to expand to adapt to conventional requirements. Thus, more compact, novel structures suitable for photonic hardware are being actively explored. Here, we focus on several representative configurations developed in recent years.

On-Chip Waveguide-Based IPNNs. On-chip waveguides are the core structures of integrated photonics. The simplest way to utilize waveguides for computation is by using fixed couplers as Mach−Zehnder interferometers (MZIs) and phase shifters with a strong electro-optic effect/thermo-optic effect/all-optical nonlinear effect. The combination of two arms of the coupler with different phase modulations converts phase modulation into intensity modulation, enabling optical computation equivalent to complex addition and multi-

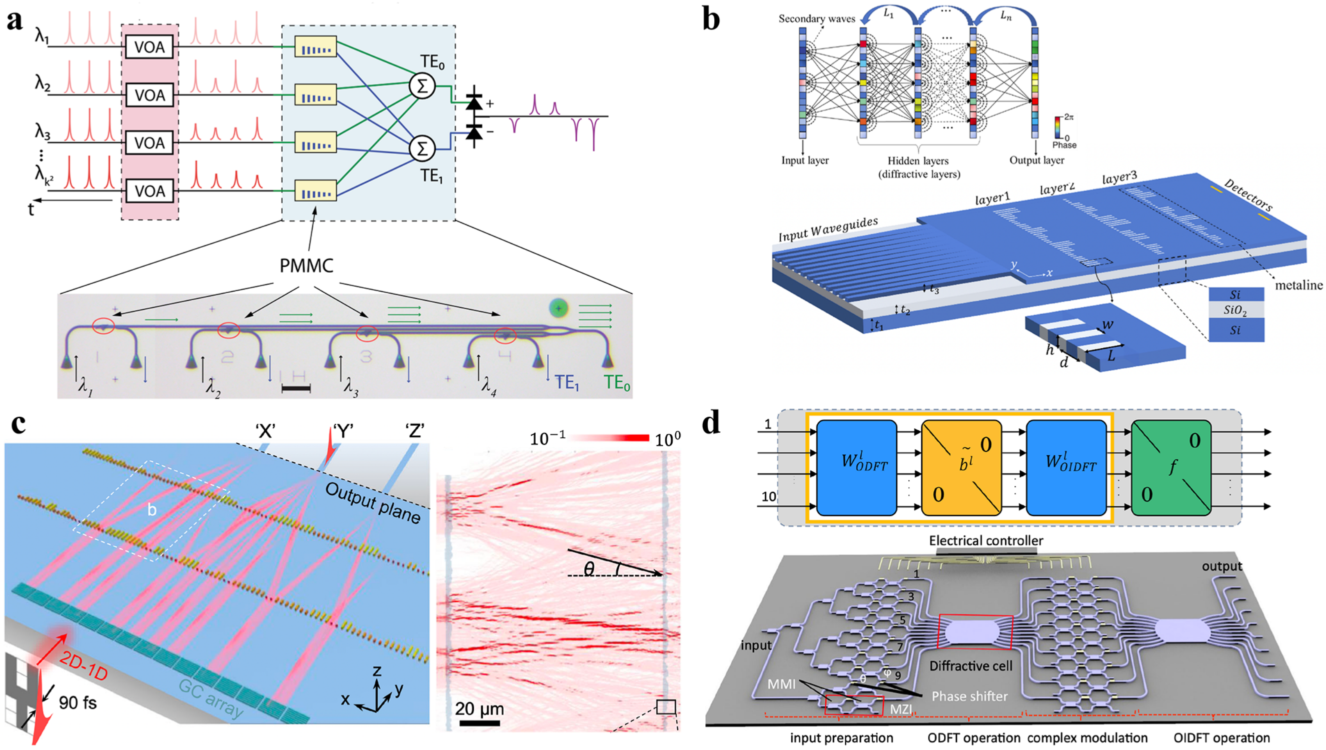

Figure 2. On-chip dielectric metasurface-based IPNNs. (a) Schematic of optical convolution for image processing. A patch of pixels of an image is encoded as optical pulses; the output in TE$_0$ and TE$_1$ are summed incoherently and measured with photodetectors (top). Optical microscope image of the photonic core consisting of four PMMCs with four input channels (bottom). Reprinted with permission from ref 76. Copyright 2021 Springer Nature. https://creativecommons.org/licenses/by/4.0/. (b) Schematic of diffractive ONN: each point on a given layer acting as a secondary source of a wave (top). Each of the three slots on a given layer act as a neuron with a complex-valued transmission coefficient (bottom). Reprinted with permission from ref 77. Copyright 2021 Optical Society of America. https://creativecommons.org/licenses/by/4.0/. (c) Schematics of the 1D multilayer diffractive metasurface system. As an example, a pattern "Y" with less than 90 fs pulse duration is coupled to the integrated metasystem through the input grating coupler array (left). Subwavelength structure manifested diffraction between metasurface layers (right). Reprinted with permission from ref 78. Copyright 2022 Springer Nature. https://creativecommons.org/licenses/by/4.0/. (d) Schematic of the IDNN operates on complex-valued inputs using coherent light (top). Schematic of the experimental device with four functional parts: input signal preparation; implementing ODFT operation; modulating amplitude/phase in the Fourier domain; implementing OIDFT operation (bottom). Reprinted with permission from ref 79. Copyright 2022 Springer Nature. https://creativecommons.org/licenses/by/4.0/.

plication. Different from neural network in electronic computers, where the weight values and intermediate results are not bounded, the optical signals propagating through waveguides must follow the rules of energy conservation, putting additional limits on the function of the IPNNs.

In 2016, Zhou et al. proposed an optical switch with a large number of channels,[53] as shown in Figure 1a. which functions with the equivalence of a neural network in binary values. Yet this device may not fully take advantage of the low noise of optical waveguides, as it supports more precision than binary signals. In 2017, Soljačić et al. proposed a new architecture for a fully optical feed-forward neural network,[54] as shown in Figure 1b, which contains 56 programmable MZIs using analog light signals for computation. The authors demonstrated its utility for vowel recognition with a computational ability equivalent to a 4 × 4 matrix multiplication. However, available space on the device for holding the controlling electrodes limits further scaling of the device channels. Besides, the weight of the network was trained via computer simulation, then configured by manual operation, which is time-consuming and becomes a serious challenge when the network is expanded to a larger scale. Note that they also discussed the feasibility of on-chip optimization with the gradient of weights based on the forward propagation. Based on a similar structure, Dong et al. proposed a silicon photonic signal processor in 2020, which also functions as the linear layer for a neural network, with capabilities of dynamically configuring the functions for reconfigurable processors, as shown in Figure 1c. The proposed structure contains 48 phase shifters and 20 MZIs, demonstrated with three functions, including multi-channel optical switching, optical multiple-input-multiple-output descrambler, and a tunable optical filter.[55] Such networks demonstrate the possibility of IPNNs to meet the requirements of simple computing tasks, but the most widely deployed artificial neural networks are in computer vision tasks, where a substantially larger number of channels are required. In 2021, Hu et al. proposed an advanced photonic neural network with 27 channels and a structural resemblance of the convolutional neural network,[56] as demonstrated in Figure 1d. This scheme can extend the functions to realize transcendental equation solvers, multifunctional logic gate operators, and half-adders, with better scalability capabilities. However, although this configuration contains three layers, it is not an orthogonal representation of the neural network, as there is a lack of nonlinear activation function. Details about integrated optical activation functions will be further discussed in the later section. But it is worth noting that in 2022, Hu et al. demonstrated a five-layer integrated locally connected

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photonic neural network with an all-optical saturated absorption nonlinear activation layer,[57] as shown in Figure 1e. This network contains an activation layer after the second linear layer, allowing it to deal with complex tasks such as solving for the eigenvalues of a matrix.

As for now, however, even the best optimized MZI structures are hard to directly scale up for conventional usage. If we count one MZI to match a single float point operation, a typical neural network would take at least 1 billion to be functional,[58,59] which is not applicable with any type of MZI design due to the amount of phase shifters used to control the MZIs. In addition, conventional neural networks usually contain dozens of layers.[60−63] as for the scheme of all-optical activation, strong optical nonlinearity results in strong energy loss, leading to almost no output with the same depth in an IPNN with current structural patterns, unless some external optical pumping is applied to the system.

On-Chip Dielectric Metasurface-Based IPNNs. Large-scale, highly integrated, low-power hardware is becoming increasingly important for realizing IPNNs with advanced optical computing capabilities. Traditional MZIs have limited scalability and consume excessive power. Here, the optical metasurfaces offer new possibilities for realizing light−matter interactions by compressing the light fields at subwavelength scales.[64−67] First, it is worth noting that functional optical computing components based on metasurfaces have been reported, such as computational imaging[68] and compact logic operator.[69] Then, it is also of great research significance to use metasurfaces to replace the components of traditional chips for computing.[70,71] Moreover, machine learning may enrich the metasurface devices by exploiting machine-learning techniques for improving optical system design and hardware.[72,73] Optical on-chip dielectric metasurfaces, as artificially designed electromagnetic interfaces,[74,75] can manipulate the degree of freedom of on-chip optical signal transmission, and they have the potential to realize on-chip integrated photonic computing with a compact footprint, broadband, and low loss. In recent years, a series of research work on PNNs based on integrated metasurface platforms has been gradually reported, with the feature structures interpreted as neurons with dense coupling, with the ability to stack multiple computations in limited footprints.

In 2021, Li et al. demonstrated a multimode photonic computing core,[76] which is a metasurface programmable waveguide mode converter based on phase-change material $Ge_2Sb_2Te_5$ (GST) to achieve phase gradient control. This phase-change metasurface mode converter (PMMC) exploits the large refractive index change of the GST during the phase transition to control the switching of the two spatial modes of the waveguide, TE_0 and TE_1 modes. A 2 × 2 PMMC array (Figure 2a) was built and used as a programmable kernel to implement a multimodal optical convolutional neural network. It can perform image processing and recognition tasks with high precision. This multimode photonic core, with a wide operating bandwidth and a compact device footprint, holds promise for large-scale PNNs with ultrahigh computational throughput. In 2021, Cheng et al. proposed a PNN composed of 1D multilayer diffractive metasurfaces,[77] as shown in Figure 2b. They considered the difference in the effective refractive index of the same slit at different positions for light input at different angles and the mutual interference between adjacent grooves of different lengths for the input light at the same angle. Thus, three silicon slots were used as a single neuron, thereby minimizing the impact of the above two factors and making the phase delay induced by the silicon slot more accurately approximate the value of the pretrained neuron. This scheme has a simple structure design, and the manufacturing process is compatible with the CMOS process, which is convenient for large-scale and low-cost manufacturing. Similarly, in 2022, Gu et al. experimentally fabricated and demonstrated this 1D multilayer diffractive metasurface system,[78] which was fabricated on SOI substrates by one-step lithography and etching (Figure 2c). The demonstrated spatial pattern classifier in a two-layer metasystem achieves accuracies of 92% and 89% under narrowband continuous wave excitation and broadband femtosecond pulse excitation, respectively. The proposed diffractive element system provides an alternative machine learning architecture for photonic integrated circuits. In 2022, Liu et al. demonstrated a silicon-based scalable integrated diffractive neural network consisting of two ultracompact diffractive units and N MZIs for parallel Fourier transform, convolution operations, and optical calculations for specific applications,[79] as shown in Figure 2d. The adopted on-chip compact diffractive unit enables the footprint and power consumption of the proposed architecture to be reduced from quadratic scaling to linear scaling of the input data dimension required for MZI-based PNN architectures. This solution contributes to the realization of energy-efficient, ultracompact, and large-scale integrated optical computing chips.

Given that on-chip dielectric metasurfaces as a unique way to manipulate the degrees of freedom of on-chip light fields demonstrate efficient, compact optical connections for IPNNs and are compatible with on-chip CMOS fabrication processes, they provide a feasible way for the efficient implementation of neural networks on integrated photonic platforms.

Integrated Photonic Spiking Neural Networks. Spiking neural networks (SNN),[80,81] which compute with light pulses instead of steady beams, tell a different story from the network configurations mentioned above. Such networks do not require a large array of unit devices, as signals can propagate through the structure multiple times and are a closer resemblance to how neurons generate electrical pulses based on membrane voltage.

The spiking neuron has several typical characteristics: (i) The spiking neuron only emits an output pulse when the power of the perturbation signal exceeds a certain threshold. (ii) The spiking neuron can be excited with several sufficiently closely spaced subthreshold pulses by integrating their combined perturbation. (iii) After an excitation, the neuron needs to relax to its steady-state before it can be triggered again. (iv) The output spike of the previous neuron should be strong enough to excite the next neuron, which is the foundation of forming a multilayer SNN. (v) The arrival of a stimulus can stop the spiking activity, which plays an important role in the spike-timing-dependent plasticity (STDP) learning rules.[82] Photonic synapses should meet these requirements to be able to construct a photonic spiking neural network.

In 2021, Wang et al. proposed a mechano-photonic artificial synapse implemented with a graphene/MoS_2 heterostructure and an integrated triboelectric nanogenerator.[83] This artificial synapse is capable of generating spiking patterns by controlling the charge transfer/exchange between the graphene and the MoS_2 layer. Moreover, other features, such as postsynaptic photocurrents, persistent photoconductivity, and photosensitivity, are controlled by the triboelectric potential. In 2021,

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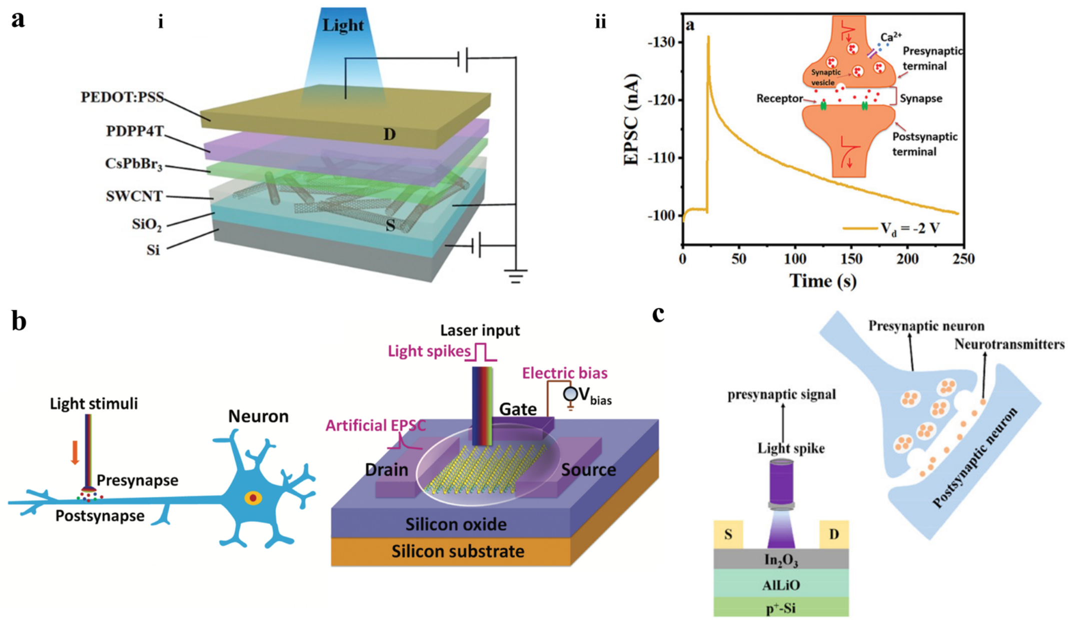

Figure 3. Integrated photonic spiking neural networks. (a) (i) 3D schematic of the vertical organic field-effect transistors device, where PDPP4T and $CsPbBr_3$ QDs are sandwiched between the source-drain electrodes. (ii) EPSC (excitatory postsynaptic current) triggered by a presynaptic light spike. The inset shows a schematic diagram of the EPSC generation process in biological synapses. Reprinted with permission from ref 84. Copyright 2021 John Wiley and Sons. (b) Schematic image of a neuron subject to light stimuli (left) and a schematic of the photonic MoS_2 synapse (right). Reprinted with permission from ref 85. Copyright 2019 Royal Society of Chemistry. (c) Schematic diagram of the device and synapse, where the UV light spike is considered as the presynaptic signal. Reprinted with permission from ref 86. Copyright 2020 American Chemical Society.

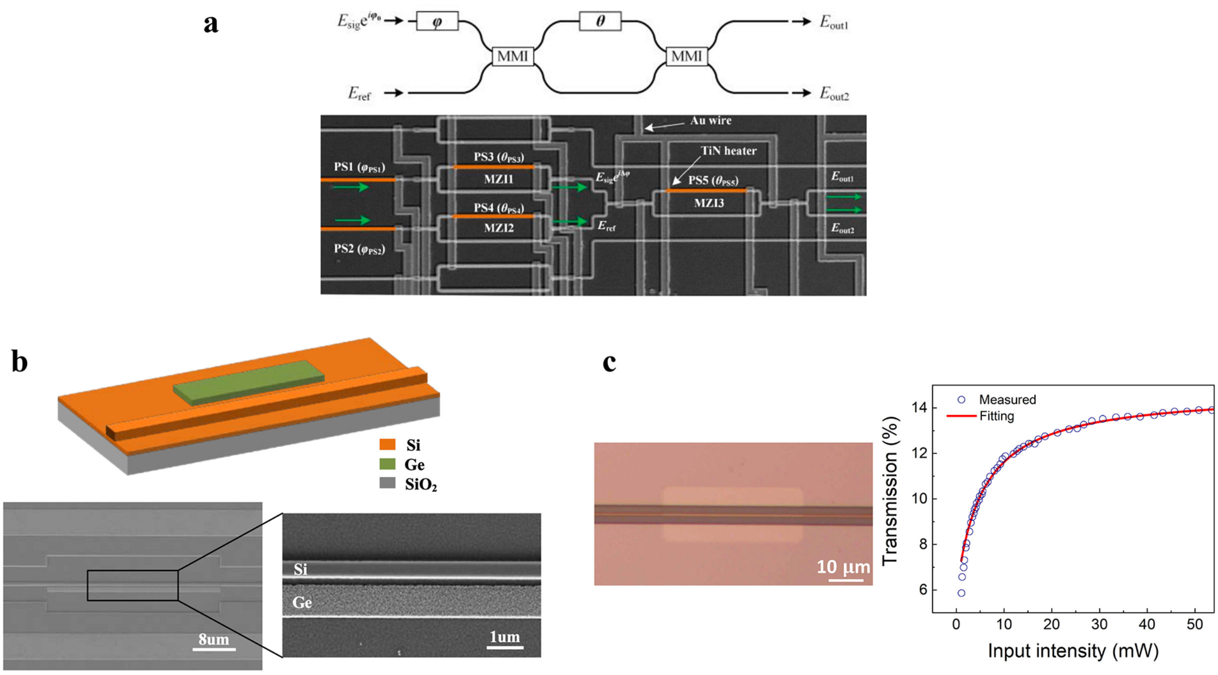

Figure 4. Implementations of on-chip optical nonlinear activations. (a) Optical nonlinear circuit based on a programmable MZI (top). Micrograph of the on-chip circuit (bottom). Reprinted with permission from ref 94. Copyright 2020 The Authors. (b) The schematic diagram of the optical activation function device (top). SEM image of fabricated device (bottom). Reprinted with permission from ref 96. Copyright 2022 IEEE. (c) The optical nonlinear activation layer of single-layer graphene covered on the silicon waveguide with the length of 40 μm: the optical micrograph of the optical nonlinear activation cell (left). The transmission curve with fitting parameters of saturated absorption effect of α_S = 0.088, α_{NS} = 0.852, and I_s = 5.446. Reprinted with permission from ref 57. Copyright 2022 De Gruyter. https://creativecommons.org/licenses/by/4.0/.

Huang et al. proposed a type of optical synapse based on vertical organic field-effect transistors,[84] as shown in Figure 3a. This scheme shows superior low-voltage capabilities, allowing for an obvious response with 1.3 fJ per spike. Another kind of

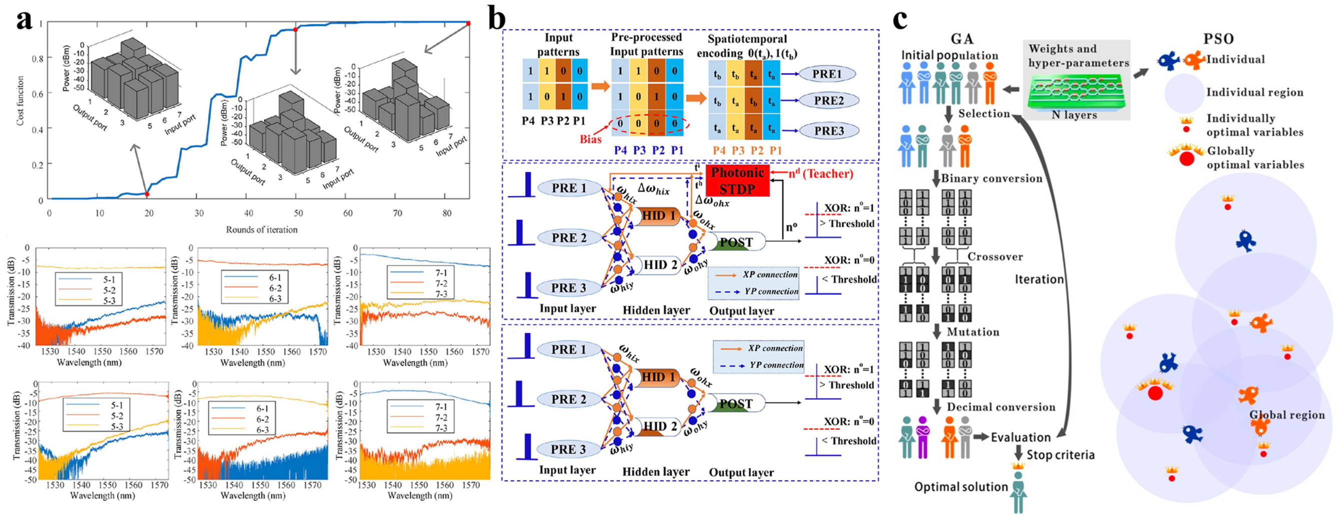

Figure 5. Training methods of IPNNs. (a) Cost function dependent on the rounds of iteration in training process (top). Transmission spectra for the signal and noise of the optical links in the shown routing states (bottom). Reprinted with permission from ref 55. Copyright 2020 American Chemical Society. (b) The architecture of the proposed multilayer photonic SNN for solving the XOR task. Reprinted with permission from ref 97. Copyright 2019 Optical Society of America. https://creativecommons.org/licenses/by/4.0/. (c) The flowcharts of the learning algorithms for the ONNs based on GA and PSO algorithms. Reprinted with permission from ref 98. Copyright 2021 IEEE.

optical synapsis is integrated with electrical ones, where in 2019, Wan et al. proposed a photoelectronic hybrid-integrated synaptic device based on a 2D MoS_2 phototransistor gated by an electric double-layer biopolymer electrolyte (Figure 3b).[85] This synapse is functional with both the synaptic potentiation and depression effects, enabling a dynamic transition from a high-pass to a low-pass photonic filter, showing flexibility for computation. Although not entirely required, a better function for the artificial optical synapse would require a shift between short-term and long-term memories, which in 2020, Zhang et al. proposed an all-inorganic light-stimulated In_2O_3/AlLiO thin-film transistor,[86] as shown in Figure 3c. This artificial synapse achieved a simulation of the associative learning behaviors under light stimulation.

However, with promising abilities, none of these spiking synapses shown above are incorporated in an actual neural network outside of simulation, and experimental testing of the designed network configuration is yet to be demonstrated. In summary, the proposed spiking synapses are in a much more primary state and would require extensive research to catch up with other approaches.

IMPLEMENTATIONS OF ON-CHIP OPTICAL NONLINEAR ACTIVATIONS

The implementations of IPNNs mentioned above are purely linear in nature, which limits the computational power of such devices to be a single matrix multiplication from inputs to outputs. On electronic computers, a nonlinear activation function is usually applied after each linear layer,[87,88] similar to neurons.[89−91] For deeper structures, nonlinear activation is vital for higher performance.[92,93] In recent years, some nonlinear elements have been proposed for nonlinear activation layers of IPNNs, including thermo-optic modulation schemes, electro-optic modulation schemes, and all-optical nonlinear modulation schemes.

In 2020, Tian et al. proposed and experimentally demonstrated a thermo-optic modulated reconfigurable MZI-based on-chip optical nonlinear unit for ONN,[94] as shown in Figure 4a, which does not require optical-electrical conversion or high input power. This nonlinear unit can be reconfigured to perform multiple types of nonlinear activation functions, making it one of the candidate scheme for future ONNs. In 2022, Chu et al. proposed a mechanism for programmable low-threshold optically controlled nonlinear activation function based on integrated on-chip Ge−Si photodetectors and silicon photoswitches.[95] They experimentally change of the slope of the nonlinear activation function by adjusting the photodetector bias voltage, validating the generation of linear unit (ReLU) and sigmoid functions at a low threshold power of 0.2 mW. They claim that these devices are suitable for low-power ONNs. In 2022, Dong's group proposed an all-optical realization of a nonlinear activation function based on the hybrid integration of germanium (Ge) and silicon by using the plasmonic dispersion effect and carrier absorption effect of Ge at 1550 nm (Figure 4b).[96] This scheme has a large operating bandwidth with the response frequency of 70 MHz, a low loss of 4.28 dB, and a low threshold power of 5.1 mW. In 2022, Hu's group proposed and experimentally verified the performance of a single-layer graphene with optical nonlinear saturable absorption effect covered on a silicon waveguide as a nonlinear activation layer in an on-chip integrated locally connected photonic neural network (Figure 4c).[57] Compared with the configuration without the proposed nonlinear layer, there is about 30% improvement in accuracy in the task of solving the eigenvalues of second-order real symmetric matrices. This work lays the foundation for a new generation of intelligent on-chip integrated all-optical computing.

In general, the successive advent of various types of activation functions with reconfigurable, low power consumption, high bandwidth, and low loss provide a solid foundation for the further development of on-chip IPNNs with powerful computing power.

TRAINING METHODS OF IPNNS

For IPNNs with steady optical inputs and outputs, the network is usually trained with gradient descending methods. For

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neural networks in computers, given the relationship between network weights and outputs, it is easy to obtain the gradient of weights used for minimizing the loss value. Using such gradient values, by applying various gradient descent methods, the network weights are adjusted step by step toward higher performance.[88] There are two approaches in obtaining the gradient value. The first approach is to use numerical methods to simulate the IPNN, and compute the gradient via the simulation. With this method, the simulated network is trained on a computer, with the optimized network weights applied on the physical network after training. The second approach is to obtain the gradient by experimentally measuring the difference in network output after modifying the network weight by a small value, using this to conduct on-chip training.[54]

In 2020, Dong et al. proposed and experimentally verified a self-configuring and reconfigurable silicon photonic signal processor. All functions are programmed through self-configuration without any internal structure information by using the deep learning improved numerical gradient descent algorithm,[55] as shown in Figure 5a. For IPNNs that work in a spiking pattern, an entirely different approach for training is used, namely, the spike timing dependent plasticity method, which optimizes the spiking neurons based on the past record of how often their activities coincide. In 2019, Xiang et al. applied this method in training simulated spiking ONNs built by using a vertical-cavity, surface-emitting laser with an embedded saturable absorber,[97] as shown in Figure 5b. This algorithm is tested on the classical XOR task, with only two inputs and one output. Another method that is available for training IPNNs is neuroevolution, derived from the evolution process that imitates the biological brain, which generates a group of networks, picks out the better networks, and uses them to generate the next group. In 2021, Xu et al. proposed neuroevolution methods for training IPNNs, as shown in Figure 5c. They showed the calculated results support the fact that these training algorithms are competitive with gradient-based learning algorithms.[98]

■ CONCLUSION AND OUTLOOK

In this Perspective, we have highlighted the recent advancements of IPNNs from several aspects which have been continuously concerned. Despite the promising potentials in high speed and high energy efficiency computation, IPNNs still face challenges concerning the scalability to meet requirements for real-world tasks. (1) As the main configuration, on-chip MZIs are difficult to scale up to computer vision and other tasks that require a large number of inputs. (2) On-chip metasurface-based IPNNs come with much more compact optical connections and efficient computation, while it is hard to optimize the specified high-dimensional transfer matrix and hard to achieve reconfiguration of weight parameters for all degrees of freedom. (3) Spiking networks with neuromorphic designs demonstrate excellent results by using temporal encoding of input meeting with these challenges. However, they are in a much more primary state and still need sufficient experimental demonstration of the full network configuration. (4) As for the on-chip optical nonlinear activation functions, various types of activation functions have been successively reported. In order to achieve an effective increase in computing power, it is necessary to continue to develop optical activations with reconfigurability, low power consumption, high bandwidth, and low loss. Especially, as for the all-optical activations utilizing the third-order nonlinear effect of materials, the dissipation of energy indicates that a full optical activation will run out of energy after a rather shallow depth. The solution to this lies in either some way to refill the energy or to develop optical nonlinearity with an independence to optical intensity. (5) In addition, the training of IPNNs still relies on simulation, but a stable and efficient scheme of on-chip training is yet to be realized. The efficient combination of novel configurations specified for the integrated photonic platform with light-field-driven nonvolatile materials will hopefully address this challenge.

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Notes

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