CUSTOM MICROBLAZE SYSTEM

FEATURES	DESCRIPTION
CORE	MICROBLAZE
PROCESSOR IMPLEMENTATION	32 BIT
INSTRUCTION MEMORY SIZE	64KB
DATA MEMORY SIZE	64KB
FLOATING POINT UNIT	PRESENT(BASIC)
AXI GPIO	PRESENT(2)
AXI UART	PRESENT(2)
AXI IIC	PRESENT(1)
AXI QUADSPI	PRESENT(1)

SPECIFICATION

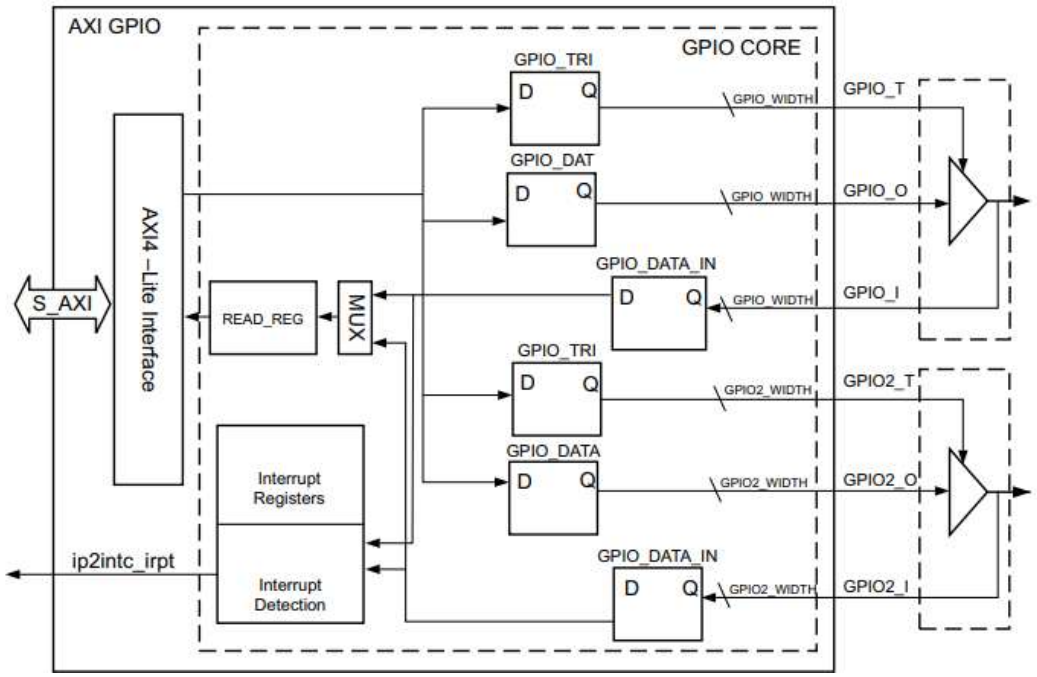
PERIPHERALS	ADDRESS	SIZE	INSTANCE NAME	COMMENT
GPIO_0	0x4000_0000-0x4000_FFFF	64K	axi_gpio_0/S_AXI	Pushbutton-rgb led control
GPIO_1	0x4100_0000-0x4100_FFFF	64K	axi_gpio_1/S_AXI	Dip switches-4 bit led
UART_0	0x4200_0000-0x4200_FFFF	64K	axi_uartlite_0/S_AXI	usb UART
UART_1	0x4300_0000-0x4300_FFFF	64K	axi_uartlite_1/S_AXI	usb UART
SPI	0x4400_0000-0x4400_FFFF	64K	axi_quad_spi_0/S_AXI_LITE	Quad SPI
IIC	0x4500_0000-0x4500_FFFF	64K	axi_iic_0/S_AXI	Axi IIC
AXI	0x4120_0000-0x4120_FFFF	64K	microblaze_0_axi_intc/S_AXI	AXI Interrupt controller

MEMORY MAP

MEMORY/BUS	ADDRESS	SIZE	COMMENT
ILMB (FLASH)	0x0000_0000-0x0000_FFFF	64K	Instruction memory
DLMB(RAM)	0x1000_0000-0x1000_FFFF	64K	Data memory
AXI BRAM(EXTERNAL)	0xc000_0000-0xc000_1FFF	8K	External memory

AXI GPIO v2.0

AXI GPIO Block Diagram



Product Specification

Parameter Values (Other Parameters at Default Value)				Device Resources		
Enable Dual Channel	Enable Interrupt	GPIO Width	GPIO2 GPIO Width	Slices	Flip-Flops	LUTs
0	0	32	32	34	174	124
0	0	16	32	21	94	72
0	1	32	16	40	179	135
0	1	32	32	36	179	135
0	1	1	1	9	24	28
1	0	32	32	66	302	230
1	0	1	1	8	23	25
1	0	5	28	40	174	134
1	0	28	5	41	174	131
1	1	32	32	65	307	249
1	1	15	28	52	219	171
1	1	1	1	12	28	33

Resource Utilization for 7 Series FPGAs

Port Descriptions

Signal Name	Interface	I/O	Initial State	Description
s_axi_aclk	Clock	I		AXI Clock.
s_axi_aresetn	Reset	I		AXI Reset, active-Low.
s_axi_*	S_AXI	NA	-	AXI4-Lite Slave Interface signals. See Appendix A of the *Vivado AXI Reference Guide* (UG1037) [Ref 3] for AXI4, AXI4-Lite and AXI Stream Signals
ip2intc_irpt	System	O	0	AXI GPIO Interrupt. active-High, level sensitive signal.
gpio_io_i (1)(3)	GPIO	I		Channel 1 general purpose input pins. Width of this port is configurable based on **GPIO Width**.
gpio_io_o(2)(3)(4)	GPIO	O	0	Channel 1 general purpose output pins. Width of this port is configurable based on **GPIO Width**.
gpio_io_t(4)	GPIO	O	1	Channel 1 general purpose 3-state pins. Width of this port is configurable based on **GPIO Width**.
gpio2_io_i(1)(3)	GPIO	I		Channel 2 general purpose input pins. Width of this port is configurable based on **GPIO2 Width**.
gpio2_io_o(2)(3)(4)	GPIO	O	0	Channel 2 general purpose output pins. Width of this port is configurable based on **GPIO2 Width**.
gpio2_io_t(4)	GPIO	O	1	Channel 2 general purpose 3-state pins Width of this port is configurable based on **GPIO2 Width**.

AXI GPIO Registers

Address Space Offset[3]	Register Name	Access Type	Default Value	Description
0x0000	GPIO_DATA	R/W	0x0	Channel 1 AXI GPIO Data Register.
0x0004	GPIO_TRI	R/W	0x0	Channel 1 AXI GPIO 3-state Control Register.
0x0008	GPIO2_DATA	R/W	0x0	Channel 2 AXI GPIO Data Register.
0x000C	GPIO2_TRI	R/W	0x0	Channel 2 AXI GPIO 3-state Control.
0x011C	GIER[1]	R/W	0x0	Global Interrupt Enable Register.
0x0128	IP IER[1]	R/W	0x0	IP Interrupt Enable Register (IP IER).
0x0120	IP ISR[1]	R/TOW[2]	0x0	IP Interrupt Status Register.

AXI GPIO Data Register Description

Bits	Field Name	Access Type	Reset Value	Description
[GPIOx_Width-1 :0]	GPIOx_DATA	Read/Write	GPIO: Default Output Value GPIO2: Default Output Value	AXI GPIO Data Register. For each I/O bit programmed as input: • R: Reads value on the input pin. • W: No effect. For each I/O bit programmed as output: • R: Reads to these bits always return zeros • W: Writes value to the corresponding AXI GPIO data register bit and output pin.

AXI GPIO Three-State Register Description

Bits	Field Name	Access Type	Reset Value	Description
[GPIOx_Width-1 :0]	GPIOx_TRI	Read/ Write	GPIO: Default Tri State Value GPIO2: Default Tri State Value	AXI GPIO 3-State Control Register. Each I/O pin of the AXI GPIO is individually programmable as an input or output. For each of the bits: 0 = I/O pin configured as output. 1 = I/O pin configured as input.

Global Interrupt Enable Register Description

Bits	Name	Core Access	Reset Value	Description
31	Global Interrupt Enable	Read/Write	0	Master enable for the device interrupt output to the system interrupt controller: 0 = Disabled 1 = Enabled
30 – 0	Reserved	N/A	0	Reserved. Set to zeros on a read.

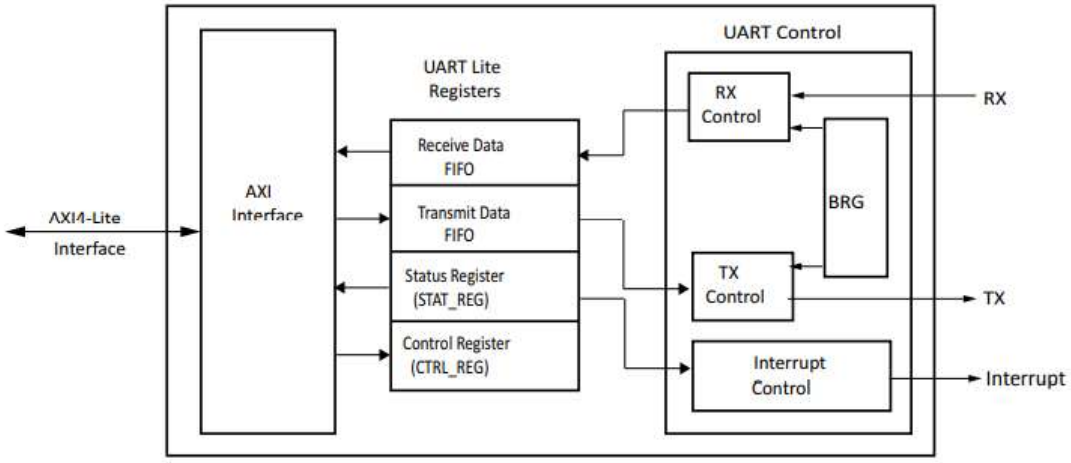
IP Interrupt Enable Register Description

Bits	Name	Core Access	Reset Value	Description
31–2	Reserved	N/A	0	Reserved. Set to zeros on a read.
1	Channel 2 Interrupt Enable	Read/Write	0	Enable Channel 2 Interrupt. 0 = Disabled (masked) 1 = Enabled
0	Channel 1 Interrupt Enable	Read/Write	0	Enable Channel 1 Interrupt. 0 = Disabled (masked) 1 = Enabled

IP Interrupt Status Register Description

Bits	Name	Core Access	Reset Value	Description
31–2	Reserved	N/A	0	Reserved. Set to zeros on a read.
1	Channel 2 Interrupt Status	Read/TOW(1)	0	Channel 2 Interrupt Status 0 = No Channel 2 input interrupt 1 = Channel 2 input interrupt
0	Channel 1 Interrupt Status	Read/TOW(1)	0	Channel 1 Interrupt Status 0 = No Channel 1 input interrupt 1 = Channel 1 input interrupt

AXI UARTLITE v2.0

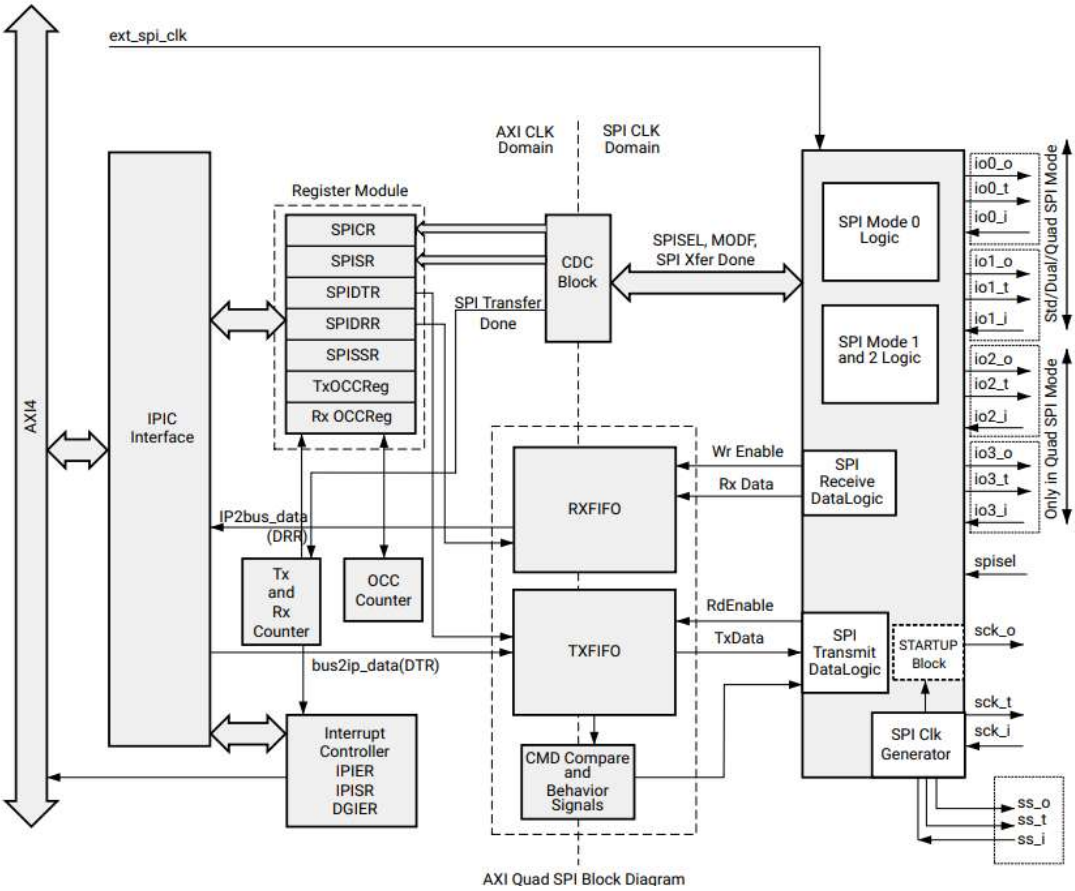


Block Diagram of AXI UART Lite

Register Address Map

Address Offset	Register Name	Description
0h	Rx FIFO	Receive data FIFO
04h	Tx FIFO	Transmit data FIFO
08h	STAT_REG	UART Lite status register
0Ch	CTRL_REG	UART Lite control register

AXI Quad SPI v3.2

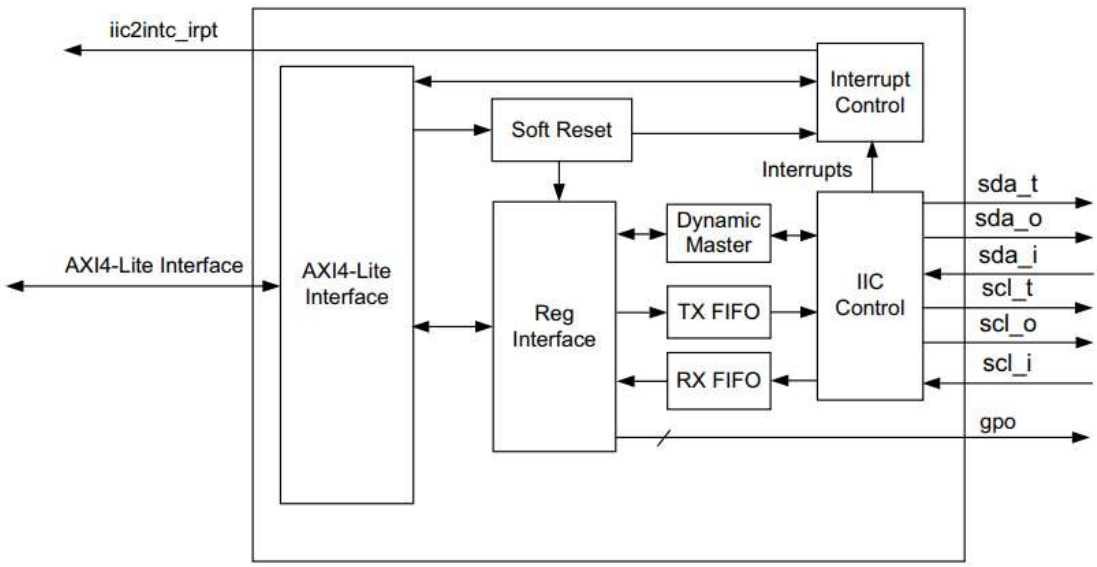


AXI Quad SPI Core Top-Level Block Diagram

Register Space

Address Space Offset	Register Name	Access Type	Default Value (hex)	Description
Core Grouping				
40h	SRR	Write	N/A	Software reset register
60h	SPICR	R/W	0x180	SPI control register
64h	SPISR	Read	0x0a5	SPI status register
68h	SPI DTR	Write	0x0	SPI data transmit register. A single register or a FIFO
6Ch	SPI DRR	Read	N/A(1)	SPI data receive register. A single register or a FIFO
70h	SPISSR	R/W	No slave is selected 0xFFFF	SPI Slave select register
74h	SPI Transmit FIFO Occupancy Register(2)	Read	0x0	Transmit FIFO occupancy register
78h	SPI Receive FIFO Occupancy Register(2)	Read	0x0	Receive FIFO occupancy register
Interrupt Control Grouping				
1Ch	DGIER	R/W	0x0	Device global interrupt enable register
20h	IPISR	R/TOW(3)	0x0	IP interrupt status register
28h	IPIER	R/W	0x0	IP interrupt enable register

AXI IIC Bus Interface v2.0



AXI IIC Bus Interface Top-Level Block Diagram

I/O Signal Descriptions

Signal Name	Interface	I/O	Initial State	Description
System Signals				
s_axi_aclk	System	I	–	AXI Clock
s_axi_aresetn	System	I	–	AXI Reset, active-Low.
iic2intc_irpt	System	O	0x0	System Interrupt output.
s_axi*	S_AXI	I	–	See Appendix A of the *Vivado AXI Reference Guide* (UG1037) [Ref 4] for a description of AXI4 signals.
IIC Signals				
sda_i	IIC	I	–	IIC Serial Data Input from 3-state buffer.
sda_o	IIC	O	0x0	IIC Serial Data Output to 3-state buffer.
sda_t	IIC	O	0x0	IIC Serial Data Output Enable to 3-state buffer.(1)
scl_i	IIC	I	–	IIC Serial Clock Input from 3-state buffer.
scl_o	IIC	O	0x0	IIC Serial Clock Output to 3-state buffer.
scl_t	IIC	O	0x0	IIC Serial Clock Output Enable to 3-state buffer. (1)
gpo	IIC	O	0x0	Configurable General Purpose Outputs.

AXI IIC Transmit FIFO

Bits	Field Name	Default Value	Access Type	Description
31:10	Reserved	N/A	N/A	Reserved
9	Stop	0	W	**Stop.** The dynamic stop bit can be used to send an IIC stop sequence on the IIC bus after the last byte has been transmitted or received.(2)
8	Start	0(1)	W	**Start.** The dynamic start bit can be used to send a start or repeated start sequence on the IIC bus. A start sequence is generated if the MSMS = 0, a repeated start sequence is generated if the MSMS = 1.(2)
7:0	D7 to D0	Indeterminate(1)	W	**AXI IIC Transmit Data.** If the dynamic stop bit is used and the AXI IIC is a master receiver, the value is the number of bytes to receive.(3)

AXI_IIC Receive FIFO

Bits	Field Name	Default Value	Access Type	Description
31:8	Reserved	N/A	N/A	Reserved
7:0	D7 to D0	Indeterminate(1)	R	IIC Receive Data

PIN MAPPING

GPIO Port	Bit Index	Signal	Direction	Board Component
`gpio_io_o[0]`	Bit 0	LED0	Output	LD0
`gpio_io_o[1]`	Bit 1	LED1	Output	LD1
`gpio_io_o[2]`	Bit 2	LED2	Output	LD2
`gpio_io_o[3]`	Bit 3	LED3	Output	LD3
`gpio2_io_i[0]`	Bit 0	SW0	Input	Switch 0
`gpio2_io_i[1]`	Bit 1	SW1	Input	Switch 1
`gpio2_io_i[2]`	Bit 2	SW2	Input	Switch 2
`gpio2_io_i[3]`	Bit 3	SW3	Input	Switch 3

Comparison between microblaze and vega processor

Feature	Custom MicroBlaze (single-core, 32-bit)	VEGA ET1031 / THEJAS32
ISA	Proprietary Xilinx MicroBlaze ISA (RISC-like, not open)	RISC-V RV32IM (open ISA, base integer + mul/div)
pipeline	5-stage, in-order	3-stage, in-order
Clock freq	100MHZ	100MHZ(ASIC)
ILMB	64K	256 KB SRAM or external flash
DLMB	64K	256 KB SRAM
External memory	AXI BRAM: 8 KB	External SPI flash for program storage
Caches	Optional I/D cache (Not enabled, but possible)	No cache (simple Harvard core)
Peripherals	2×GPIO, 2×UART, 1×SPI, 1×I²C, AXI INTC	3×UART, 3×SPI, 2×I²C, 3×Timers, 8×PWM, 32×GPIO, 4×ADC
Interrupt controller	AXI INTC, vectoring depends on config	Platform interrupt controller, up to 127 IRQs
Debugging	Xilinx SDK / Vivado, JTAG debug	Eclipse IDE, GDB/OpenOCD via JTAG
Toolchain	Xilinx Toolchain	VEGA SDK (based on GCC/LLVM for RISC-V)
Power Target	FPGA softcore → not optimized for low power	ASIC microcontroller → low power
Openness	Proprietary, tied to Xilinx FPGAs	Open RISC-V ISA, indigenous Indian design