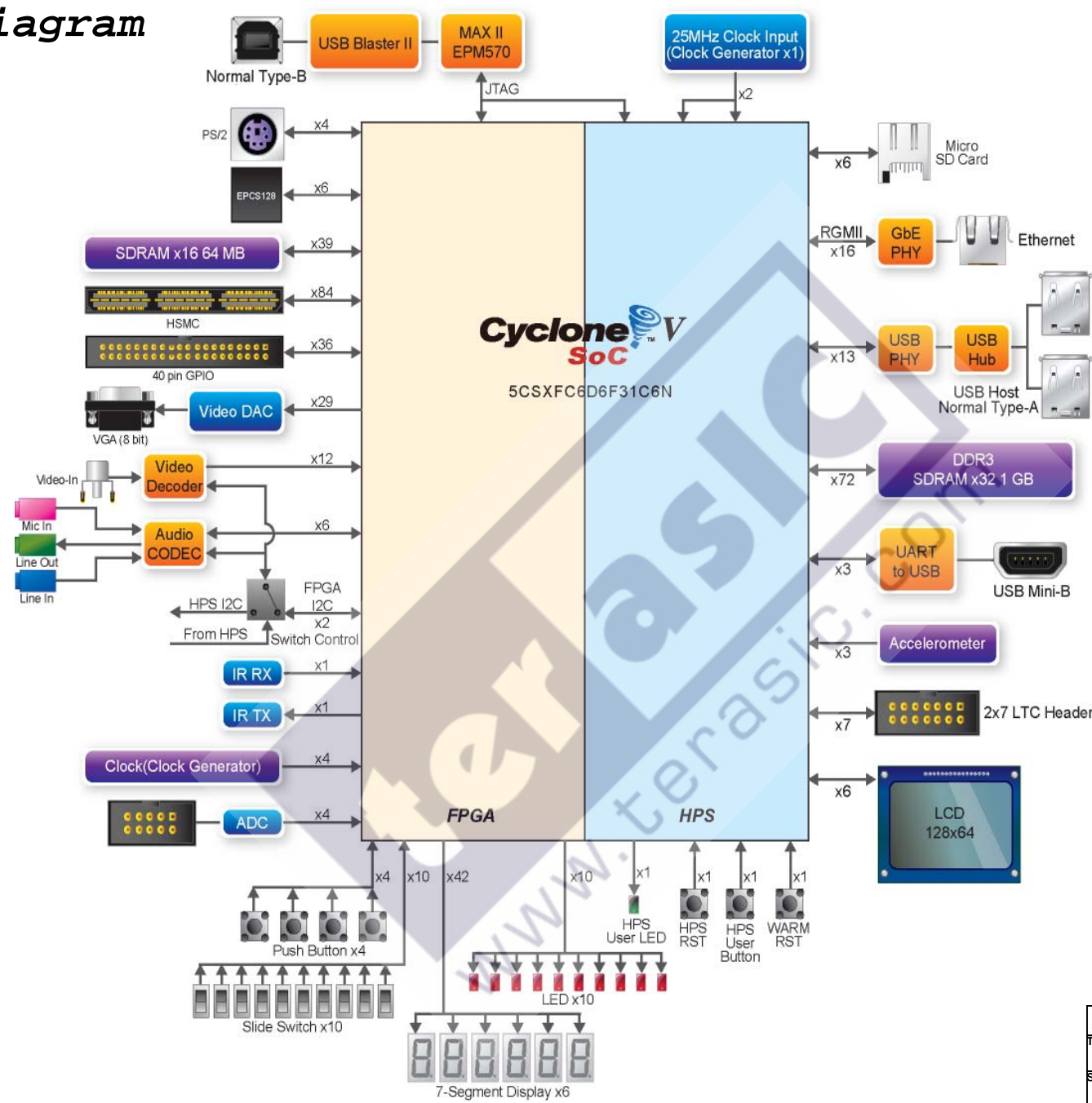
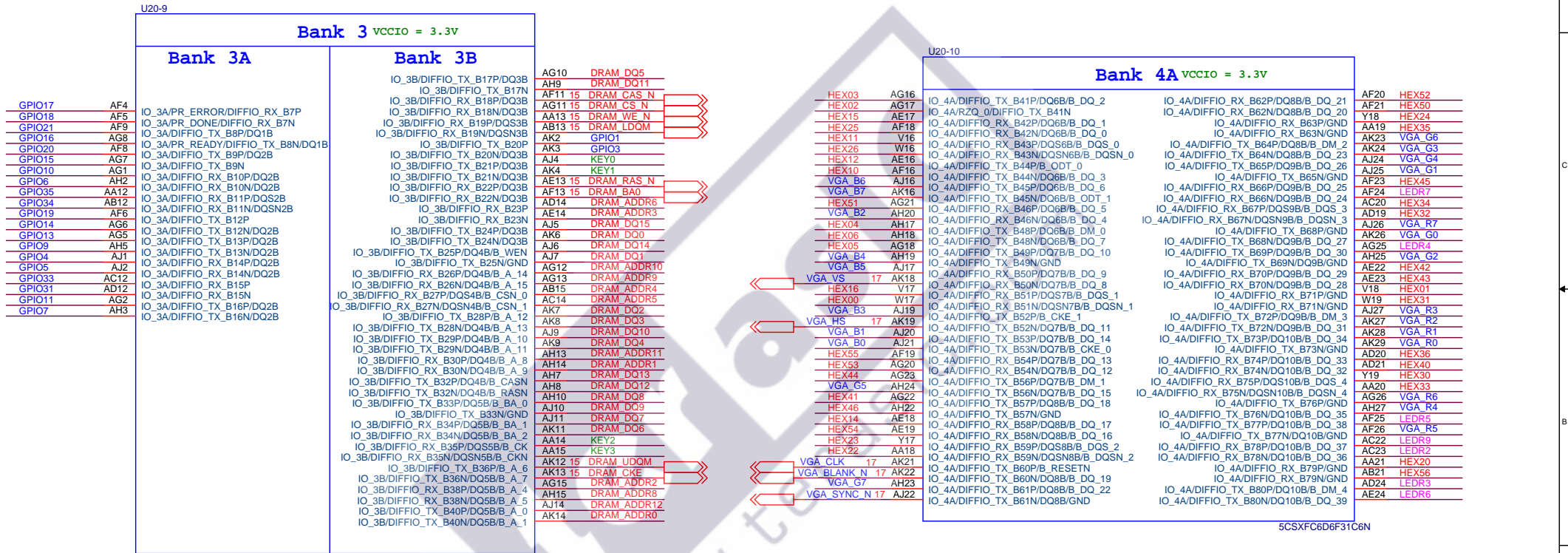


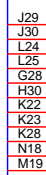
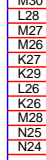
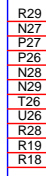
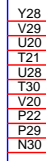
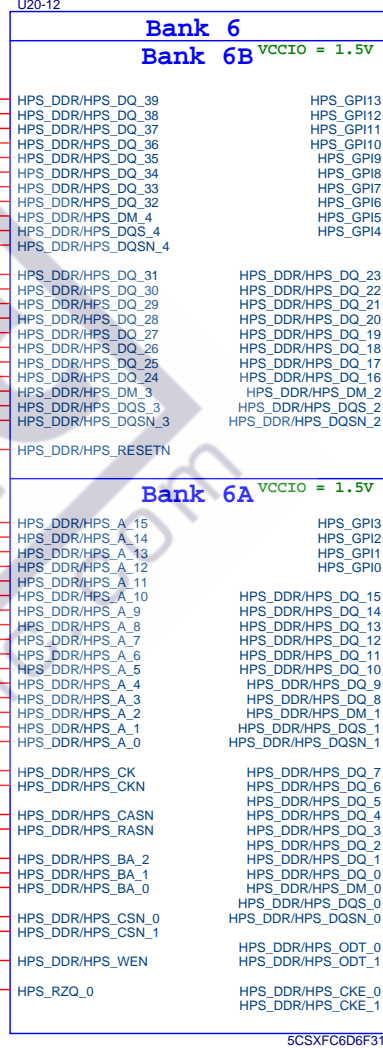
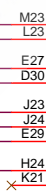
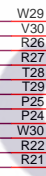
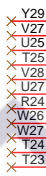
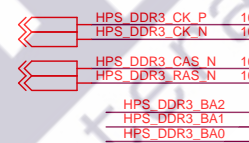
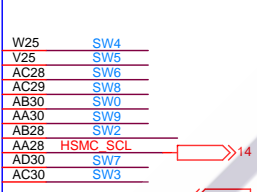
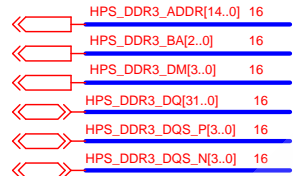
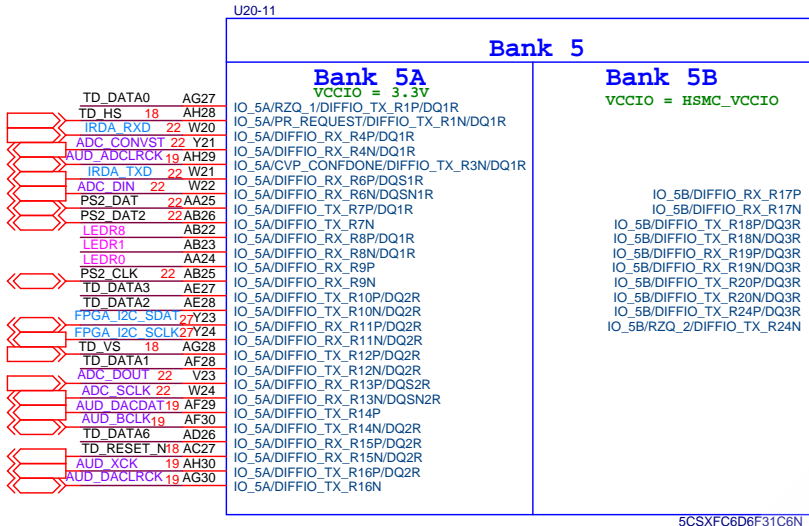
# ALTERA Cyclone V SoC Development & Education Board (DE10-Standard)

PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	18	ADV7180 Video Decoder
2	Block Diagram	19	Audio CODEC
3	FPGA BANK 3, BANK 4	20	7-Segment Display, LED
4	FPGA BANK 5, BANK 6	21	FPGA BUTTON, Switch
5	FPGA BANK 7, BANK 8	22	ADC, PS2, IR Tx, IR Rx
6	FPGA Clocks, GND	23	2-port USB Host
7	Transceiver	24	1 Gigabit Ethernet
8	FPGA Configuration	25	UART to USB, SD CARD
9	FPGA Decoupling	26	Accelerometer, LTC Connector
10	FPGA Power	27	I2C Multiplexer, HPS BUTTON, HPS LED
11	USB Blaster II	28	LCD
12	JTAG Chain	29	Power - 1.1V
13	GPIO	30	Power - 5V, 3.3V
14	HSMC	31	Power - 9V, 2.5V, 1.5V
15	SDRAM, HPS QSPI Flash	32	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT
16	HPS DDR3 SDRAM	33	Power - VCCIO_HSMC & HSMC_VCCPD
17	ADV7123 VGA		

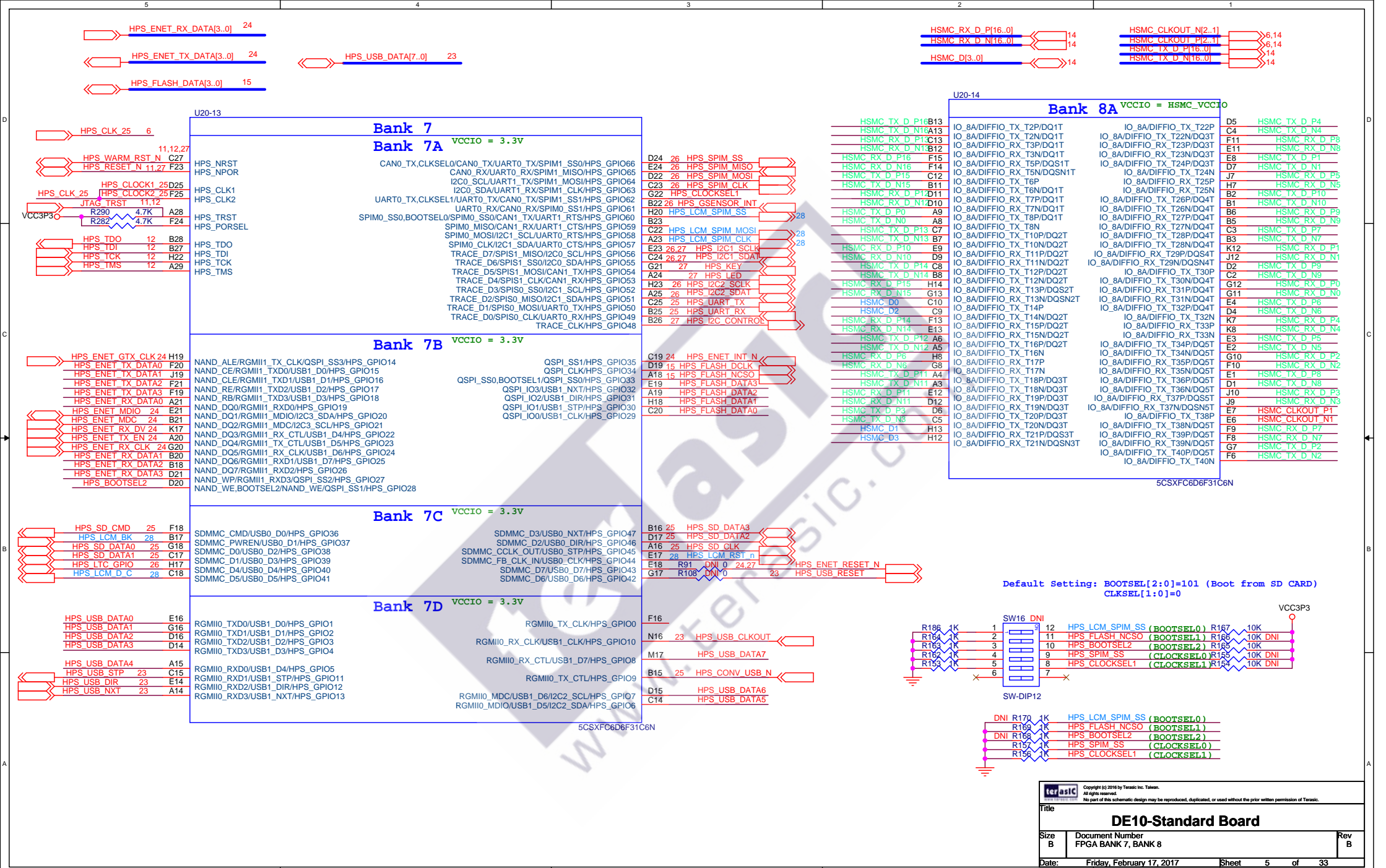
Block Diagram

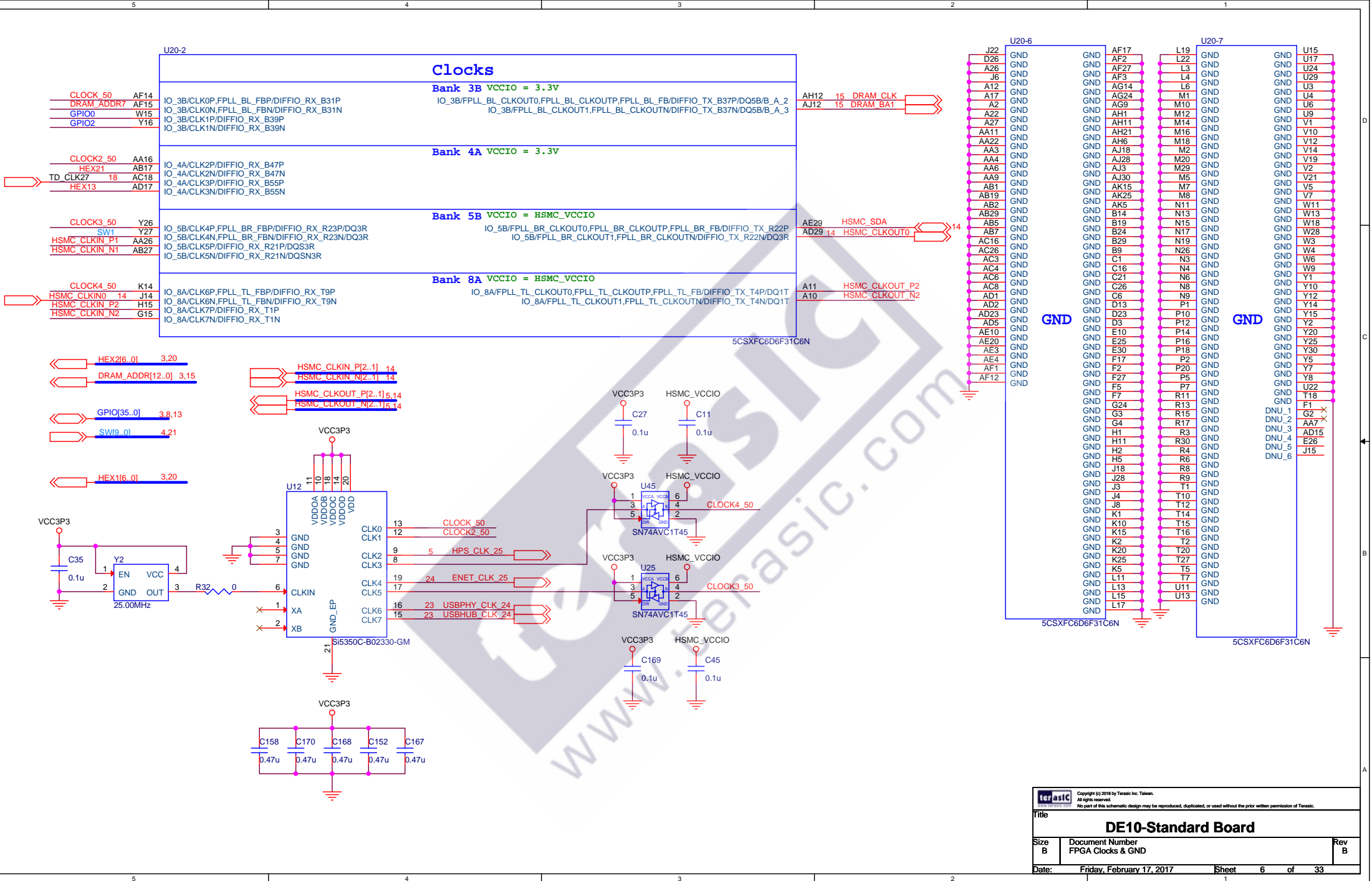


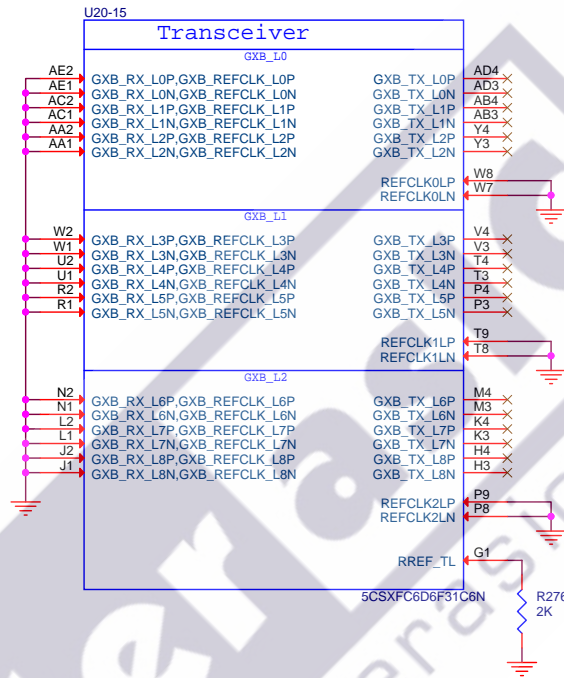









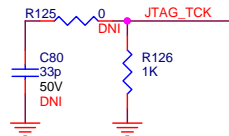




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Title		
DE10-Standard Board		
Size B	Document Number Transceiver	Rev B
Date:	Friday, February 17, 2017	Sheet 7 of 33

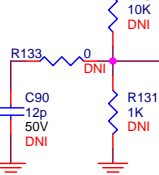
# USB Blaster

FPGA_TDI	12
JTAG_TMS	12
JTAG_TCK	12
FPGA_TDO	12



Design Note:  
Optional termination resistor  
for DCLK

CAD Note:  
Place near FPGA DCLK pin



JTAG_TCK	AC5	TCK
JTAG_TMS	V9	TMS
FPGA_TDO	AB9	TDO
FPGA_TDI	U8	TDI
EPCQ_DCLK	U7	DCLK
EPCQ_AS_DATA0	AE6	AS_DATA0/ASDO/DATA0
EPCQ_AS_DATA1	AE5	AS_DATA1/DATA1
EPCQ_AS_DATA2	AE8	AS_DATA2/DATA2
EPCQ_AS_DATA3	AC7	AS_DATA3/DATA3
EPCQ_NCSO	AB8	NCSO/DATA4
GPIO24	AE9	IO_3A/DATA5/DIFFIO_TX_B2N
GPIO26	AE12	IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B
GPIO28	AD9	IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B
GPIO30	AD11	IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B
GPIO22	AF10	IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B
GPIO29	AD10	IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B
GPIO25	AE11	IO_3A/DATA11/DIFFIO_TX_B4P
GPIO32	AC9	IO_3A/DATA12/DIFFIO_RX_B3P/DQ1B
GPIO8	AH4	IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B
GPIO23	AE7	IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B
GPIO12	AG3	IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B
GPIO27	AD7	IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B

### Configuration

Bank 3A VCCIO = 3.3V

Bank 5A VCCIO = 3.3V

IO\_5A/INIT\_DONE/DIFFIO\_RX\_R2P

IO\_5A/CRC\_ERROR/DIFFIO\_RX\_R2N

IO\_5A/DEV\_OE/DIFFIO\_TX\_R5P

IO\_5A/NCEO/DIFFIO\_TX\_R3P/DQ1R

IO\_5A/DEV\_CLRN/DIFFIO\_TX\_R5N/DQ1R

### Bank 9A

CONF\_DONE

NSTATUS

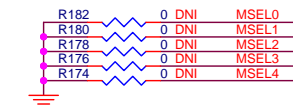
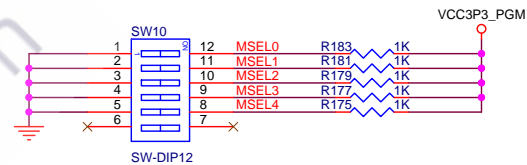
NCONFIG

NCE

5CSXFC6D6F31C6N

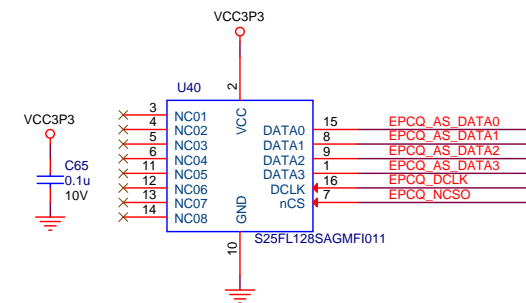
AD25	TD_DATA7
AC25	PS2_CLK2
AE26	TD_DATA4
AJ29	AUD_ADCDAT
AD27	TD_DATA5

Fix MSEL[4:0]=10010 in AS Fast Mode

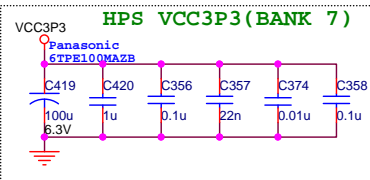
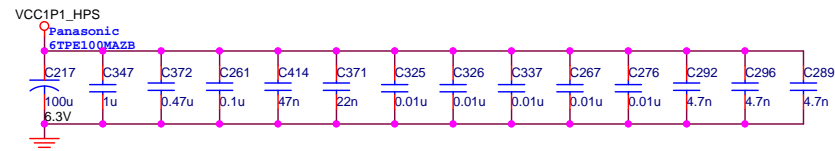
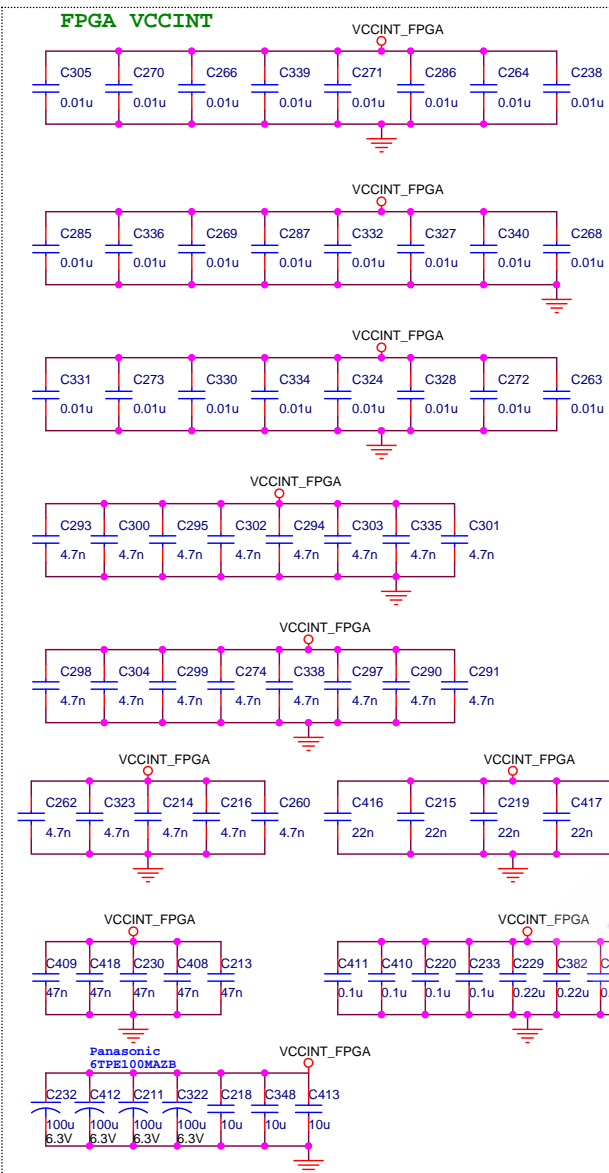


TD\_DATA[7..0] 4,18

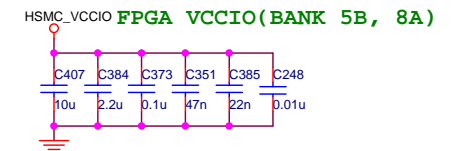
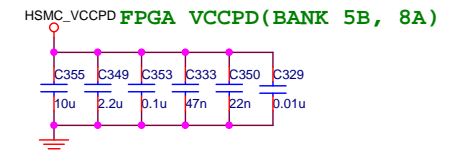
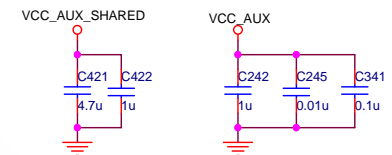
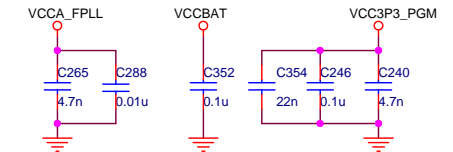
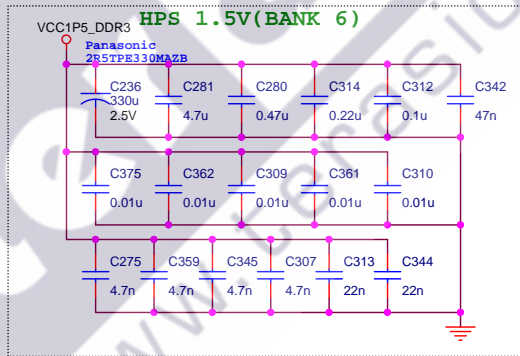
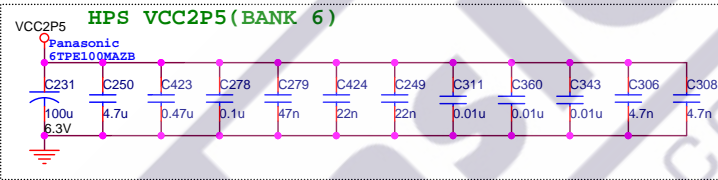
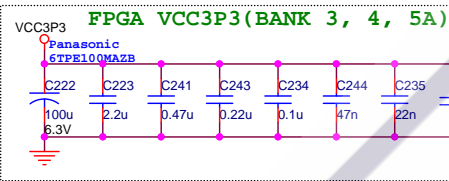
GPIO[35..0] 3,6,13



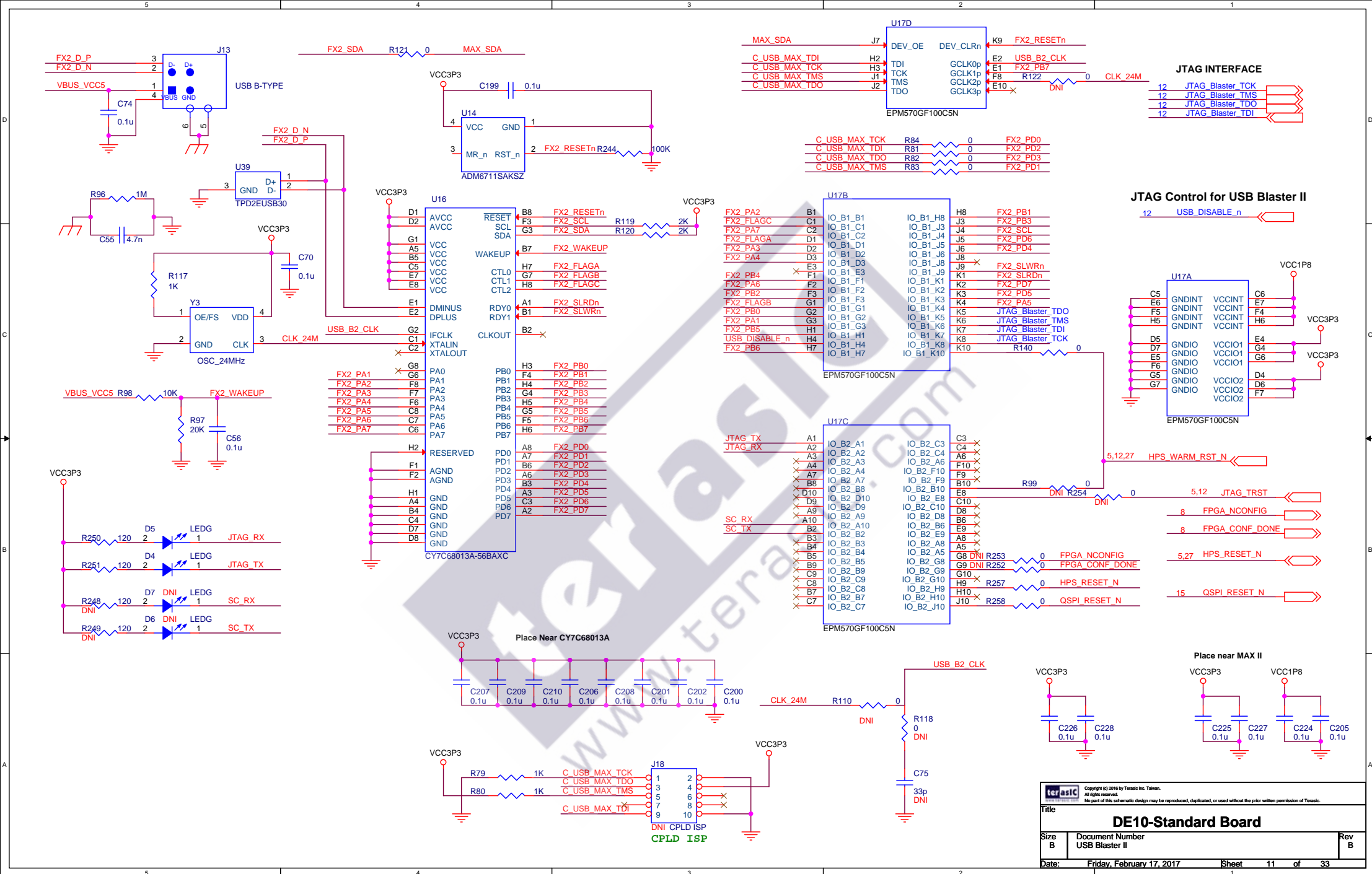




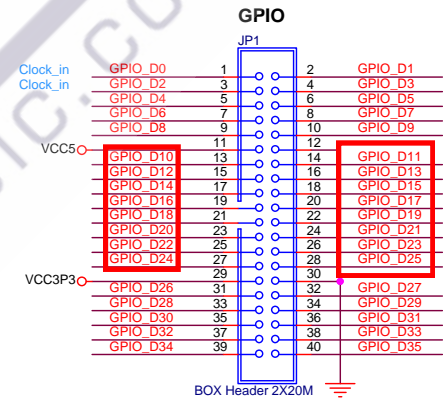
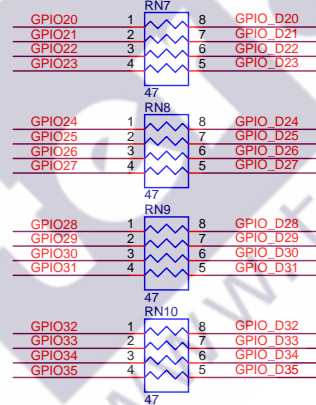
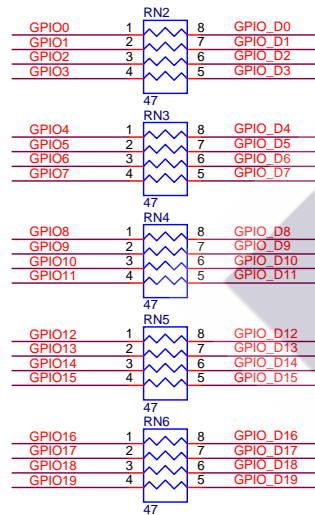
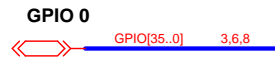
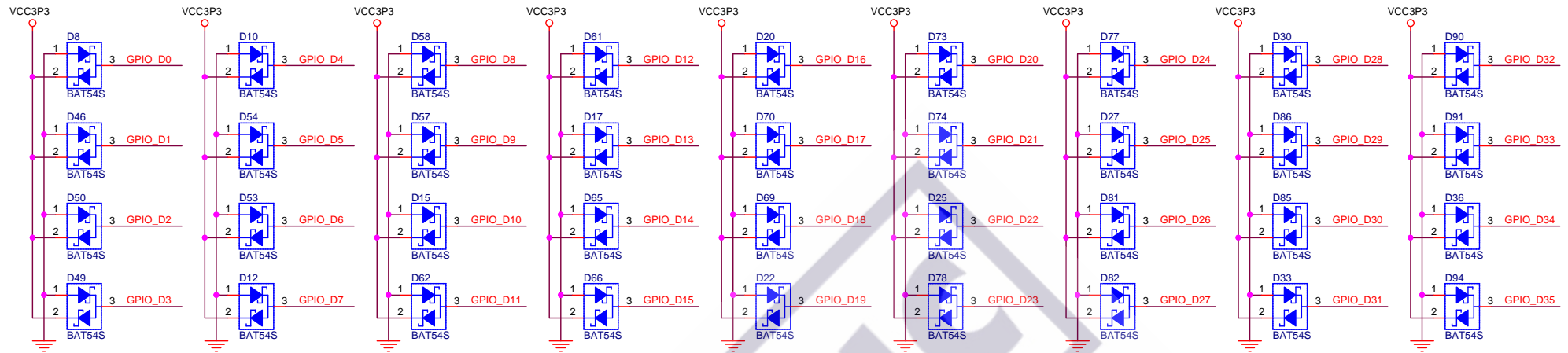
Place C394 close to J20/G23 pin



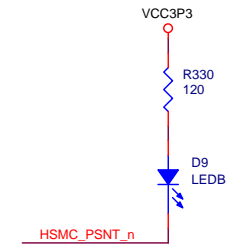
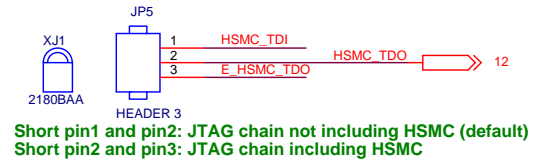
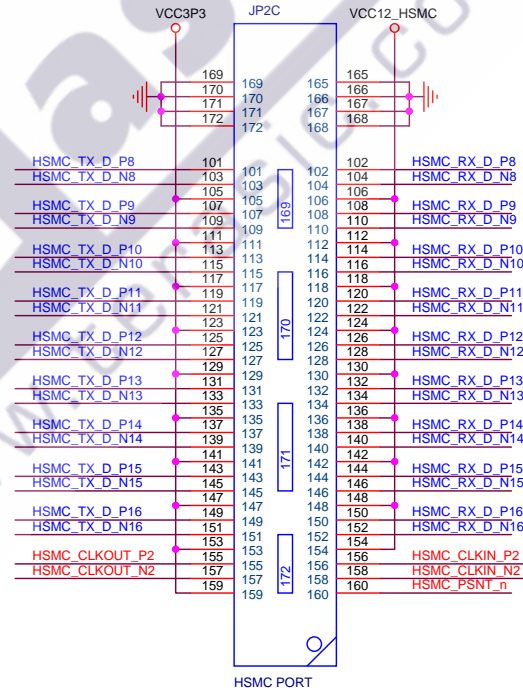
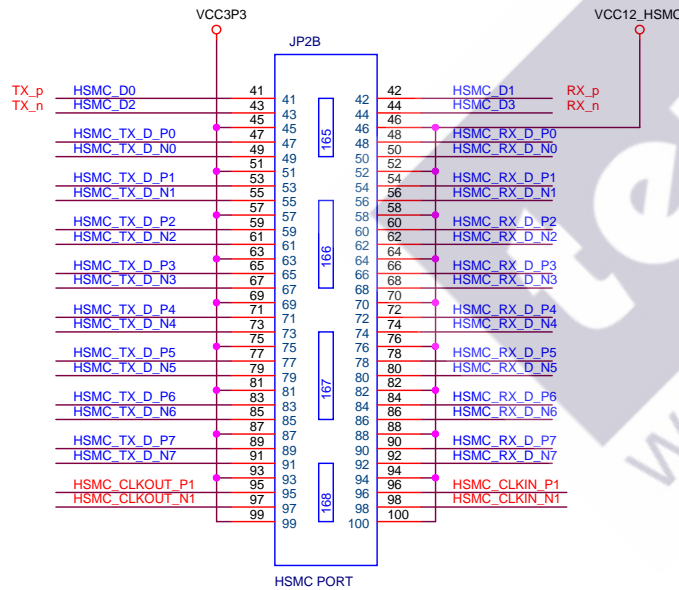
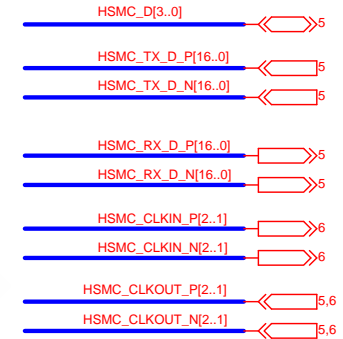
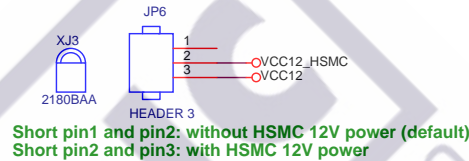
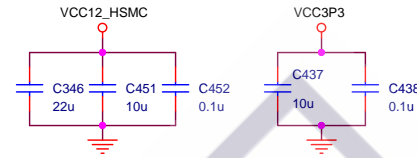
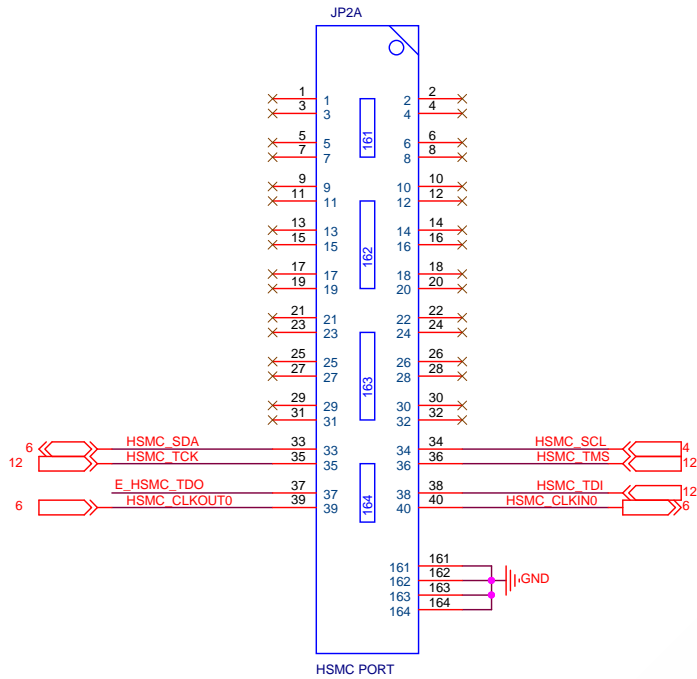




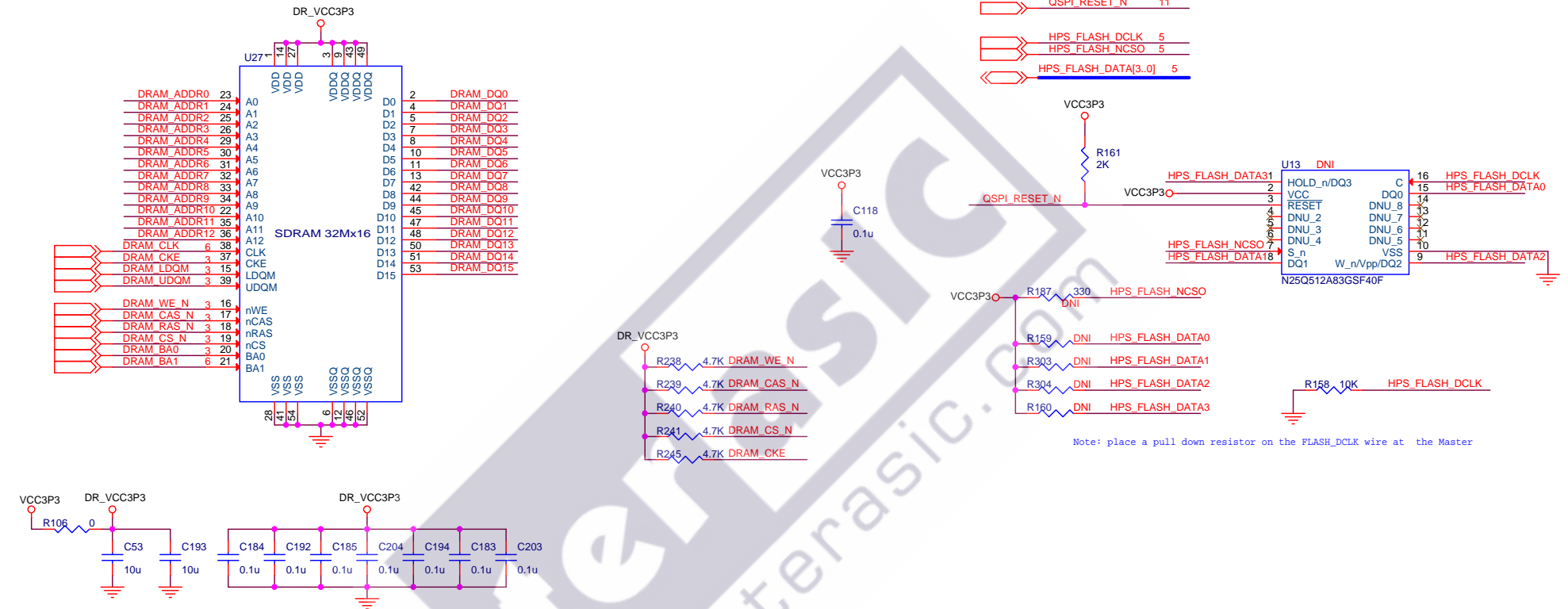




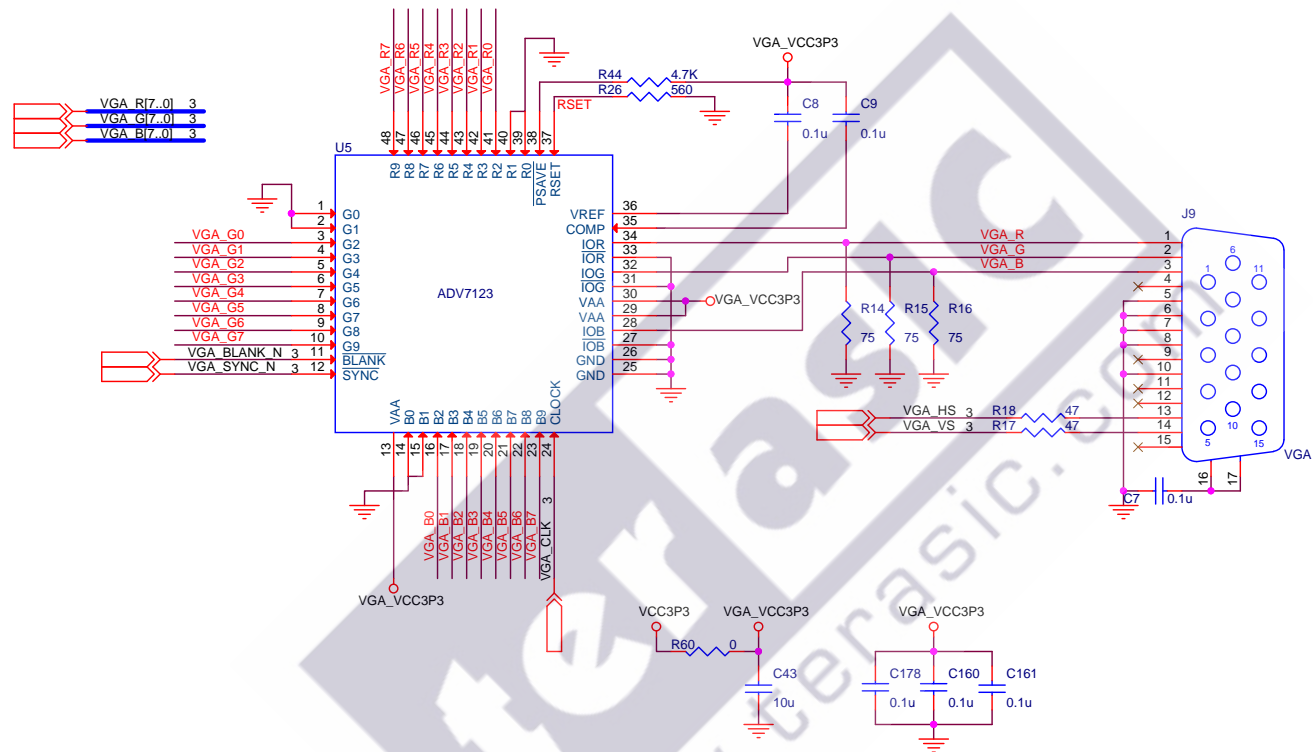


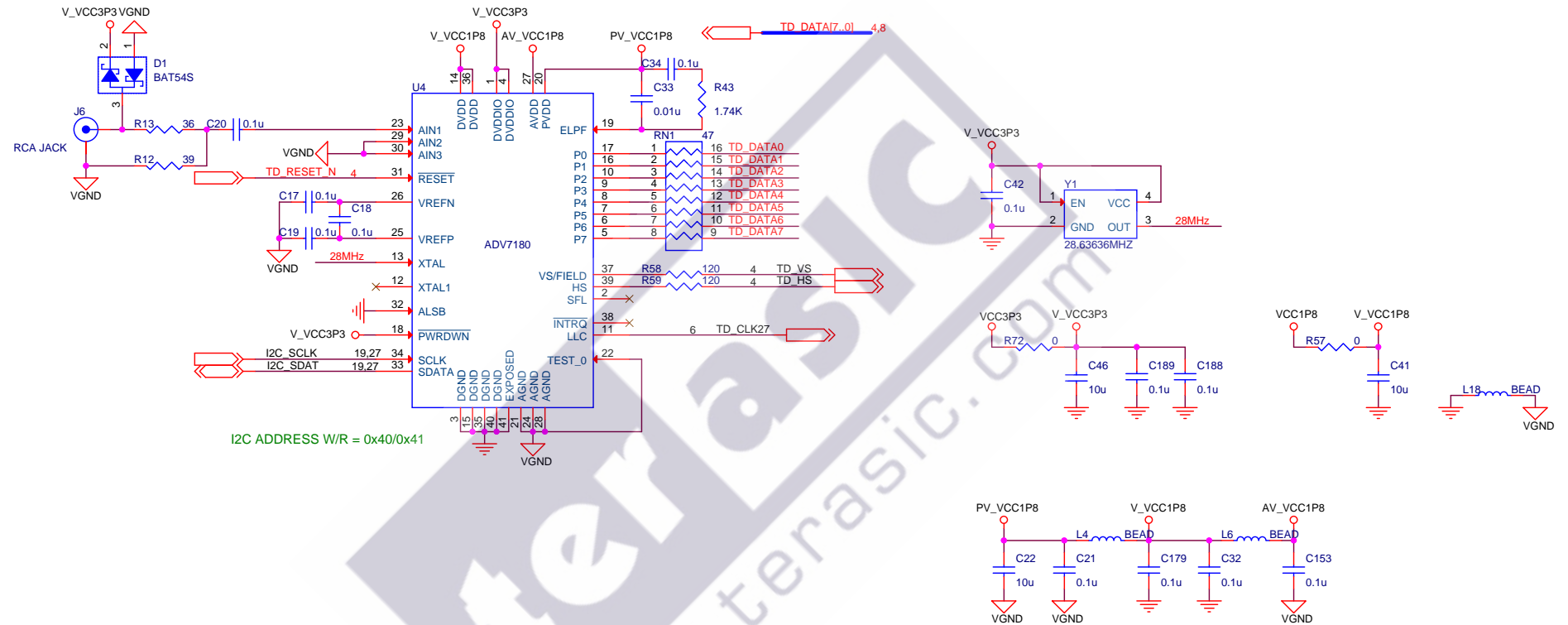


DRAM\_DQ[15..0] 3  
DRAM\_ADDR[12..0] 3,6

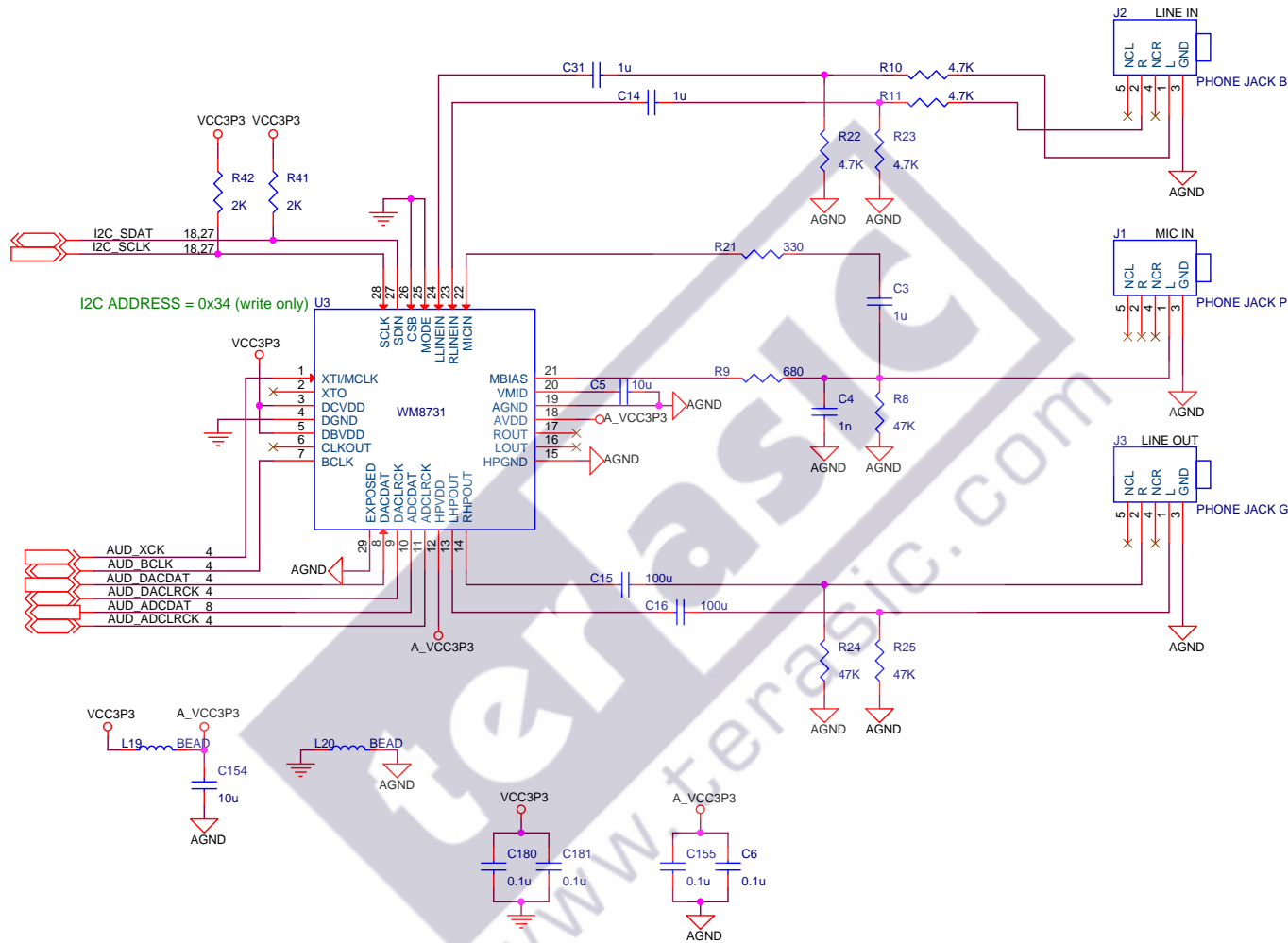


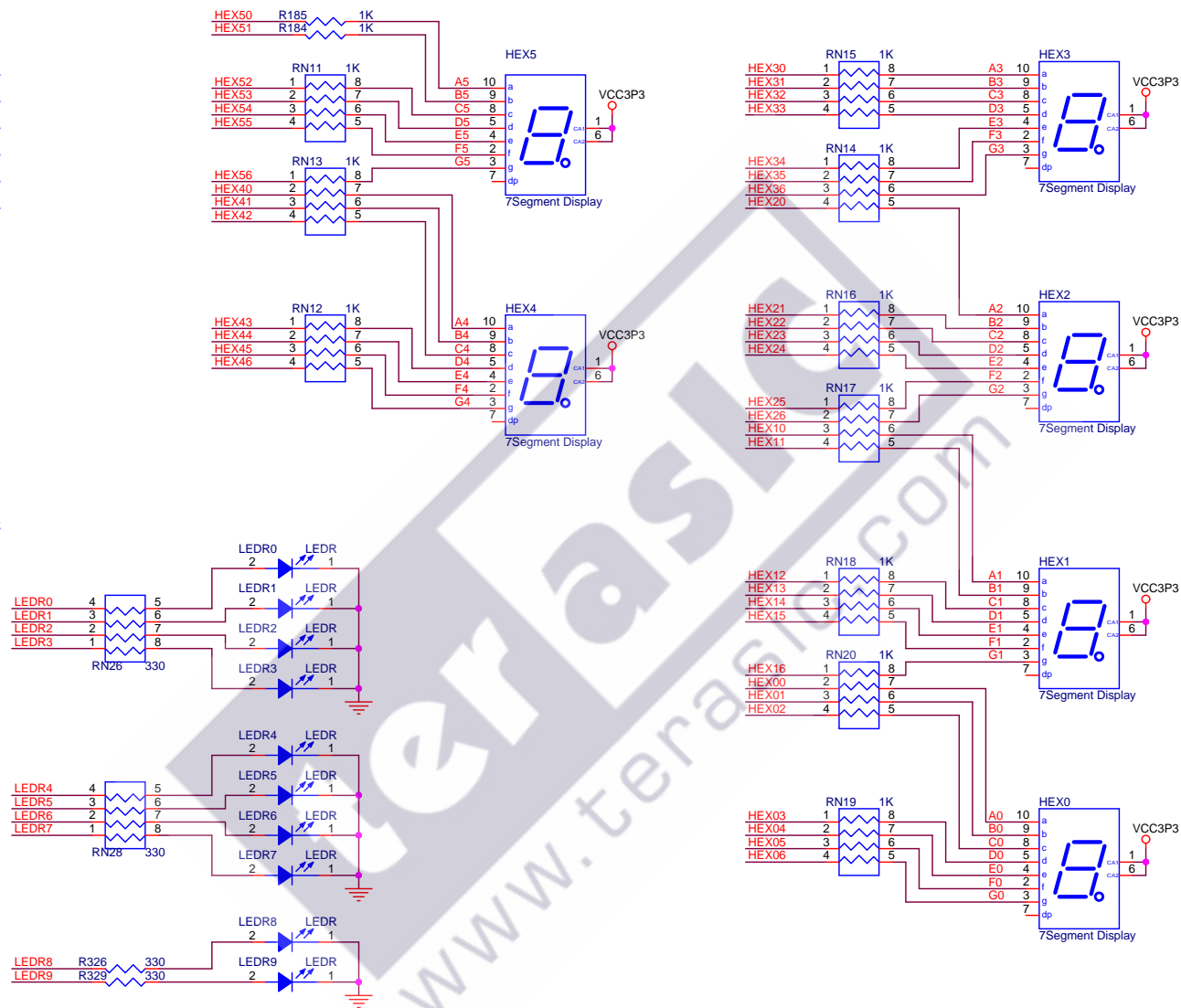
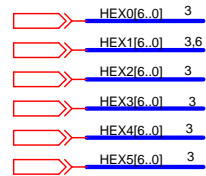




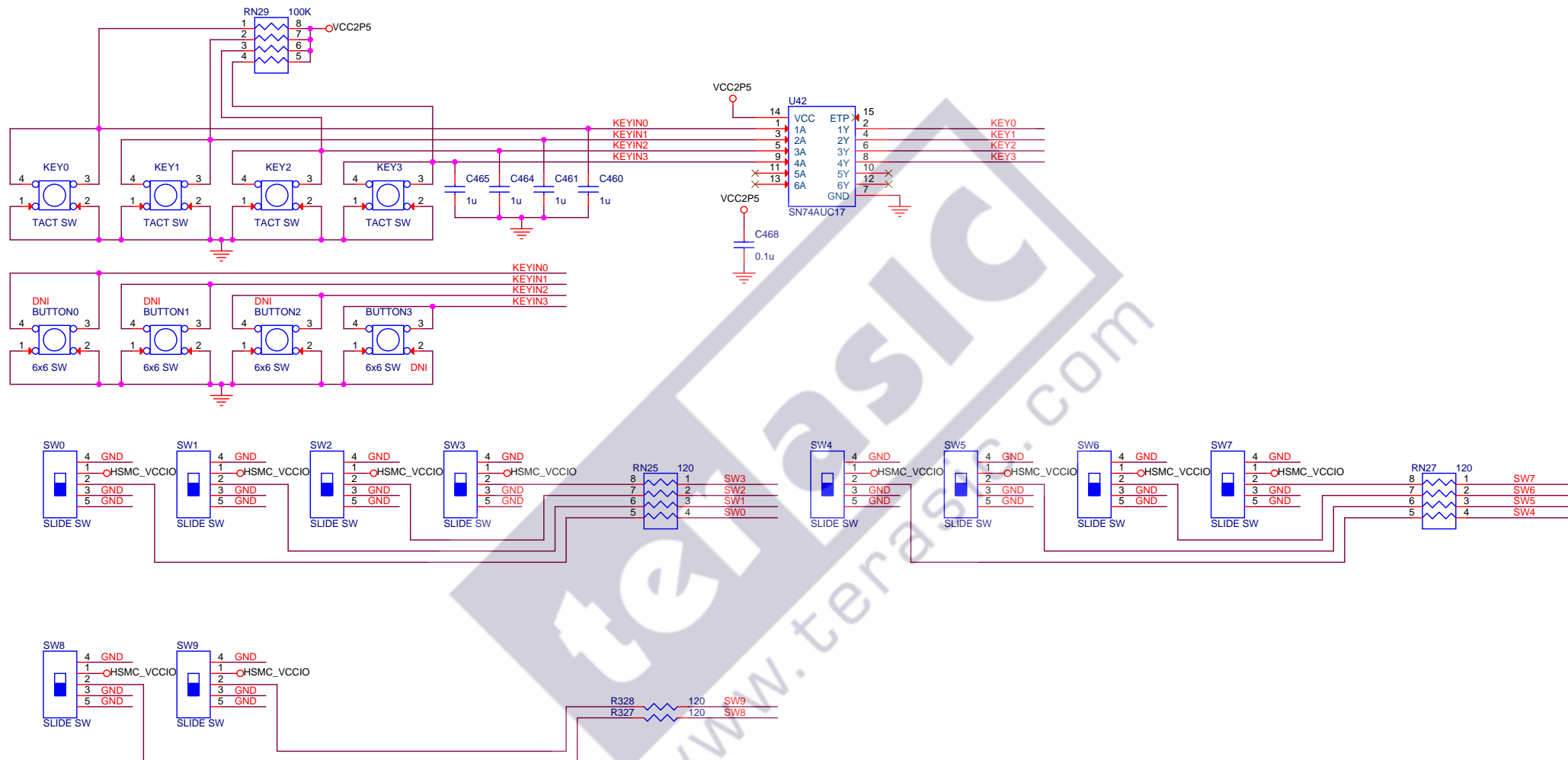





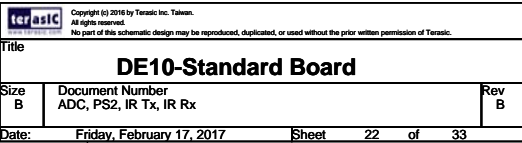


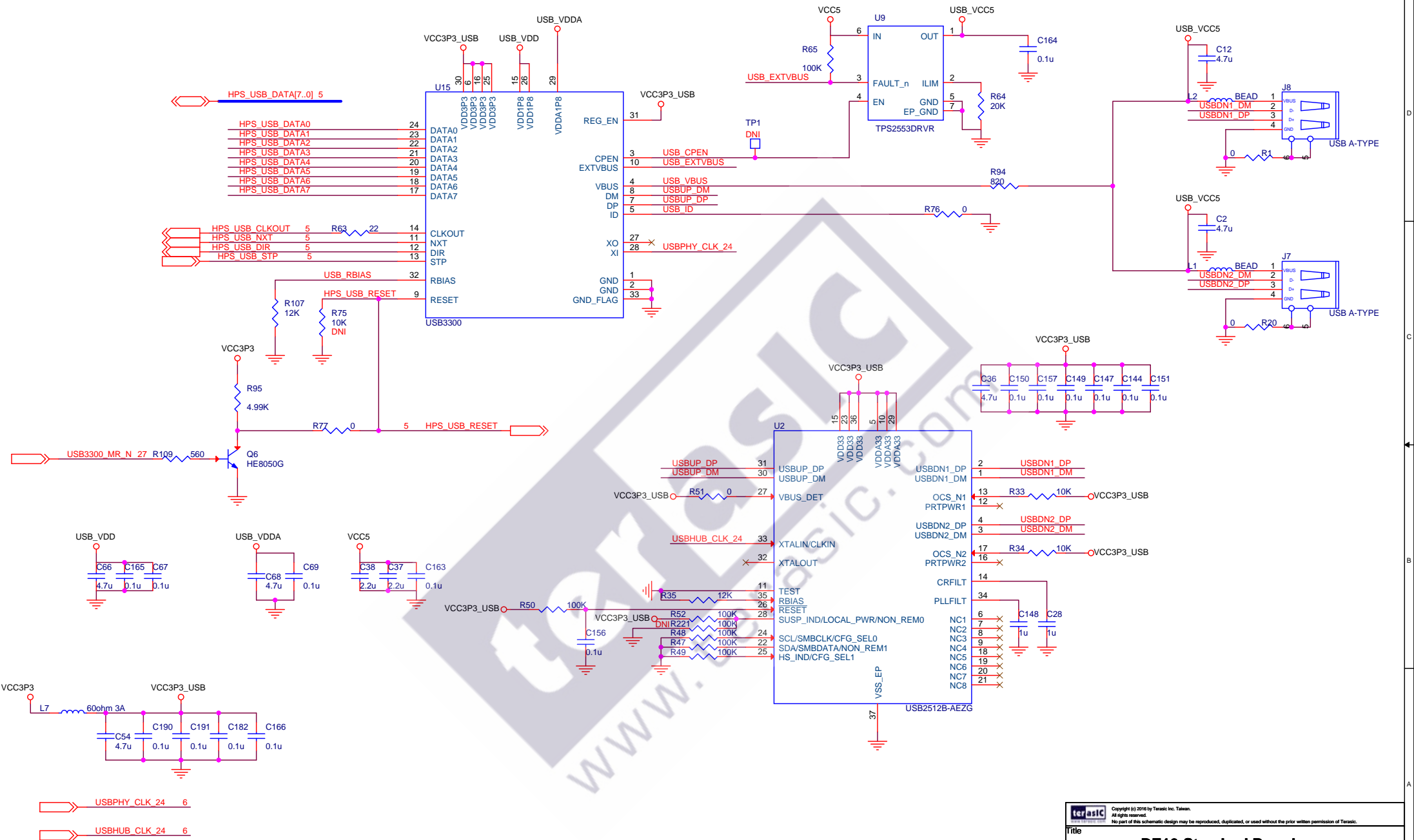


KEY[3..0] 3  
SW[9..0] 4,6

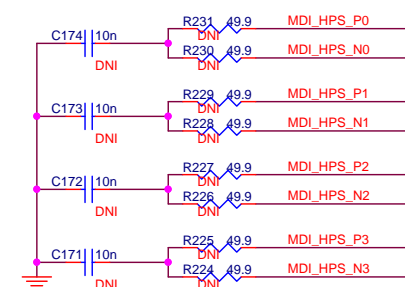
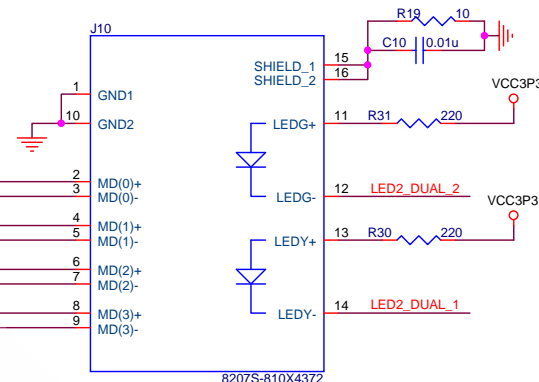
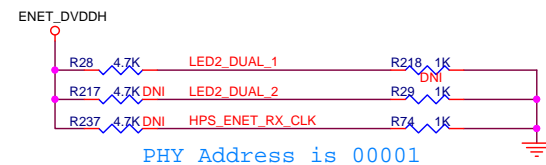
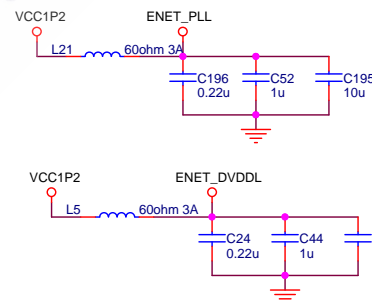
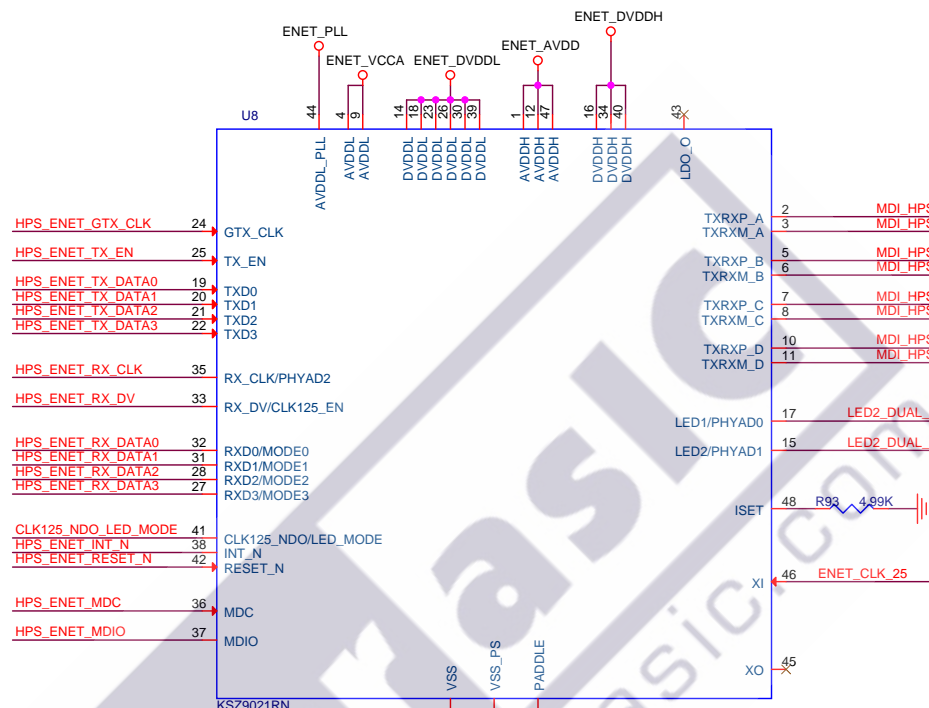
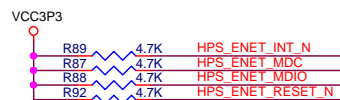
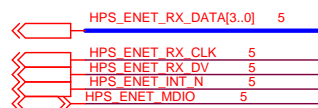


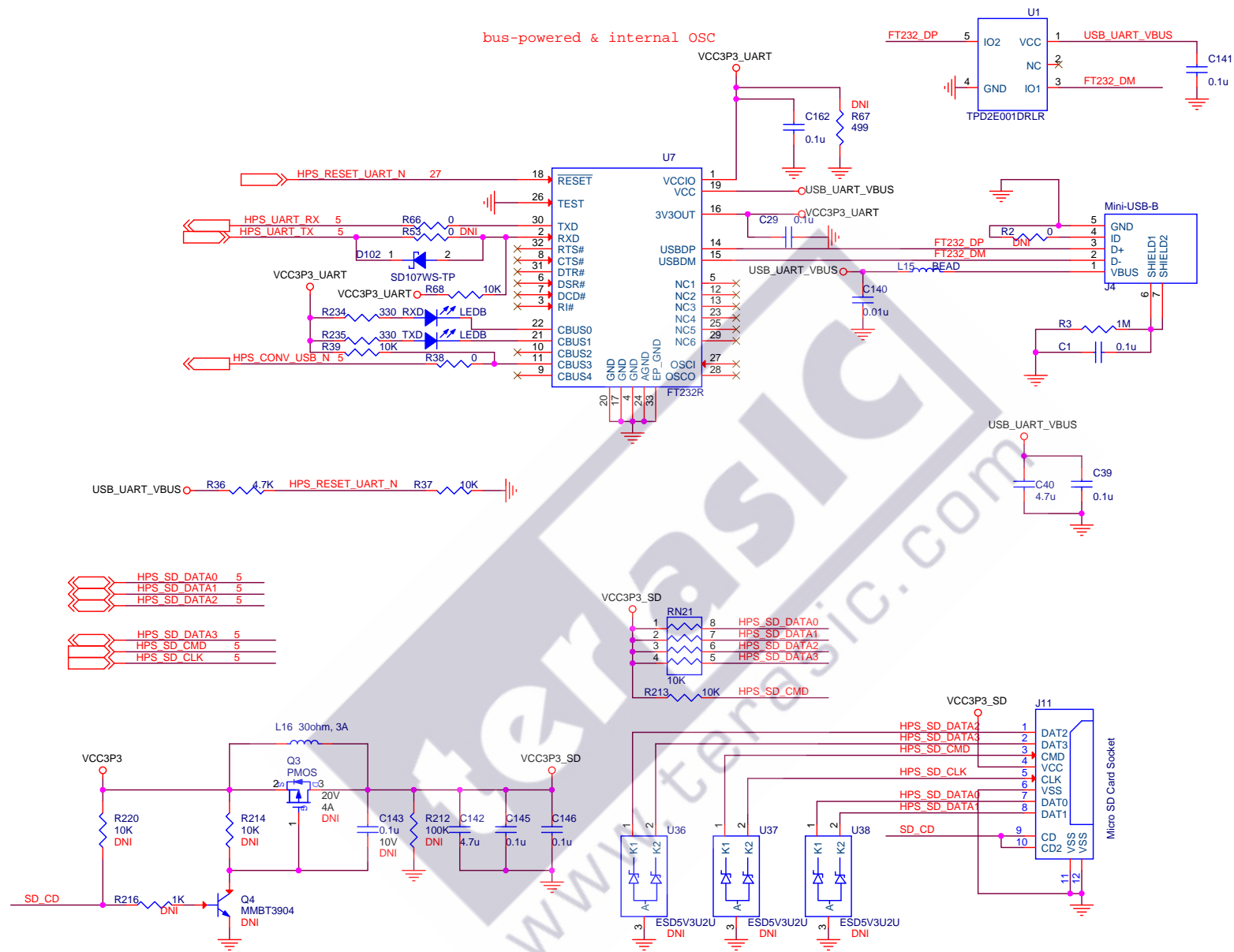
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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	FPGA BUTTON, Switch	B
Date:	Friday, February 17, 2017	Sheet 21 of 33





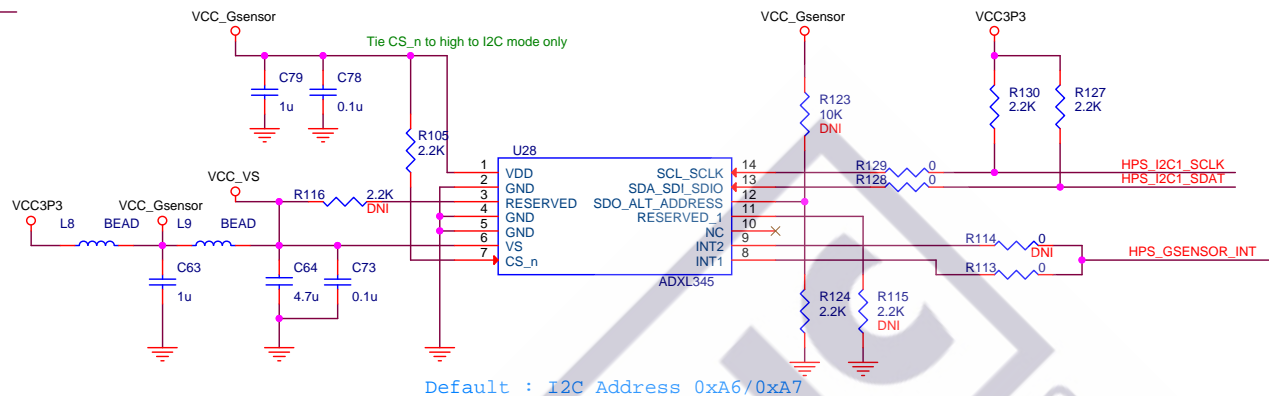




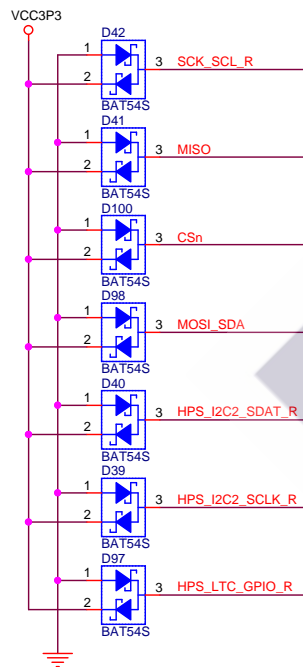


HPS\_I2C1\_SDAT 5,27  
HPS\_I2C1\_SCLK 5,27  
HPS\_GSENSOR\_INT 5

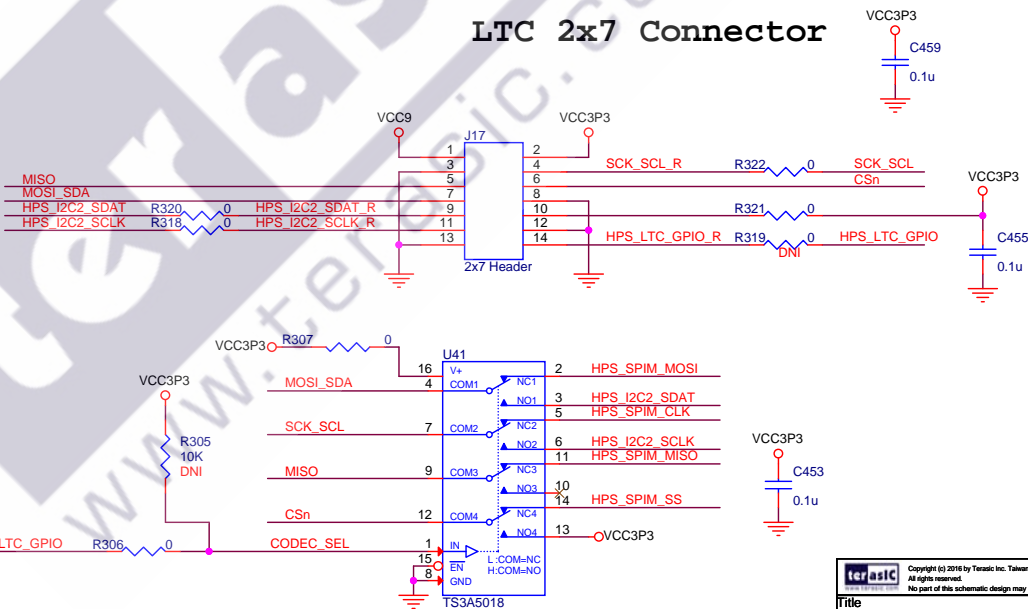
## Digital Accelerometer



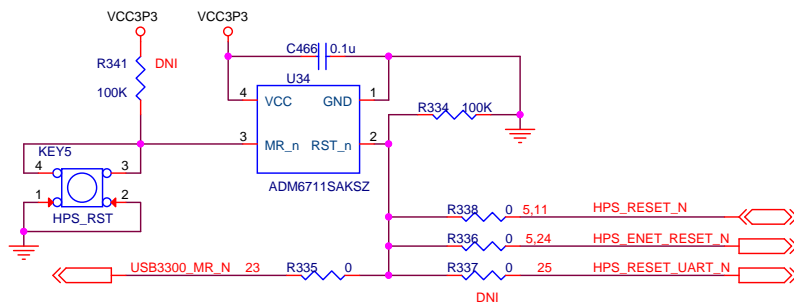
HPS\_I2C2\_SCLK 5  
HPS\_I2C2\_SDAT 5  
HPS\_SPIM\_MOSI 5  
HPS\_SPIM\_CLK 5  
HPS\_SPIM\_SS 5  
HPS\_SPIM\_MISO 5  
HPS\_LTC\_GPIO 5



## LTC 2x7 Connector

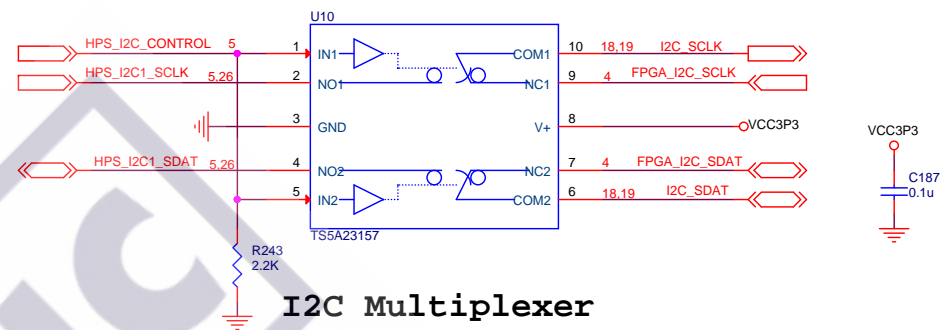


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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Accelerometer, LTC Connector	B
Date:	Friday, February 17, 2017	Sheet 26 of 33

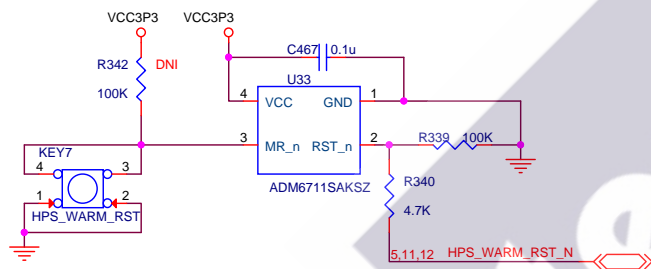


**HPS Cold Reset**

LOW --> NC to/from COM = ON and NO to/from COM = OFF  
HIGH --> NC to/from COM = OFF and NO to/from COM = ON



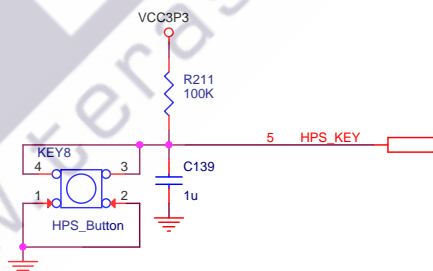
**I2C Multiplexer**



**HPS Warm Reset**



**HPS User LED**

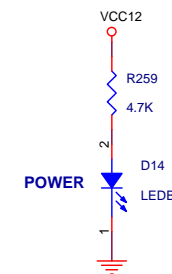
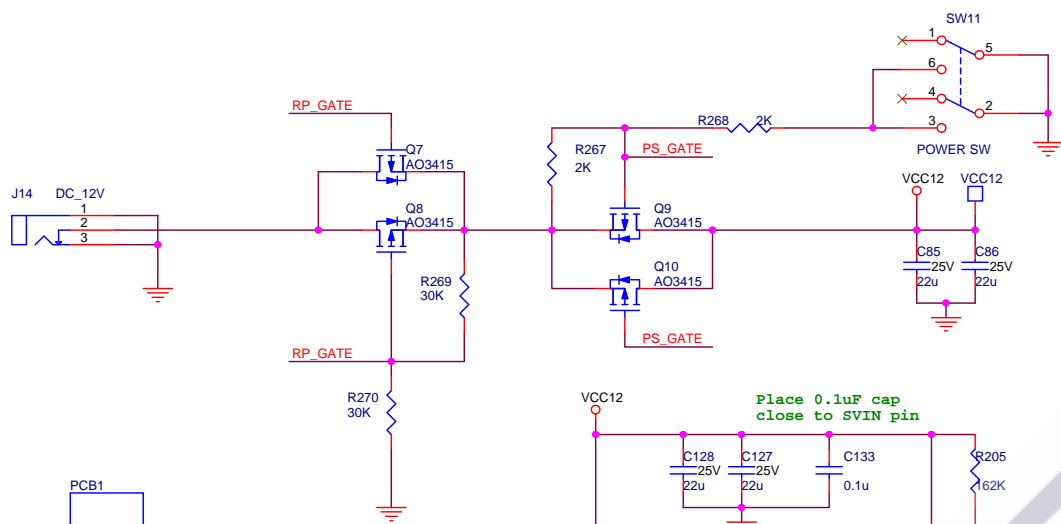


**HPS User Button**

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Title		
<b>DE10-Standard Board</b>		
Size	Document Number	Rev
B	I2C Multiplexer, HPS BUTTON, HPS LED	B
Date:	Friday, February 17, 2017	Sheet 27 of 33





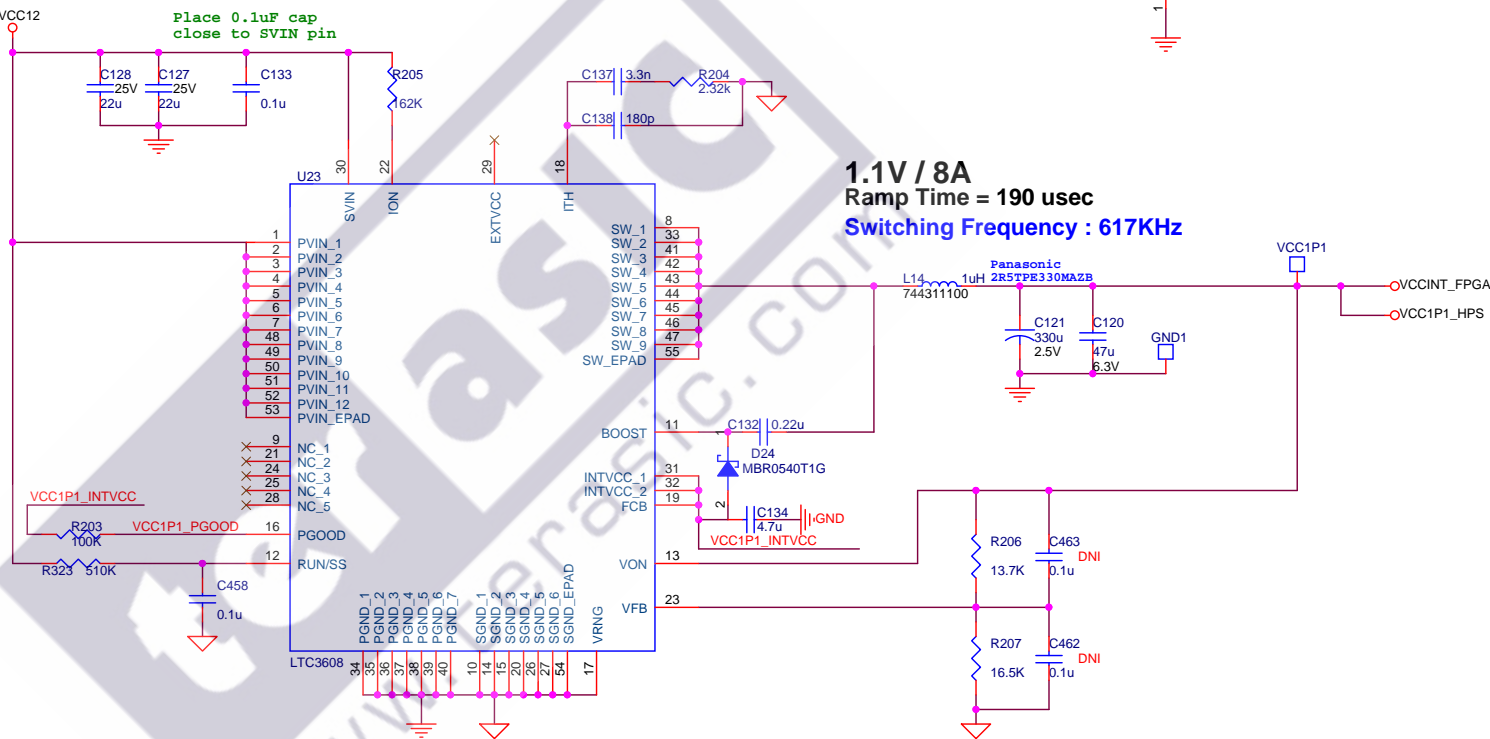
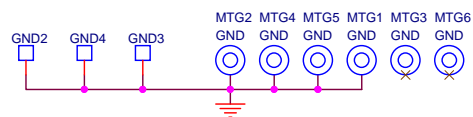


PCB1  
10-01609270-B0

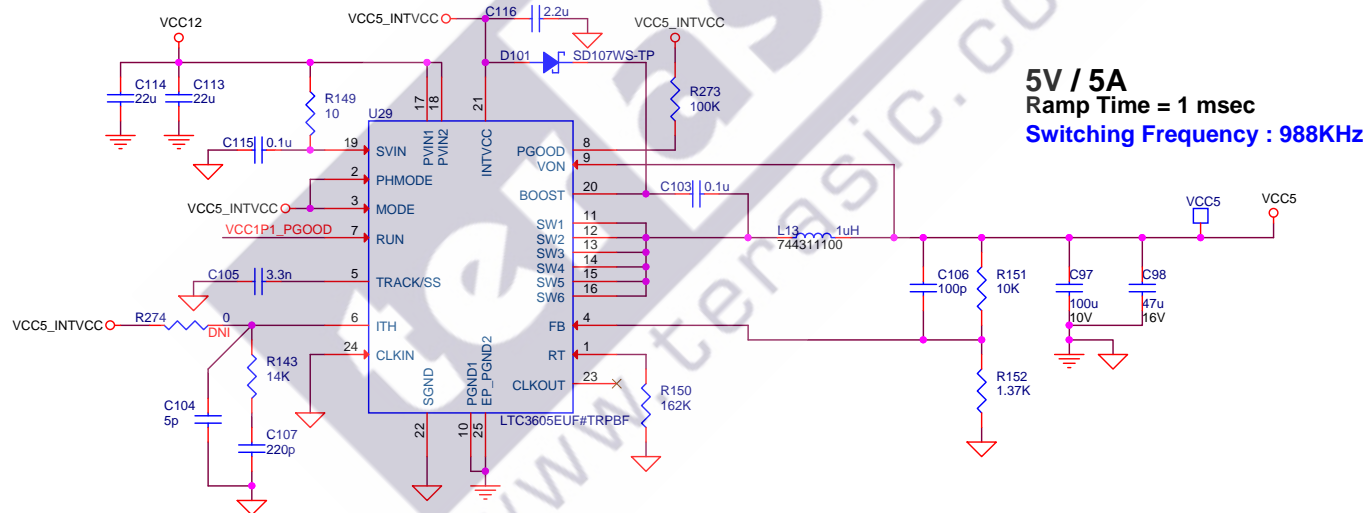
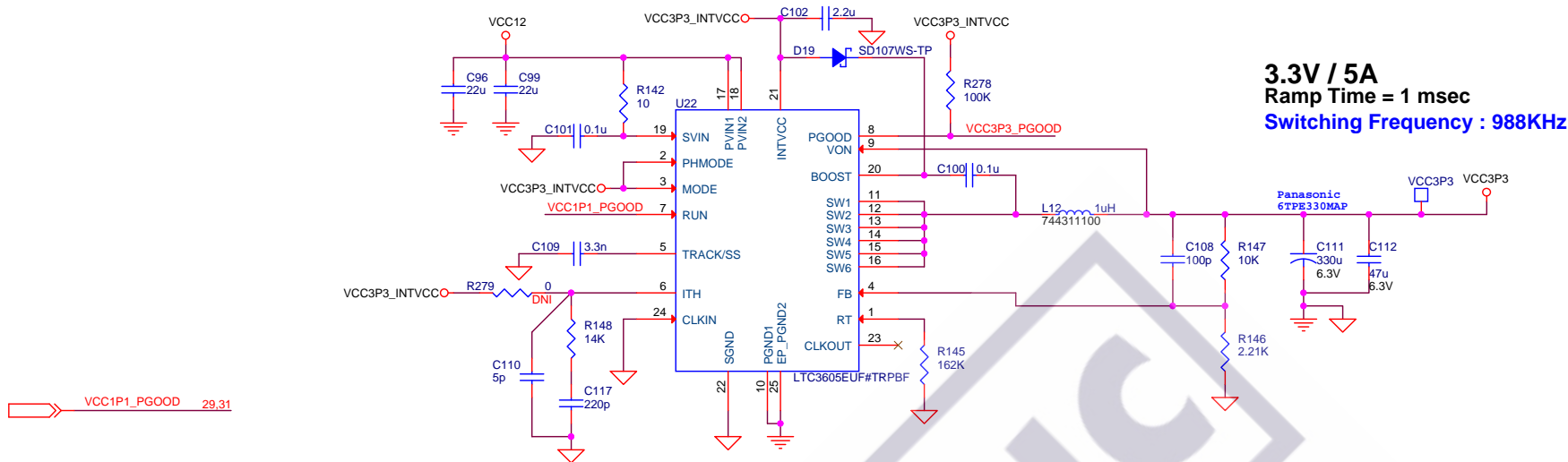
Place 0.1uF cap  
close to SVIN pin

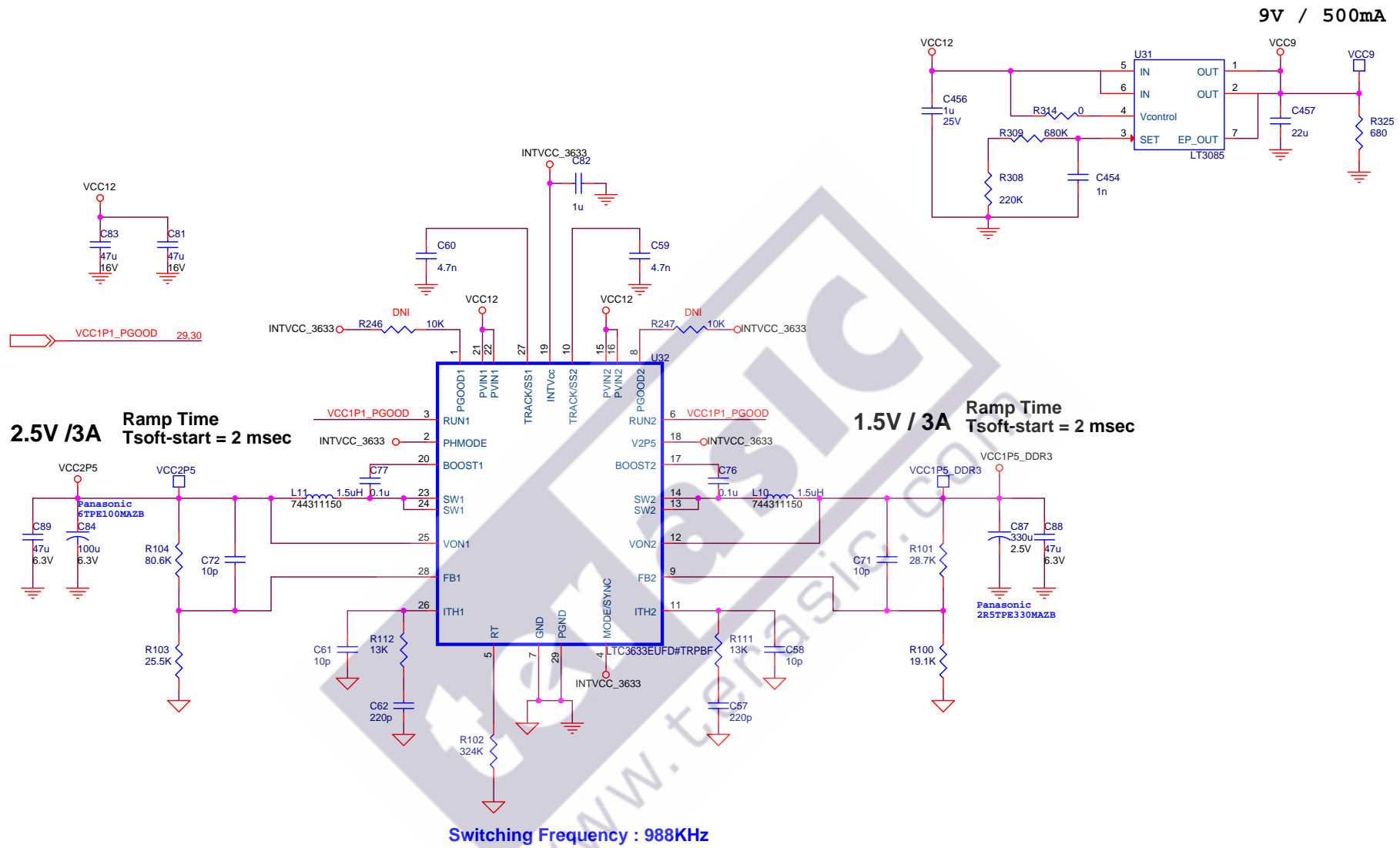
**1.1V / 8A**  
**Ramp Time = 190 usec**  
**Switching Frequency : 617KHz**

30,31 VCC1P1\_PGOOD

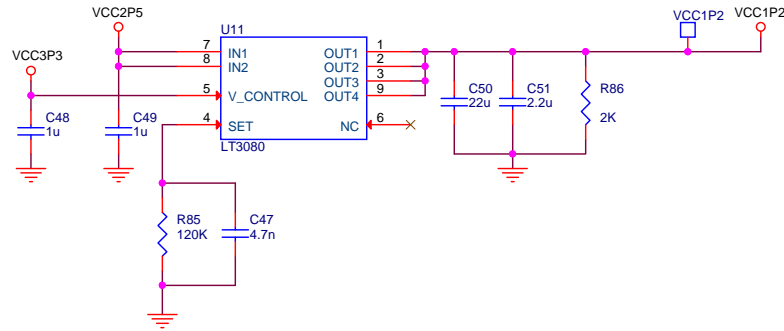


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Title		
<b>DE10-Standard Board</b>		
Size B	Document Number Power - 1.1V	Rev B
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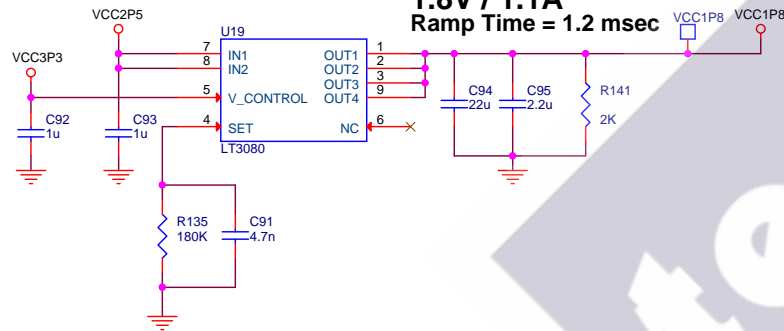




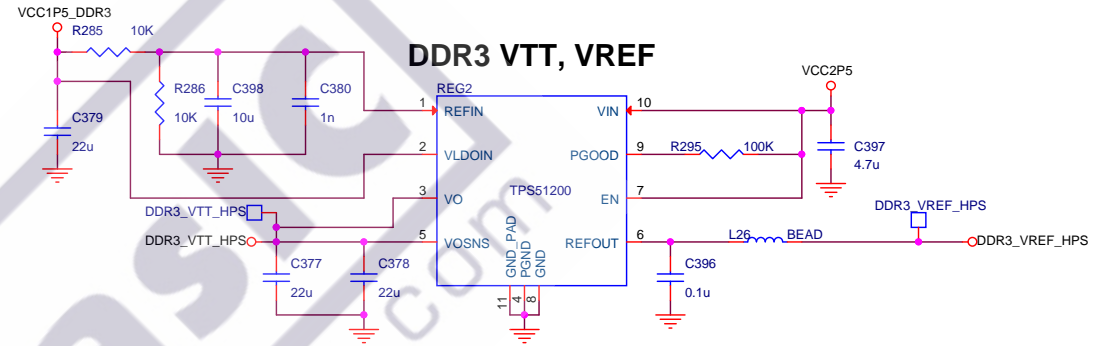
**1.2V / 1.1A**  
Ramp Time = 0.8msec



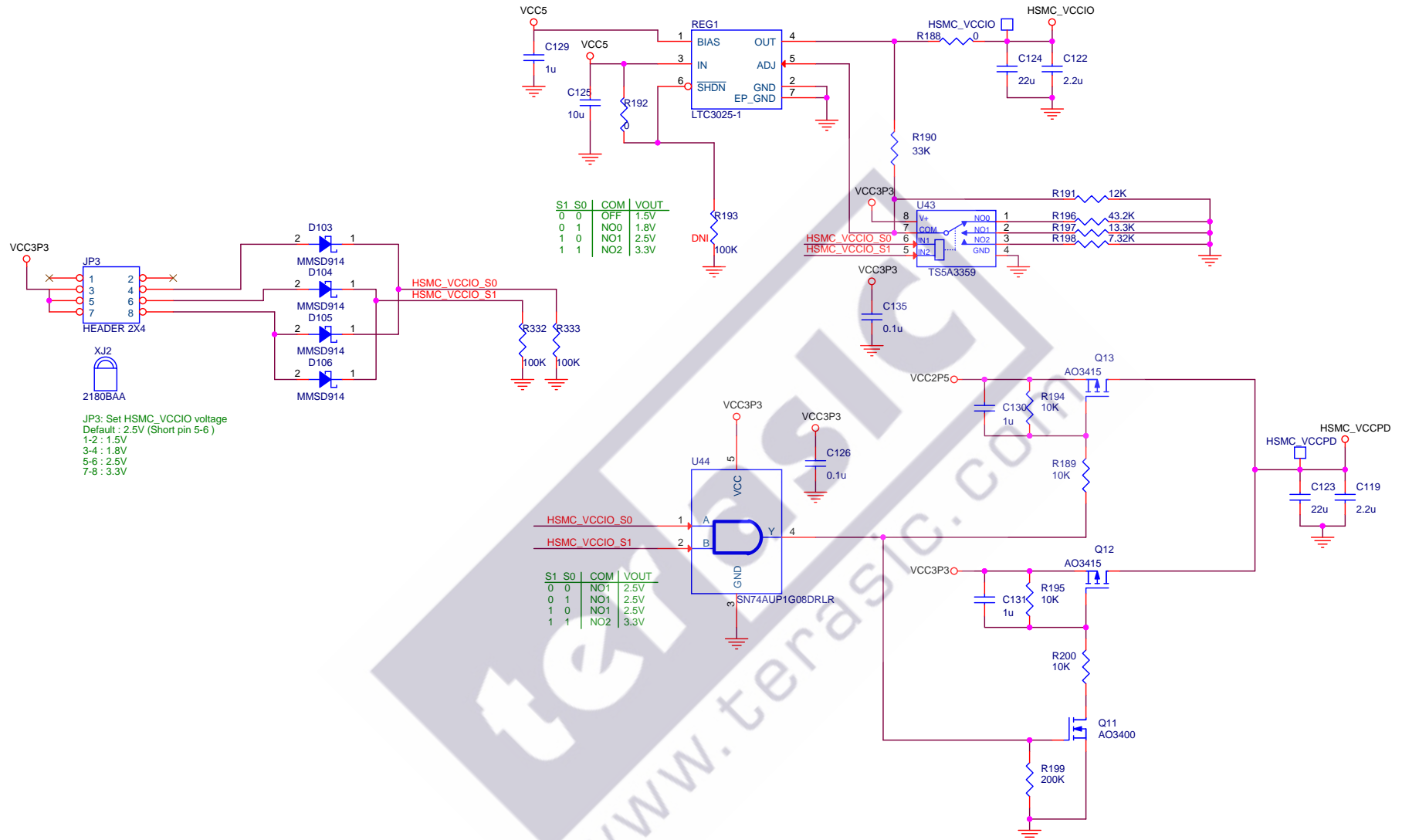
**1.8V / 1.1A**  
Ramp Time = 1.2 msec




**DDR3 VTT, VREF**



HSMC\_VCCIO / 0.5A Adjustable: 3.3/2.5/1.8/1.5 V  
Default: 2.5V



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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Power - VCCIO_HSMC & HSMC_VCCPD	B
Date:	Friday, February 17, 2017	Sheet 33 of 33