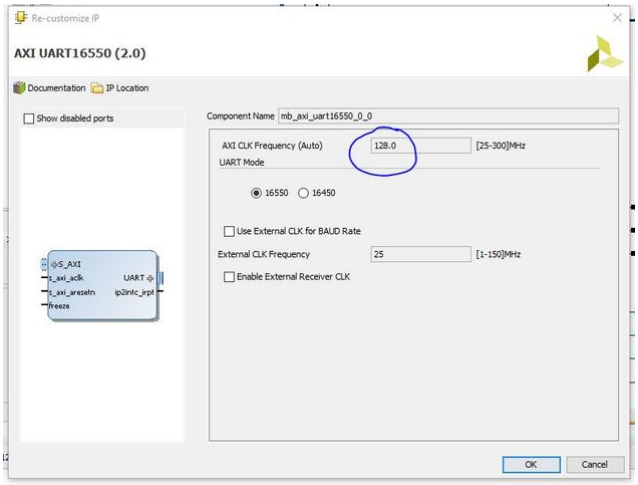
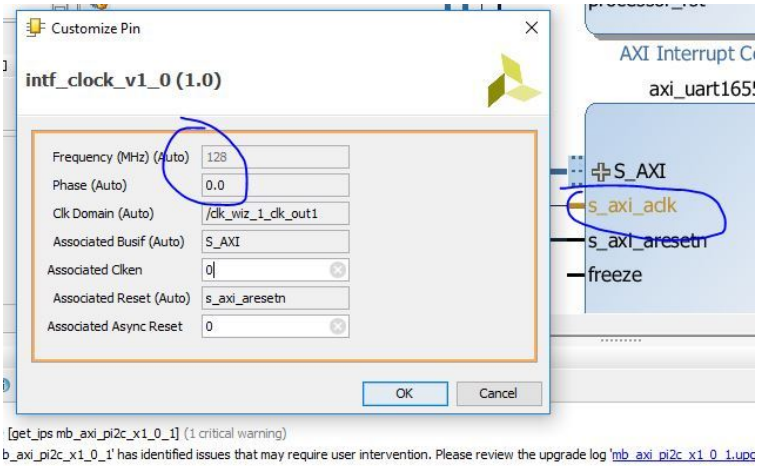
jliu83 (/s/profile/0052E00000N2uNNQAZ) (Customer) asked a question.
May 2, 2016 at 3:44 AM (/s/question/0D52E00006iHkzzSAC/help-with-automatic-generation-of-parameter-such-as-clock-frequency)

## Help with automatic generation of parameter such as clock frequency

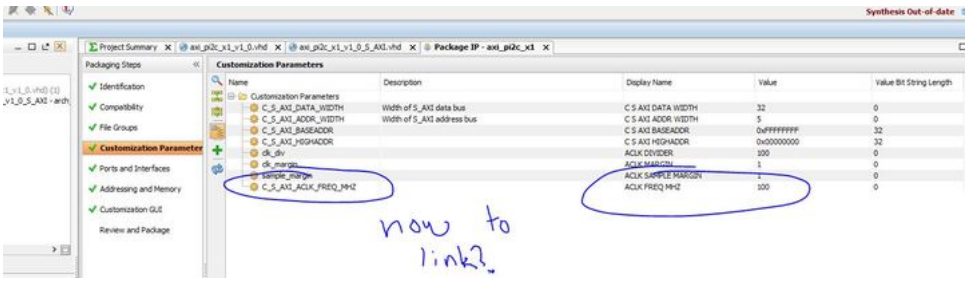
I have having trouble understanding how to get parameters to be automatically passed when creating and packaging an IP.
As an example, this is what I would like to do:
In the AXI_UART16550_v2_0 IP by Xilinx. When adding this IP, then customizing, there is parameter that is automatically acquired. I want to this exact same thing in my very own custom IP. This is not as straight forward as I had hoped, and I have not been able to find the documentation for this. If any one knows how to do this when packaging and IP, I would appreciate the advice. Also, I'd like to know how to use this parameter on the VHDL side (IE. linking the IP/GUI to the actual VHDL).




When double clicking the clock wire interface, it seems like some of the interface parameters are already there, I guess the crux of my issue is to extract this parameter somehow into my IP.




When I create my own IP, I can create these parameters, but I do not know how to link this to the interface parameter value.




Any help? Any insight would be greatly appreciated.

PROCESSOR SYSTEM DESIGN AND AXI (/S/TOPIC/0TO2E000000YKXZWA4/)

2 answers 23 views



Top Rated Answers



UserNotFound (/s/profile/0052E00000N31ZlQAJ) (Customer)
Edited by User16321524762994828 73 September 25, 2021 at 11:13 AM

**BEST SOLUTION**
Solved... cost me most of my day.
Now I can program a timer that will delay the same time no matter the axi frequency
I hope this will help some other people too.
You don't need to deal with propagation if you use AXI interfaces. You simply can't access the interface parameter because it contains a dot, so you need to copy it
S00_AXI.FREQ_HZ -> C_S00_AXI_FREQ_HZ

1. Select your AXI-Interface.
   Properties -> Name = S00_AXI ?
   Properties -> Config -> FREQ_HZ = Value you want ?
2. Create Parameter to hold FREQ_HZ (I use C_S00_AXI_FREQ_HZ)
3. Add following code lines to *proc propagate* in *bd.tcl*

```
1  set freq_hz [get_property config.FREQ_HZ [get_bd_intf_pins $cellpath/S00_AXI]]
2  set_property config.C_S00_AXI_FREQ_HZ $freq_hz [get_bd_cells $cellpath]
3
```

4. Package IP-Core
5. Update your Design
6. **RESTART VIVADO!** (or the old TCL script will run)
7. Reopen Vivado and Validate Design

If you really need to propagate try
https://support.xilinx.com/0D52E00006hpTlzSAE (https://support.xilinx.com/0D52E00006hpTlzSAE)

```
1  proc propagate { cellpath otherInfo} {
2     set cell_handle [get_bd_cells $cellpath]
3     set_property config.PARAM1 [get_property config.PARAM2 [find_bd_objs –relation connected_to [get_bd_intf_pins
   $cell_handle/Interface1]]] $cell_handle
4  }
```

Felix

Selected as Best Like 2 likes

All Answers

jliu83 (/s/profile/0052E00000N2uNNQAZ) (Customer)
6 years ago

Any update on this? Still waiting for a response. There has to be a way to do this.

Like Reply

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```
1  proc propagate { cellpath otherInfo} {
2     set cell_handle [get_bd_cells $cellpath]
```

```
3     set_property config.PARAM1 [get_property config.PARAM2 [find_bd_objs -relation connected_to [get_bd_intf_pins
4   }
```



Felix

Selected as Best · Like · Reply · 2 likes

(https://www.xilinx.com/)

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**TRENDING ARTICLES**

Export IP Invalid Argument / Revision Number Overflow Issue (Y2K22)
(/s/article/76960)

AXI Basics 1 - Introduction to AXI
(/s/article/1053914)

Debugging PCIe Issues using lspci and setpci
(/s/article/1148199)

PetaLinux 2021.2 - Product Update Release Notes and Known Issues
(/s/article/000032521)

65444 - Xilinx PCI Express DMA Drivers and Software Guide
(/s/article/65444)

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