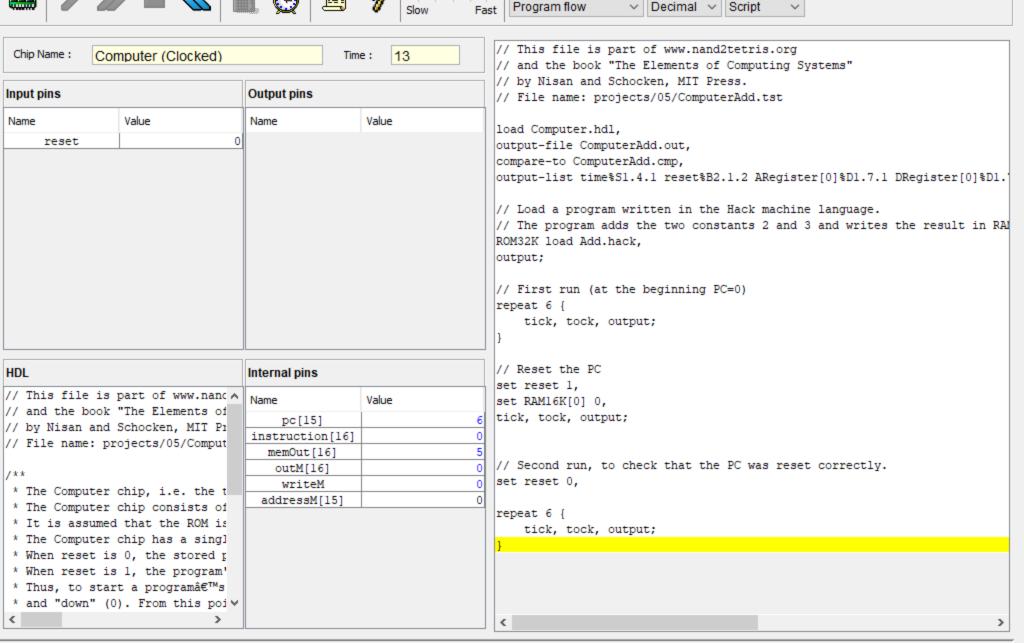
```
File Edit Selection Find View Goto Tools Project Preferences Help
◆▶
                                               Computer.hdl
      // This file is part of www.nand2tetris.org
      // and the book "The Elements of Computing Systems"
      // by Nisan and Schocken, MIT Press.
      // File name: projects/05/Computer.hdl
      /**
       * The Computer chip, i.e. the top-most chip of the Hack architecture.
       * The Computer chip consists of CPU, ROM and RAM chip-parts.
       * It is assumed that the ROM is pre-loaded with some Hack program.
       * The Computer chip has a single 1-bit input, named "reset".
       * When reset is 0, the stored program starts executing.
11
12
       * When reset is 1, the program's execution restarts.
13
       * Thus, to start a program's execution, reset must be pushed "up" (1)
14
       * and "down" (0). From this point onward the user is at the mercy of
15
       * the software. In particular, depending on the program loaded into
       st the computer, the screen may show some output and the user may be
17
       * expected to interact with the computer via the keyboard.
       */
19
      CHIP Computer {
21
22
          IN reset;
23
24
          PARTS:
25
          ROM32K(address=pc, out=instruction);
          CPU(inM=memOut, instruction=instruction, reset=reset, outM=outM,
27
              writeM=writeM, addressM=addressM, pc=pc);
28
          Memory(in=outM, load=writeM, address=addressM, out=memOut);
      X
```

C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\Computer.hdl - Sublime Text (UNREGISTERED)

File View Run Help



Animate:

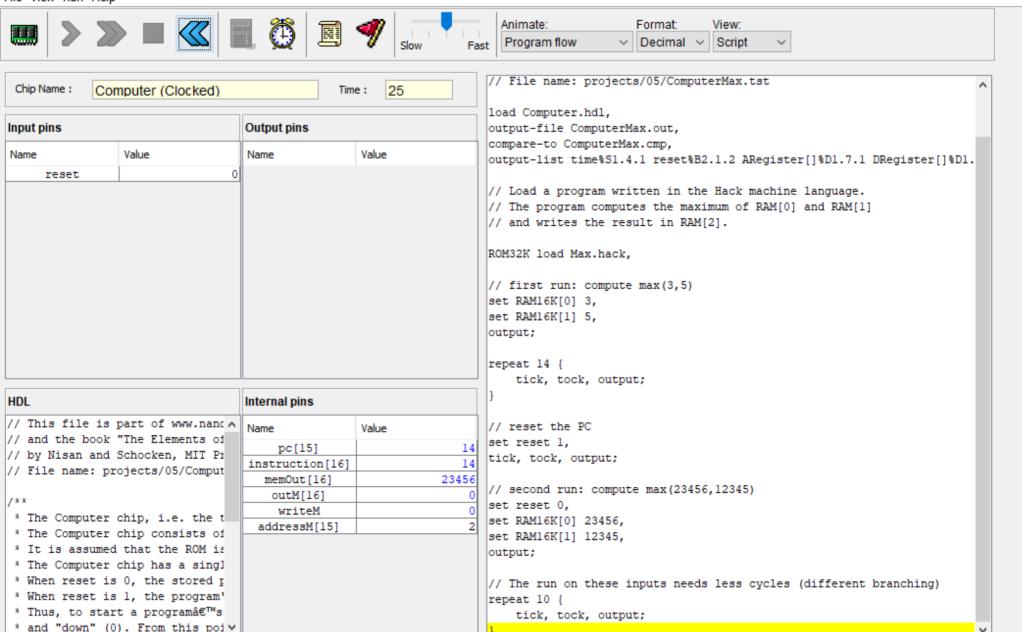
Format:

View:

End of script - Comparison ended successfully

Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\Computer.hdl

File View Run Help



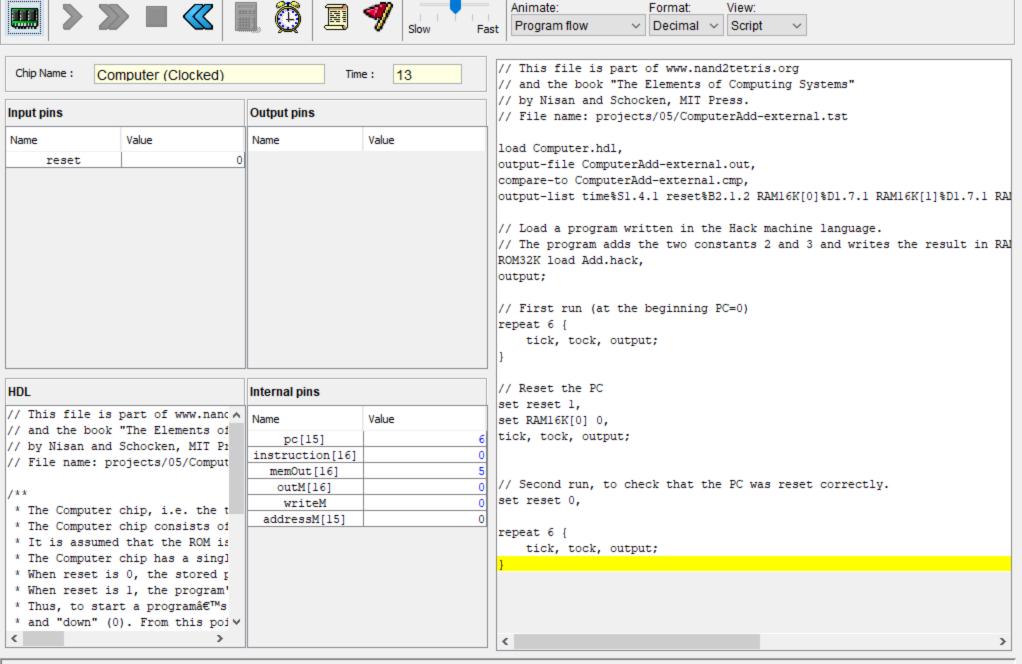
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>

End of script - Comparison ended successfully

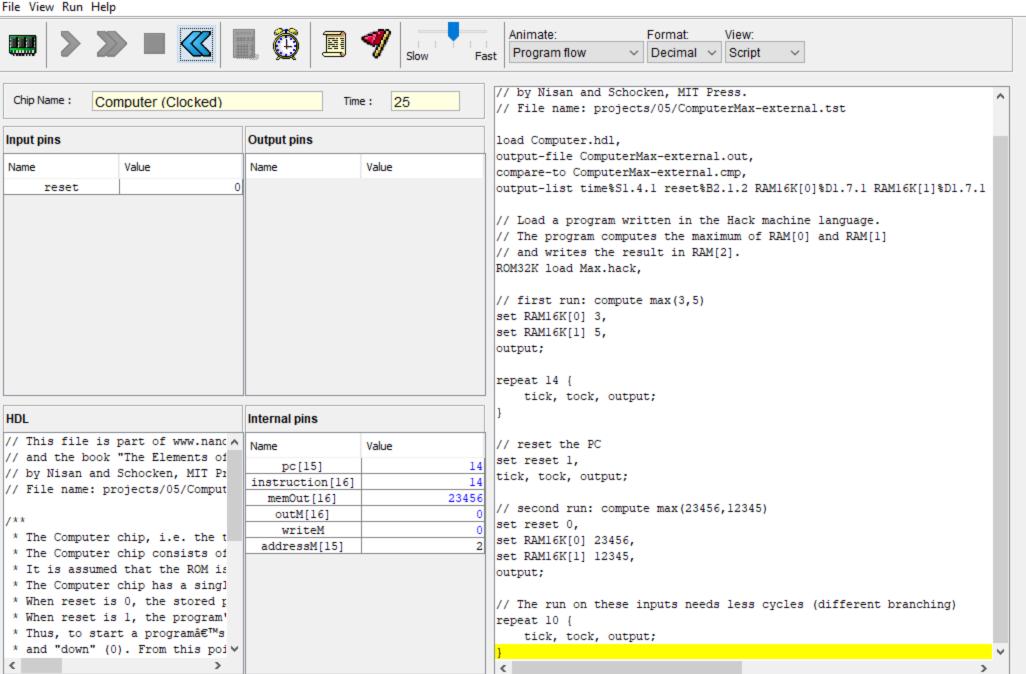
>

Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\Computer.hdl



End of script - Comparison ended successfully

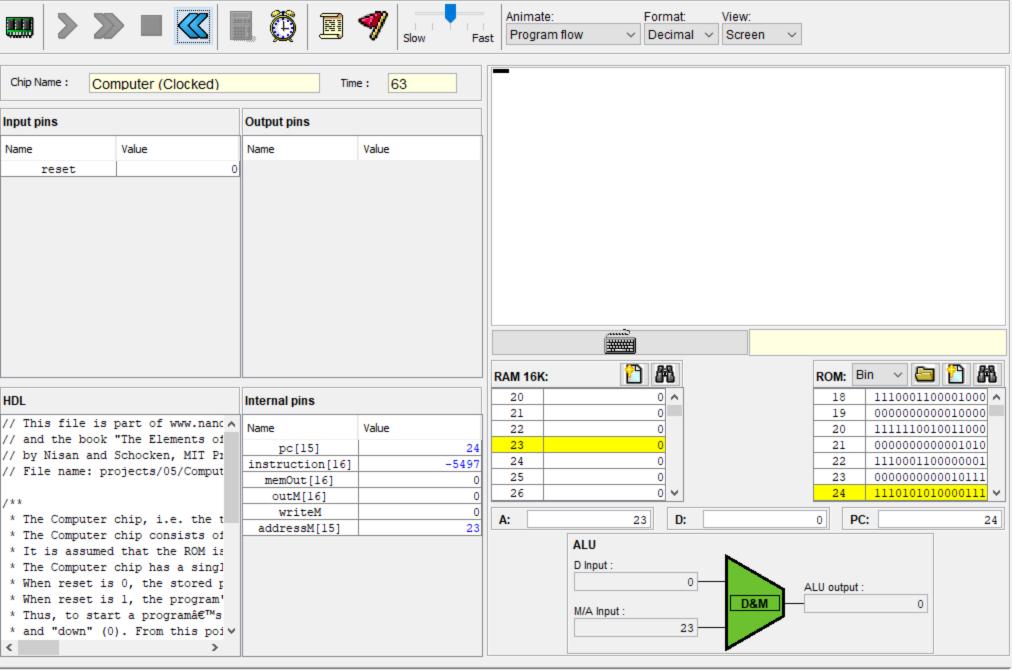
Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\Computer.hdl



End of script - Comparison ended successfully

Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\Computer.hdl

File View Run Help



End of script - Comparison ended successfully

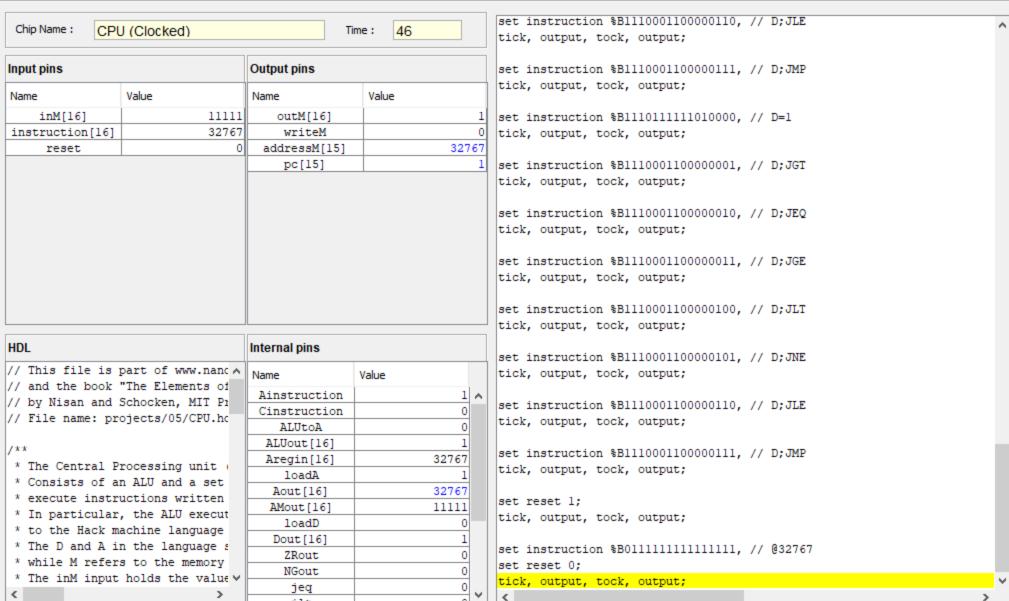
Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\Computer.hdl File View Run Help Animate: Format: View: Program flow Screen Decimal ~ Chip Name: Computer (Clocked) 63 Time: Input pins **Output pins** Value Value Name Name ol reset **2** ROM: Bin 🗸 🛅 🖺 船 **RAM 16K:** 0 ^ 1110001100001000 20 18 Internal pins HDL 0000000000010000 21 0 19 // This file is part of www.nanc A Name Value 0 1111110010011000 22 20 // and the book "The Elements of 23 0 21 0000000000001010 pc[15] // by Nisan and Schocken, MIT Pr 22 0 1110001100000001 -5497 24 instruction[16] // File name: projects/05/Comput 0 0000000000010111 25 23 memOut[16] 0 0 4 24 1110101010000111 26 0 outM[16] writeM * The Computer chip, i.e. the t 23 D: PC: 0 24 A: addressM[15] * The Computer chip consists of ALU * It is assumed that the ROM is * The Computer chip has a singl D Input: * When reset is 0, the stored p 0 ALU output : * When reset is 1, the program' D&M 0 M/A Input: * Thus, to start a program's 23 * and "down" (0). From this poi ∨

End of script - Comparison ended successfully

Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\CPU.hdl

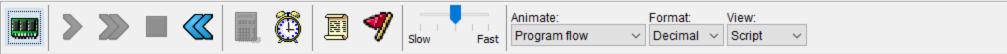
File View Run Help

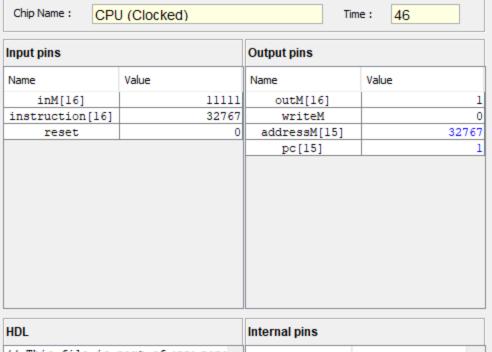




Hardware Simulator (2.5) - C:\Users\desha\OneDrive\Desktop\Classes\CS220\nand2tetris\projects\05\CPU.hdl

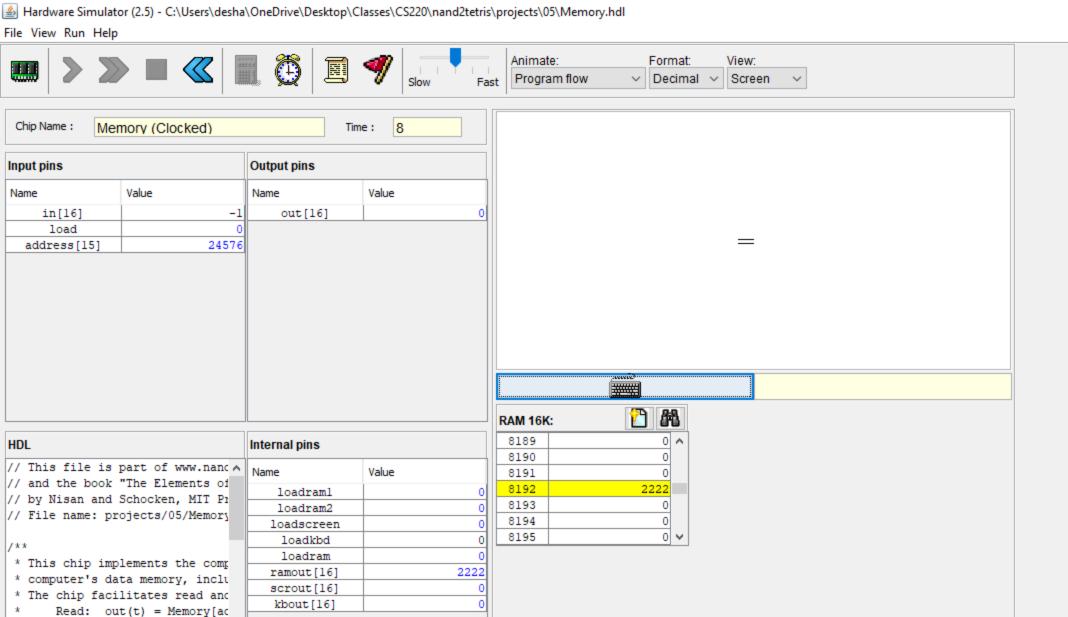
File View Run Help





HDL	Internal pins		
// This file is part of www.nanc ^ // and the book "The Elements of	Name	Value	
// by Nisan and Schocken, MIT Pr	Ainstruction	1	٨
// File name: projects/05/CPU.hc	Cinstruction	0	
/ Tile name. projects/05/cro.ne	ALUtoA	0	
/**	ALUout[16]	1	
* The Central Processing unit * Consists of an ALU and a set * execute instructions written * In particular, the ALU execut	Aregin[16]	32767	
	loadA	1	
	Aout[16]	32767	
	AMout[16]	11111	
* to the Hack machine language	loadD	0	
* The D and A in the language s	Dout[16]	1	
* while M refers to the memory	ZRout	0	
* The inM input holds the value >	NGout	0	
< Internal input noids the value >	jeq	0	b.4
`	÷1+		-

```
set instruction %B1110001100000110, // D;JLE
tick, output, tock, output;
set instruction %B1110001100000111, // D;JMP
tick, output, tock, output;
set instruction %B1110111111010000, // D=1
tick, output, tock, output;
set instruction %B1110001100000001, // D;JGT
tick, output, tock, output;
set instruction %B1110001100000010, // D;JEQ
tick, output, tock, output;
set instruction %B1110001100000011, // D;JGE
tick, output, tock, output;
set instruction %B1110001100000100, // D;JLT
tick, output, tock, output;
set instruction %B1110001100000101, // D; JNE
tick, output, tock, output;
set instruction %B1110001100000110, // D;JLE
tick, output, tock, output;
set instruction %B1110001100000111, // D;JMP
tick, output, tock, output;
set reset 1:
tick, output, tock, output;
|set instruction %B011111111111111, // @32767
set reset 0:
tick, output, tock, output;
 <
                                                                      >
```



End of script - Comparison ended successfully

>

* Write: If load(t-1) then
* In words: the chip always out
* location specified by address
* into the memory location spec >

```
CHIP CPU {
    IN inM[16],
                         // M value input (M = contents of RAM[A])
        instruction[16], // Instruction for execution
                        // Signals whether to re-start the current program
                         // (reset == 1) or continue executing the current
                         // program (reset == 0).
    OUT outM[16],
                        // M value output
       writeM,
                        // Write into M?
        addressM[15],
                        // RAM address (of M)
        pc[15];
                         // ROM address (of next instruction)
   PARTS:
    // get type of instruction
    Not(in=instruction[15], out=Ainstruction);
   Not(in=Ainstruction, out=Cinstruction);
    And(a=Cinstruction, b=instruction[5], out=ALUtoA);
   Mux16(a=instruction, b=ALUout, sel=ALUtoA, out=Aregin);
    Or(a=Ainstruction, b=ALUtoA, out=loadA); // load A if A-inst or C-inst&dest to A-reg
    ARegister(in=Aregin, load=loadA, out=Aout);
   Mux16(a=Aout, b=inM, sel=instruction[12], out=AMout); // select A or M based on a-bit
    And(a=Cinstruction, b=instruction[4], out=loadD);
    DRegister(in=ALUout, load=loadD, out=Dout); // load the D register from ALU
    ALU(x=Dout, y=AMout, zx=instruction[11], nx=instruction[10],
        zy=instruction[9], ny=instruction[8], f=instruction[7],
        no=instruction[6], out=ALUout, zr=ZRout, ng=NGout); // calculate
    // Set outputs for writing memory
    Or16(a=false, b=Aout, out[0..14]=addressM);
    Or16(a=false, b=ALUout, out=outM);
    And(a=Cinstruction, b=instruction[3], out=writeM);
    // calc PCload & PCinc - whether to load PC with A reg
    And(a=ZRout, b=instruction[1], out=jeq); // is zero and jump if zero
    And(a=NGout, b=instruction[2], out=jlt); // is neg and jump if neg
    Or(a=ZRout, b=NGout, out=zeroOrNeg);
   Not(in=zeroOrNeg, out=positive);
                                               // is positive (not zero and not neg)
    And(a=positive, b=instruction[0], out=jgt); // is pos and jump if pos
    Or(a=jeq, b=jlt, out=jle);
    Or(a=jle, b=jgt, out=jumpToA);
                                                // load PC if cond met and jump if cond
    And(a=Cinstruction, b=jumpToA, out=PCload); // Only jump if C instruction
    Not(in=PCload, out=PCinc);
                                                // only inc if not load
    PC(in=Aout, inc=PCinc, load=PCload, reset=reset, out[0..14]=pc);
```

```
File Edit Selection Find View Goto Tools Project Preferences Help
```

Memory.hdl

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```
// This file is part of www.nand2tetris.org
// and the book "The Elements of Computing Systems"
// by Nisan and Schocken, MIT Press.
// File name: projects/05/Memory.hdl
 * This chip implements the complete address space of the
 * computer's data memory, including RAM and memory mapped I/O.
 * The chip facilitates read and write operations, as follows:
       Read: out(t) = Memory[address(t)](t)
       Write: If load(t-1) then Memorv[address(t-1)](t) = in(t-1)
 * In words: the chip always outputs the value stored at the memory
 * location specified by address. If load == 1, the in value is loaded
 * into the memory location specified by address. This value becomes
 * available through the out output in the next time step.
 * Address space rules:
 * Only the upper 16K+8K+1 words of the Memory chip are used.
 * Access to address>0x6000 is invalid. Access to any address in
 * the range 0x4000 to 0x5FFF results in accessing the screen memory
 * map. Access to address 0x6000 results in accessing the keyboard
 * memory map. The behavior in these addresses is described in the

    Screen and Keyboard chip specifications given in the book.

 */
CHIP Memory {
    IN in[16], load, address[15];
    OUT out[16];
    PARTS:
    DMux4Way(in=load, sel=address[13..14], a=loadram1, b=loadram2, c=loadscreen, d=loadkbd);
    Or(a=loadram1, b=loadram2, out=loadram);
    RAM16K(in=in, load=loadram, address=address[0..13], out=ramout);
    Screen(in=in, load=loadscreen, address=address[0..12], out=scrout);
    Keyboard(out=kbout);
    Mux4Way16(a=ramout, b=ramout, c=scrout, d=kbout, sel=address[13..14], out=out);
// 0000 000 RAM start
// 0011 FFF RAM end
// 0100 000 Screen start
// 0101 FFF Screen end
// 0110 000 Keyboard
```