1. Description

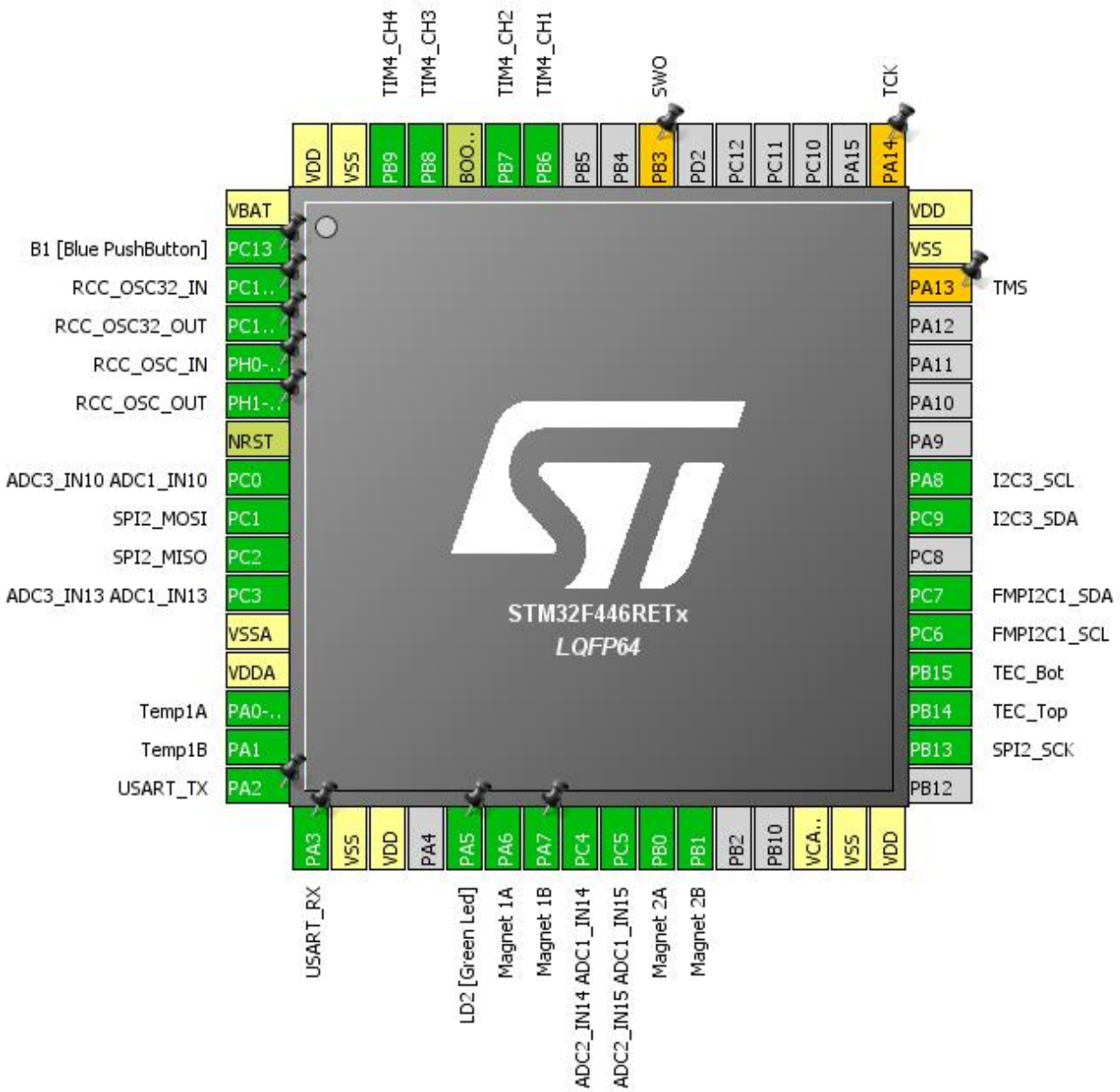
1.1. Project

Project Name	MPUTest
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 4.25.1
Date	05/13/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

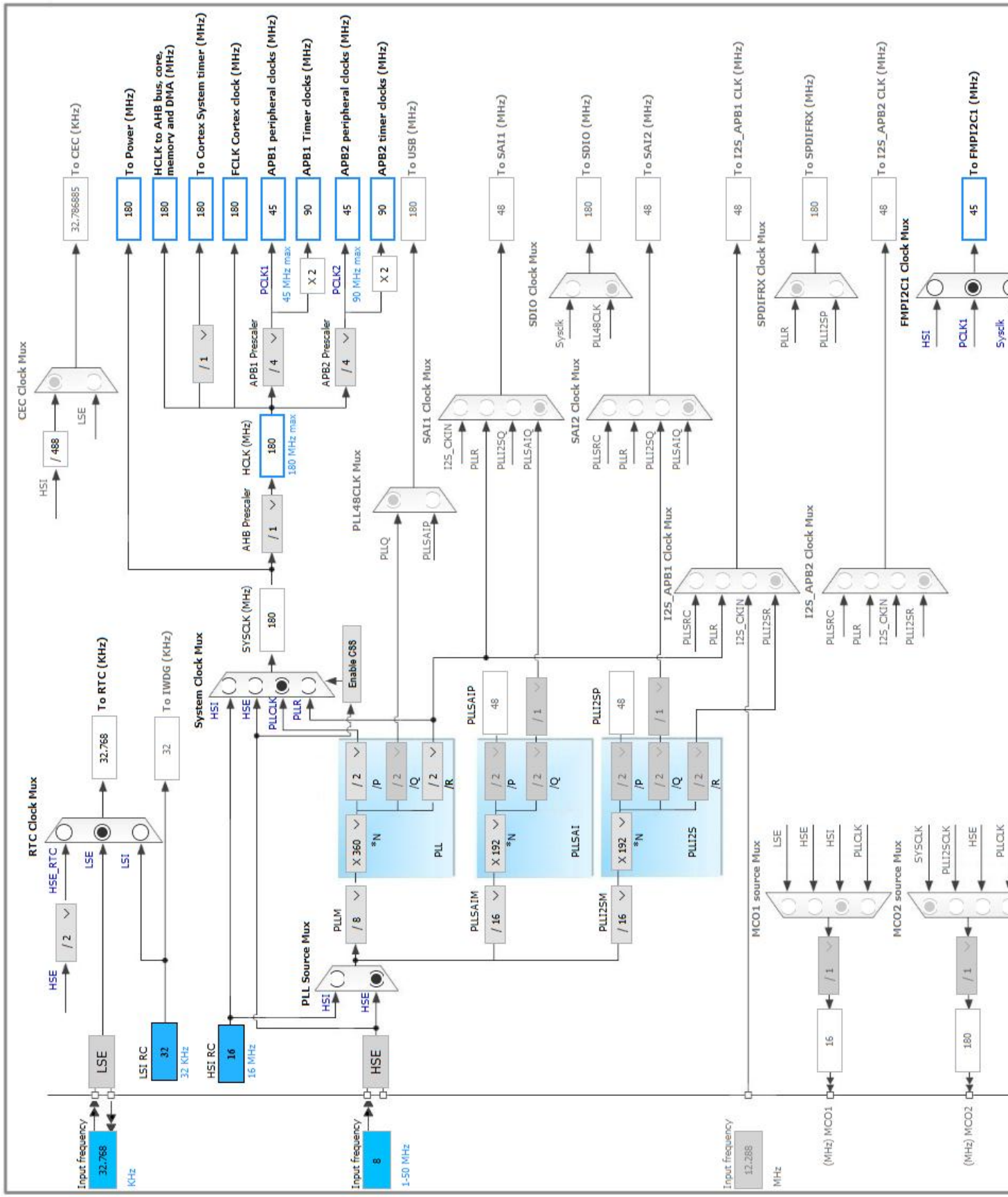
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC3_IN10, ADC1_IN10	
9	PC1	I/O	SPI2_MOSI	
10	PC2	I/O	SPI2_MISO	
11	PC3	I/O	ADC3_IN13, ADC1_IN13	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	Temp1A
15	PA1	I/O	ADC1_IN1	Temp1B
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	TIM3_CH1	Magnet 1A
23	PA7	I/O	TIM3_CH2	Magnet 1B
24	PC4	I/O	ADC2_IN14, ADC1_IN14	
25	PC5	I/O	ADC2_IN15, ADC1_IN15	
26	PB0	I/O	TIM3_CH3	Magnet 2A
27	PB1	I/O	TIM3_CH4	Magnet 2B
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
34	PB13	I/O	SPI2_SCK	
35	PB14	I/O	TIM12_CH1	TEC_Top
36	PB15	I/O	TIM12_CH2	TEC_Bot
37	PC6	I/O	FMPI2C1_SCL	
38	PC7	I/O	FMPI2C1_SDA	
40	PC9	I/O	I2C3_SDA	
41	PA8	I/O	I2C3_SCL	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
46	PA13 **	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14 **	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	
62	PB9	I/O	TIM4_CH4	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0
mode: IN1
mode: IN10
mode: IN13
mode: IN14
mode: IN15
mode: Vrefint Channel
mode: Vbat Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**12 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	**15 Cycles ***
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**15 Cycles ***
Rank	**3 ***

Channel	**Channel 10 ***
Sampling Time	**15 Cycles ***
Rank	**4 ***
Channel	**Channel 13 ***
Sampling Time	**15 Cycles ***
Rank	**5 ***
Channel	**Channel 14 ***
Sampling Time	**15 Cycles ***
Rank	**6 ***
Channel	**Channel 15 ***
Sampling Time	**15 Cycles ***
Rank	**7 ***
Channel	Channel 0
Sampling Time	**15 Cycles ***
Rank	**8 ***
Channel	**Channel 1 ***
Sampling Time	**15 Cycles ***
Rank	**9 ***
Channel	**Channel 10 ***
Sampling Time	**15 Cycles ***
Rank	**10 ***
Channel	**Channel 13 ***
Sampling Time	**15 Cycles ***
Rank	**11 ***
Channel	**Channel 14 ***
Sampling Time	**15 Cycles ***
Rank	**12 ***
Channel	**Channel 15 ***
Sampling Time	**15 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles
Injected Offset	0
Rank	**2 ***
Channel	Channel 0

Sampling Time	3 Cycles
Injected Offset	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN14

mode: IN15

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 15 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN10
mode: IN13

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 10
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. FMPI2C1

I2C: I2C

5.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00401650 ***

Slave Features:

Clock No Stretch Mode	Clock Stretch Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.5. I2C3

I2C: I2C

5.5.1. Parameter Settings:

Master Features:

I2C Speed Mode	**Fast Mode ***
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.6. RCC

High Speed Clock (HSE): BYPASS Clock Source
Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled

Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

5.7. RTC

mode: Activate Clock Source

mode: Activate Calendar

5.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	**11 ***
Minutes	**18 ***
Seconds	**10 ***
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	**Wednesday ***
Month	**April ***
Date	**11 ***
Year	0

5.8. SPI2

Mode: Full-Duplex Master

5.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**22.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.9. SYS

Timebase Source: TIM6

5.10. TIM3

Channel1: Output Compare CH1
Channel2: Output Compare CH2
Channel3: Output Compare CH3
Channel4: Output Compare CH4

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	**Enable (Trigger delayed for master/slaves simultaneous start) ***
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 1:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

Output Compare Channel 2:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

Output Compare Channel 3:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

Output Compare Channel 4:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

5.11. TIM4

Channel1: Output Compare CH1
Channel2: Output Compare CH2
Channel3: Output Compare CH3
Channel4: Output Compare CH4

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	**Enable (Trigger delayed for master/slaves simultaneous start) ***
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 1:

Mode	**Active Level on match ***
Pulse (16 bits value)	0

CH Polarity	High

Output Compare Channel 2:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

Output Compare Channel 3:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

Output Compare Channel 4:

Mode	**Active Level on match ***
Pulse (16 bits value)	0
CH Polarity	High

5.12. TIM12

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**TEC_PWM_PERIOD-1 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.13. USART2

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	**230400 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.14. FREERTOS

mode: Enabled

5.14.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	**256 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled

USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	**Dynamic / Static ***
TOTAL_HEAP_SIZE	**4096 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	**Enabled ***
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	**Enabled ***

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.14.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled

uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	**Enabled ***

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	Temp1A
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	Temp1B
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC4	ADC2_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC2_IN15	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC0	ADC3_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC3_IN13	Analog mode	No pull-up and no pull-down	n/a	
FMPI2C1	PC6	FMPI2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PC7	FMPI2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Magnet 1A

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Magnet 1B
	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	Magnet 2A
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	Magnet 2B
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	TEC_Top
	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	TEC_Bot
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	USART_RX
Single Mapped Signals	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***
I2C3_RX	DMA1_Stream1	Peripheral To Memory	Low

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

I2C3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
USART2 global interrupt	true	5	0
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	5	0
I2C3 event interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
FMPI2C1 event interrupt	unused		
FMPI2C1 error interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	027107_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	MPUTest
Project Folder	D:\Users\Tyler\Documents\tyler\School\University of Toronto\CAN-
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.21.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report