CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group #: _____12_____

Team Members: _____

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Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*
- Ty:
  - Earn a B
  - Develop a functional processor
- Adnan:
  - Earn at least a B
  - Learn how to incorporate what is learned in class into the labs
- Zach:
  - Learn to write more advanced assembly programs
  - Earn at least a B in the course
- Tianshu

- Earn a B
- Get to know more about vhdl design and assembly language.

Team Expectations:

- **Conduct:** *Complete tasks in a timely manner. Don't plagiarize.*
- **Communication:** *GroupMe, respond at least within a day to any questions. Google Doc with tasks and progress updates, update every time progress is made.*
- **Group conventions:** *inputs in the form "i_*", outputs "o_*" signals "s_*". 2008 emulation options. General implementation tested first, edge cases second. If do files are included properly config. Github: commit every time you do work. Comment at developer discretion, adhere to group requests as needed.*
- **Meetings:** *Examples of other issues to consider include:*
  - *Work together in-person outside of lab sections (a few absences are excused at group discretion):*
    - *Mondays: 7pm*
    - *Tuesdays: 6pm*
    - *Meet for integration with specific components as needed*
  - *Work separately on responsibilities*
    - *Divide work amongst pairs, integrate and reschedule at full group meetings*
- **Peer Evaluation Criteria:** *Evaluate group members based on time spent as well as progress made. Keeping up with progress report.*

Role Responsibilities: *Also complete appropriate portions of the report doc as parts are completed.*

Lab Part	Estimated Time	Design		Test	
		Lead	Deadline	Lead	Deadline
High-level design/Integration	3 hr	(all together)	3/6	(all together)	3/6
Control logic	2 hr	(all together)	3/6	(all together)	3/6
Fetch logic	3 hr	Ty	3/6	Tianshu	3/6
Barrel shifter	2 hr	Hamza	3/6	Zach	3/6
Multiplier	3 hr	Adnan	3/6	Declan	3/6
ALU integration + Misc Ypdates	3	(all together)	3/13	(all together)	3/13
Test Programs	4 hr	(all together)	3/25	(all together)	3/25
Synthesis (human effort)	1.5 hr	(all together)	3/25	(all together)	3/25

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature _____ **Date** _____

Student Signature _____ **Date** _____

Student Signature _____ **Date** _____

Student Signature _____ **Date** _____

Student Signature _____ **Date** _____

Student Signature _____ **Date** _____